Rev 0; 10/02

DS1086 Spread-Spectrum EconOscillator

General Description

The DS1086 EconOscillator™ is a programmable clock generator that produces a spread-spectrum (dithered) square-wave output of frequencies from 260kHz to 133MHz. The selectable dithered output reduces radiated-emission peaks by dithering the frequency 2% or 4% below the programmed frequency. The DS1086 has a power-down mode and an output-enable control for power-sensitive applications. All the device settings are stored in nonvolatile (NV) EEPROM memory allowing it to operate in stand-alone applications.

Applications

Printers
Copiers
PCs
Computer Peripherals
Cell Phones
Cable Modems

Features

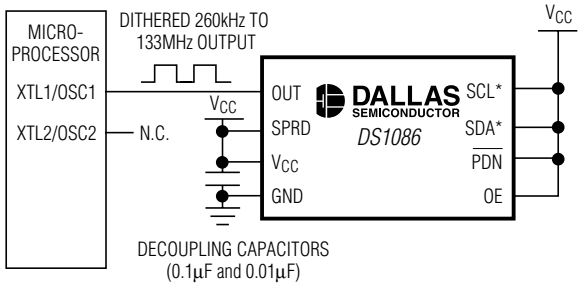
- **User-Programmable Square-Wave Generator**
- **Frequencies Programmable from 260kHz to 133MHz**
- **2% or 4% Selectable Dithered Output**
- **Glitchless Output-Enable Control**
- **2-Wire Serial Interface**
- **Nonvolatile Settings**
- **5V Supply**
- **No External Timing Components Required**
- **Power-Down Mode**
- **10kHz Master Frequency Step Size**
- **EMI Reduction**

Ordering Information

PART	PIN-PACKAGE
DS1086U*	8 µSOP (118mil)
DS1086Z	8 SO (150mil)

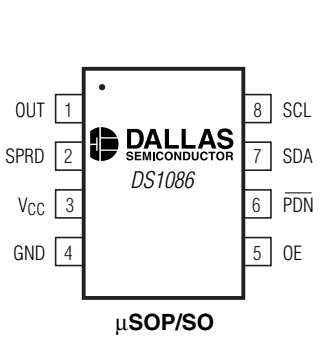
**Future Product*

Typical Operating Circuit



*SDA AND SCL CAN BE CONNECTED DIRECTLY HIGH IF THE DS1086 NEVER NEEDS TO BE PROGRAMMED IN-CIRCUIT, INCLUDING DURING PRODUCTION TESTING.

Pin Configuration



µSOP/SO

EconOscillator is a trademark of Dallas Semiconductor.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Relative to Ground .....-0.5V to +6.0V
Voltage on SPRD, $\overline{PDN}$, OE, SDA,
SCL Relative to Ground (See Note 1).....-0.5 to (V_{CC} + 0.5V)

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A

Note 1: This voltage must not exceed 6.0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.75	5.00	5.25	V
High-Level Input Voltage (SDA, SCL)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL)	V_{IL}		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (SPRD, $\overline{PDN}$, OE)	V_{IH}		2		V_{CC} + 0.3	V
Low-Level Input Voltage (SPRD, $\overline{PDN}$, OE)	V_{IL}		-0.3		0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Output Voltage (OUT)	V_{OH}	I_{OH} = -4mA, V_{CC} = min	2.4			V
Low-Level Output Voltage (OUT)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Input Current	I_{IH}	V_{CC} = 5.25V			1	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0	-1			µA
Supply Current (Active)	I_{CC}	C_L = 15pF (output at default frequency)			35	mA
Standby Current (Power-Down)	I_{CCQ}	Power-down mode			10	µA

MASTER OSCILLATOR CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Master Oscillator Range	f_{OSC}	(Note 2)		66		133	MHz
Default Master Oscillator Frequency	f_0				97.1		MHz
Master Oscillator Frequency Tolerance	$\frac{\Delta f_0}{f_0}$	V_{CC} = 5V, T_A = +25°C (Note 3)	Default frequency	-0.75		+0.75	%
			DAC step size	-0.75		+0.75	
Voltage Frequency Variation	$\frac{\Delta f_V}{f_0}$	Over voltage range, T_A = +25°C (Note 4)	Default frequency	-0.75		+0.75	%
			DAC step size	-0.75		+0.75	
Temperature Frequency Variation	$\frac{\Delta f_T}{f_0}$	Over temperature range, T_A = +25°C (Note 5)	Default frequency	-0.5		+0.5	%
			133MHz	-0.5		+0.5	
			66MHz	-1.0		+1.0	
Dither Frequency Range	$\frac{\Delta f}{f_0}$	Prescaler bit J0 = 1 (Note 6)			2		%
		Prescaler bit J0 = 0 (Note 6)			4		
Integral Nonlinearity of Frequency DAC	INL	Entire range (Note 7)		-0.4		+0.4	%
DAC Step Size		Δ between two consecutive DAC values (Note 8)			10		kHz
DAC Span		Frequency range for one offset setting (see Table 2)			10.24		MHz
DAC Default		Factory default register setting			500		decimal
Offset Step Size		Δ between two consecutive offset values (see Table 2)			5.12		MHz
Offset Default	OS	Factory default OFFSET register setting (5 LSBs) (see Table 2)			RANGE (5 LSBs of RANGE register)		hex

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency Stable After Prescaler Change					1	Period
Frequency Stable After DAC or Offset Change		(Note 9)		0.2	1	ms
Power-Up Time	t_{por} + t_{stab}	(Note 10)		0.1	0.5	ms
Enable of OUT After Exiting Power-Down Mode	t_{stab}				500	µs
OUT High-Z After Entering Power-Down Mode	t_{stab}				0.1	ms
Load Capacitance	C_L	(Note 11)		15	50	pF
Output Duty Cycle (OUT)			40		60	%
$\overline{PDN}$ Rise/Fall Time					1	µs

AC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	(Note 12)			400	kHz
		Standard mode				100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	(Note 12)	1.3			µs
		Standard mode		4.7			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode	(Notes 12, 13)	0.6			µs
		Standard mode		4.0			
LOW Period of SCL	t_{LOW}	Fast mode	(Note 12)	1.3			µs
		Standard mode		4.7			
HIGH Period of SCL	t_{HIGH}	Fast mode	(Note 12)	0.6			µs
		Standard mode		4.0			
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	(Note 12)	0.6			µs
		Standard mode		4.7			
Data Hold Time	$t_{HD:DAT}$	Fast mode	(Notes 12, 14, 15)	0		0.9	µs
		Standard mode					
Data Setup Time	$t_{SU:DAT}$	Fast mode	(Note 12)	100			ns
		Standard mode		250			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode	(Note 16)	20 + 0.1C_B		300	ns
		Standard mode		20 + 0.1C_B		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode	(Note 16)	20 + 0.1C_B		300	ns
		Standard mode		20 + 0.1C_B		1000	

AC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE (continued)

(V_{CC} = 5V ±5%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line	C_B	(Note 16)			400	pF
NV Write-Cycle Time	t_{WR}				10	ms
Input Capacitance	C_I			5		pF

Note 1: All voltages are referenced to ground.

Note 2: DAC and OFFSET register settings must be configured to maintain the clock frequency within this range. Correct operation of the device is not guaranteed if these limits are exceeded.

Note 3: This is the absolute accuracy of the master oscillator frequency at the default settings.

Note 4: This is the change that is observed in master oscillator frequency with changes in voltage from nominal voltage at T_A = +25°C.

Note 5: This is the percentage frequency change from the +25°C frequency due to temperature at V_{CC} = 5V. The maximum temperature change varies with the master frequency setting. The minimum occurs at the default master frequency ($f_{default}$). The maximum occurs at the extremes of the output frequency range (66MHz or 133MHz) (see Figure 2).

Note 6: The dither deviation of the master frequency is unidirectional and lower than the undithered frequency.

Note 7: The integral nonlinearity of the frequency adjust DAC is a measure of the deviation from a straight line drawn between the two endpoints of a range. The error is in percentage of the span.

Note 8: This is true when the prescaler = 1.

Note 9: Frequency settles faster for small changes in value. During a change, the frequency transitions smoothly from the original value to the new value.

Note 10: This indicates the time elapsed between power-up and the output becoming active. An on-chip delay is intentionally introduced to allow the oscillator to stabilize. t_{stab} is equivalent to approximately 512 master clock cycles and therefore depends on the programmed clock frequency.

Note 11: Output voltage swings can be impaired at high frequencies combined with high output loading.

Note 12: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line at least $t_{R\ MAX}$ + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.

Note 13: After this period, the first clock pulse is generated.

Note 14: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Note 15: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 16: C_B—total capacitance of one bus line, timing referenced to 0.9 x V_{CC} and 0.1 x V_{CC}.

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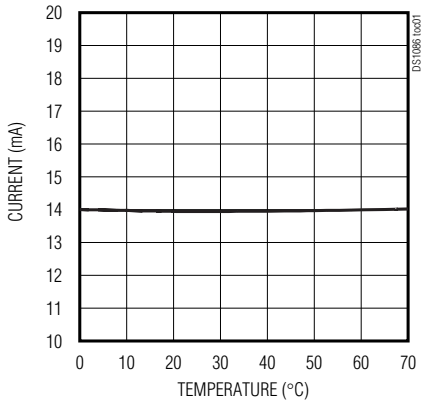
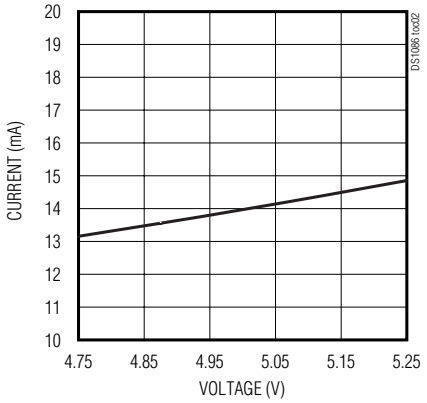
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = 25°C, unless otherwise noted)

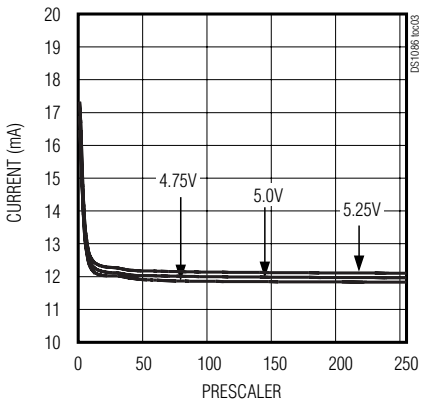
SUPPLY CURRENT vs. TEMPERATURE



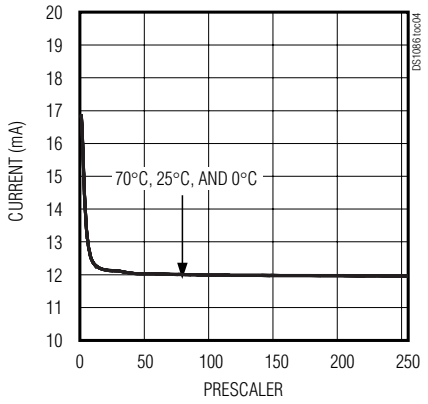
SUPPLY CURRENT vs. VOLTAGE



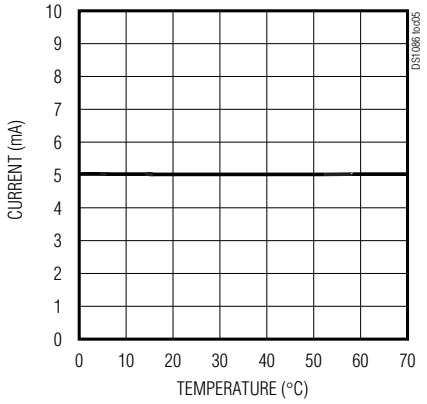
SUPPLY CURRENT vs. PRESCALER



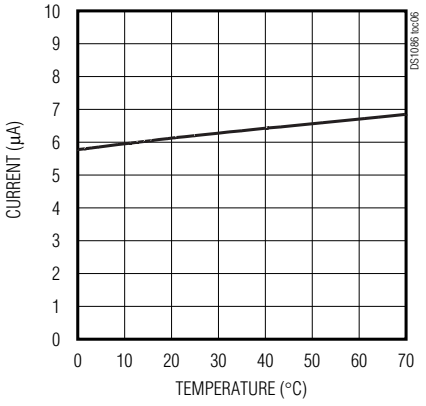
SUPPLY CURRENT vs. PRESCALER



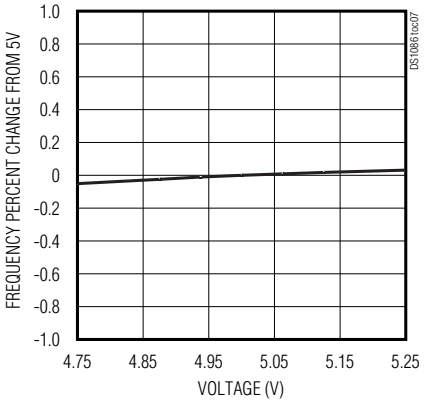
SUPPLY CURRENT vs. TEMPERATURE WITH OE = 0



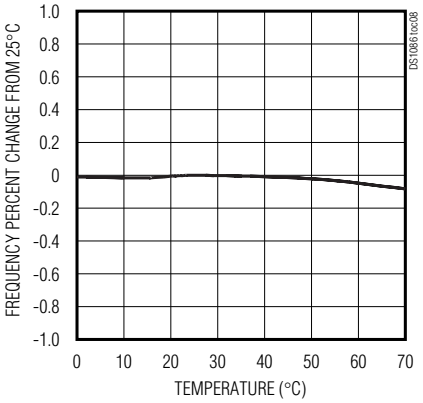
SUPPLY CURRENT vs. TEMPERATURE WITH $\overline{PDN}$ = 0



FREQUENCY PERCENT CHANGE vs. SUPPLY VOLTAGE



FREQUENCY PERCENT CHANGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	OUT	Oscillator Output
2	SPRD	Dither Enable. When the pin is high, the dither is enabled. When the pin is low, the dither is disabled.
3	V_{CC}	Power Supply
4	GND	Ground
5	OE	Output Enable. When the pin is high, the output buffer is enabled. When the pin is low, the output is disabled but the master oscillator is still on.
6	$\overline{PDN}$	Power-Down. When the pin is high, the master oscillator is enabled. When the pin is low, the master oscillator is disabled (power-down mode).
7	SDA	2-Wire Serial Data. This pin is for serial data transfer to and from the device. The pin is open drain and can be wire-OR'ed with other open-drain or open-collector interfaces.
8	SCL	2-Wire Serial Clock. This pin is used to clock data into the device on rising edges and clock data out on falling edges.

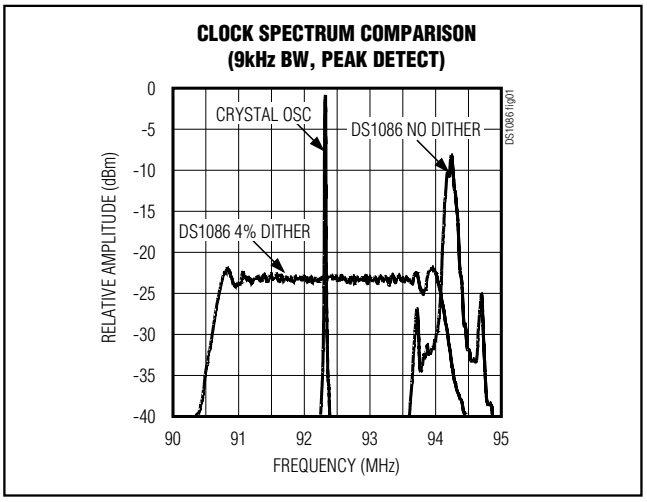


Figure 1. Clock Spectrum Dither Comparison

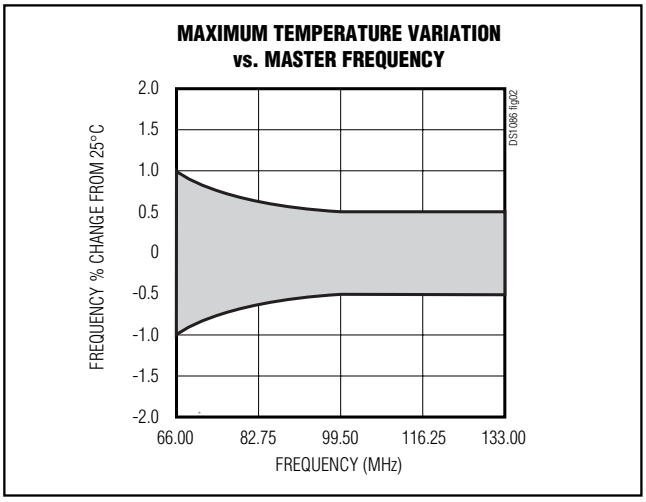
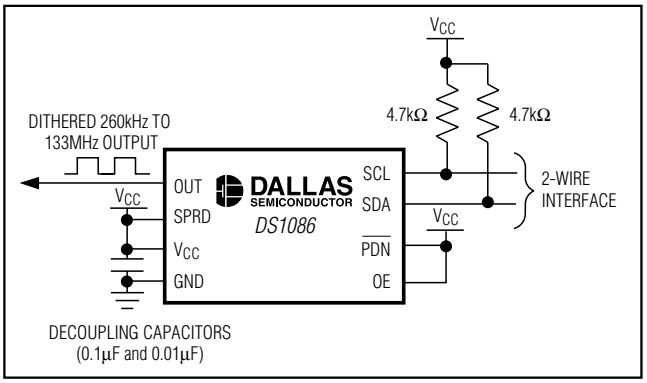


Figure 2. Temperature Variation Over Frequency

Processor-Controlled Mode



Stand-Alone Mode

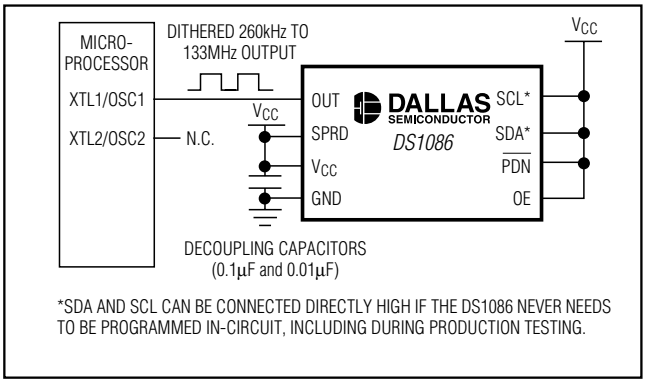


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Table 1. Register Summary

REGISTER	ADDR	MSB				BINARY			LSB	FACTORY DEFAULT	ACCESS
PRESCALER	02h	X_1	X_1	X_X	J0	P3	P2	P1	P0	11100000b	R/W
DAC HIGH	08h	b9	b8	b7	b6	b5	b4	b3	b2	01111101b	R/W
DAC LOW	09h	b1	b0	X_0	X_0	X_0	X_0	X_0	X_0	00000000b	R/W
OFFSET	0Eh	X_1	X_1	X_1	b4	b3	b2	b1	b0	111-----b	R/W
ADDR	0Dh	X_1	X_1	X_1	X_1	WC	A2	A1	A0	11110000b	R/W
RANGE	37h	X_X	X_X	X_X	b4	b3	b2	b1	b0	xxx-----b	R
WRITE EE	3Fh	NO DATA								—	—

X_0 = Don't care, reads as zero.

X_1 = Don't care, reads as one.

X_X = Don't care, reads indeterminate.

X = Don't care.

Table 2. Offset Settings

OFFSET	FREQUENCY RANGE (MHz)
OS - 6	61.44 to 71.67
OS - 5	66.56 to 76.79
OS - 4	71.68 to 81.91
OS - 3	76.80 to 87.03
OS - 2	81.92 to 92.15
OS - 1	87.04 to 97.27
OS*	92.16 to 102.39
OS + 1	97.28 to 107.51
OS + 2	102.40 to 112.63
OS + 3	107.52 to 117.75
OS + 4	112.64 to 122.87
OS + 5	117.76 to 127.99
OS + 6	122.88 to 133.11

**Factory default setting. OS is the integer value of the 5 LSBs of the RANGE register.*

Detailed Description

A block diagram of the DS1086 is shown in Figure 3. The internal master oscillator generates a square wave with a 66MHz to 133MHz frequency range. The frequency of the master oscillator can be programmed with the DAC register over a two-to-one range in 10kHz steps. The master oscillator range is larger than the range possible with the DAC step size, so the OFFSET register is used to select a smaller range of frequencies over which the DAC spans. The prescaler can then be set to divide the master oscillator frequency by 2^x (where x equals 0 to 8) before routing the signal to the output (OUT) pin.

A programmable triangle-wave generator injects an offset element into the master oscillator to dither its output 2% or 4%. The dither is controlled by the J0 bit in the PRESCALER register and enabled with the SPRD pin. The maximum spectral attenuation occurs when the prescaler is set to 1. The spectral attenuation is reduced by 2.7dB for every factor of 2 that is used in the prescaler. This happens because the prescaler's divider function tends to average the dither in creating the lower frequency. However, the most stringent spectral emission limits are imposed on the higher frequencies where the prescaler is set to a low divider ratio.

The external control input, OE, gates the clock output buffer. The $\overline{PDN}$ pin disables the master oscillator and turns off the clock output for power-sensitive applications*. On power-up, the clock output is disabled until power is stable and the master oscillator has generated 512 clock cycles. Both controls feature a synchronous enable that ensures there are no output glitches when the output is enabled, and a constant time interval (for a given frequency setting) from an enable signal to the first output transition.

The control registers are programmed through a 2-wire interface and are used to determine the output frequency and settings. Once programmed into EEPROM, since the register settings are NV, the settings only need to be reprogrammed if it is desired to reconfigure the device.

**The power-down command must persist for at least two output frequency cycles plus 10µs for deglitching purposes.*

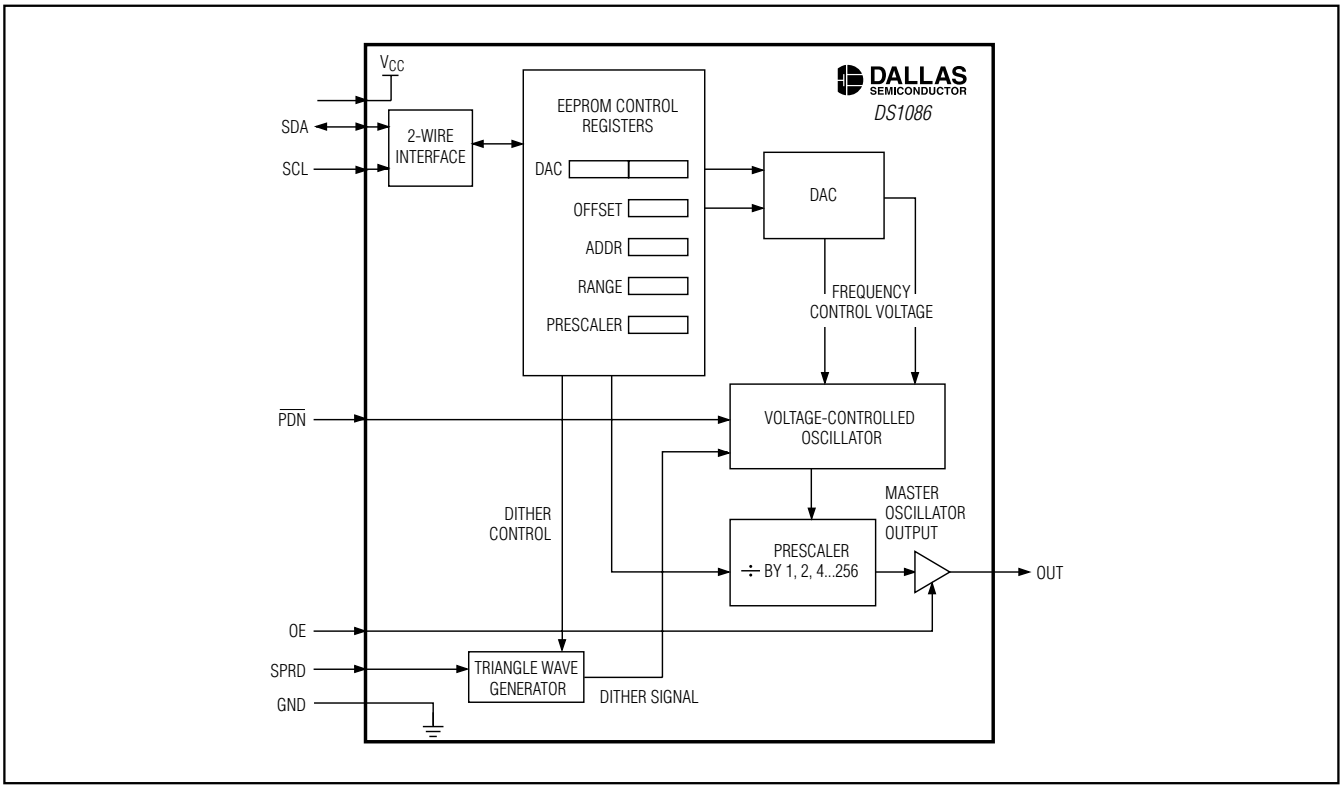

Figure 3. DS1086 Block Diagram

The output frequency is determined by the following equation:

$$f_{OUTPUT} = \frac{(\text{MIN FREQUENCY OF SELECTED OFFSET RANGE}) + (\text{DAC VALUE} \times 10\text{kHz STEP SIZE})}{\text{PRESCALER}} \quad (1)$$

where: *min frequency of selected OFFSET range* is the lowest frequency (shown in Table 2 for the corresponding offset).

DAC value is the value of the DAC register (0 to 1023).

Prescaler is the value of 2^x where x = 0 to 8.

See the *Example Frequency Calculations* section for a more in-depth look at using the registers.

Register Definitions

The DS1086 registers are used to determine the output frequency and dither amount. A summary of the registers is shown in Table 1. Using the default register settings below, the default output frequency is 97.1MHz. See the *Example Frequency Calculations* section for an example on how to determine the register settings for a desired output frequency.

PRESCALER Register

The PRESCALER register controls the prescaler (bits P3 to P0) and dither (bit J0). The prescaler divides the master oscillator frequency by 2^x where x can be from 0 to 8. Any prescaler value entered that is greater than 8 decodes as 8. The dither applied to the output is controlled with bit J0. When J0 is high, 2% peak dither is selected. When J0 is low, 4% peak dither is selected.

DAC HIGH/DAC LOW Register

The 2-byte DAC register sets the frequency of the master oscillator to a particular value within the current offset range. Each step of the DAC changes the master oscillator frequency by 10kHz. The first byte is the MSB (DAC HIGH) and the second byte is the LSB (DAC LOW).

OFFSET Register

The OFFSET register determines the range of frequencies that can be obtained for a given DAC setting. The factory default offset is copied into the RANGE register so the user can access the default offset after making changes to the OFFSET register. See Table 2 for OFFSET ranges.

Correct operation of the device is not guaranteed outside the range 66MHz to 133MHz.

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ADDR Register

The A0, A1, A2 bits determine the 2-wire slave address. The WC bit determines if the EEPROM is to be written to after register contents have been changed. If WC = 0 (default), EEPROM is written automatically after a WRITE EE command. If WC = 1, the EEPROM is only written when the WRITE EE command is issued. In applications where the register contents are frequently written, the WC bit should be set to 1. Otherwise, it is necessary to wait for an EEPROM write cycle to complete between writing to the registers. This also prevents wearing out the EEPROM. Regardless of the value of the WC bit, the value of the ADDR register is always written immediately to EEPROM. When the WRITE EE command has been received, the contents of the registers are written into the EEPROM, thus locking in the register settings.

RANGE Register

This read-only register contains a copy of the factory-set offset (OS). This value can be read to determine the default value of the OFFSET register when programming a new master oscillator frequency.

WRITE EE Command

This command is used to write data from RAM to EEPROM when the WC bit in ADDR register is 1. See the *ADDR Register* section for more details.

Example Frequency Calculations

Example #1: ***Calculate the register values needed to generate a desired output frequency of 11.0592MHz.***
Since the desired frequency is not within the valid master oscillator range of 66MHz to 133MHz, the prescaler must be used. Valid prescaler values are 2^X where x equals 0 to 8 (and x is the value that is programmed into the P3 to P0 bits of the PRESCALER register). Equation 1 shows the relationship between the desired frequency, the master oscillator frequency, and the prescaler.

$$f_{DESIRED} = \frac{f_{MASTER\ OSCILLATOR}}{prescaler} = \frac{f_{MASTER\ OSCILLATOR}}{2^X} \quad (2)$$

By trial and error, x is incremented from 0 to 8 in Equation 2, finding values of x that yield master oscillator frequencies within the range of 66MHz to 133MHz.

Equation 2 shows that a prescaler of 8 (x = 3) and a master oscillator frequency of 88.4736MHz generates our desired frequency. In terms of the device register, x = 3 is programmed in the lower four bits of the PRESCALER register. Writing 03h to the PRESCALER register sets the PRESCALER to 8 (and 4% peak dither). Be aware that the J0 bit also resides in the PRESCALER register.

$$f_{MASTER\ OSCILLATOR} = f_{DESIRED} \times prescaler = f_{DESIRED} \times 2^X$$

$$f_{MASTER\ OSCILLATOR} = 11.0592MHz \times 2^3 = 88.4736MHz \quad (3)$$

Once the target master oscillator frequency has been calculated, the value of offset can be determined. Using Table 2, 88.4736MHz falls within both OS - 1 and OS - 2. However, choosing OS - 1 would be a poor choice since 88.4736MHz is so close to OS - 1's minimum frequency. On the other hand, OS - 2 is ideal since 88.4736MHz is very close to the center of OS - 2's frequency span. Before the OFFSET register can be programmed, the default value of offset (OS)

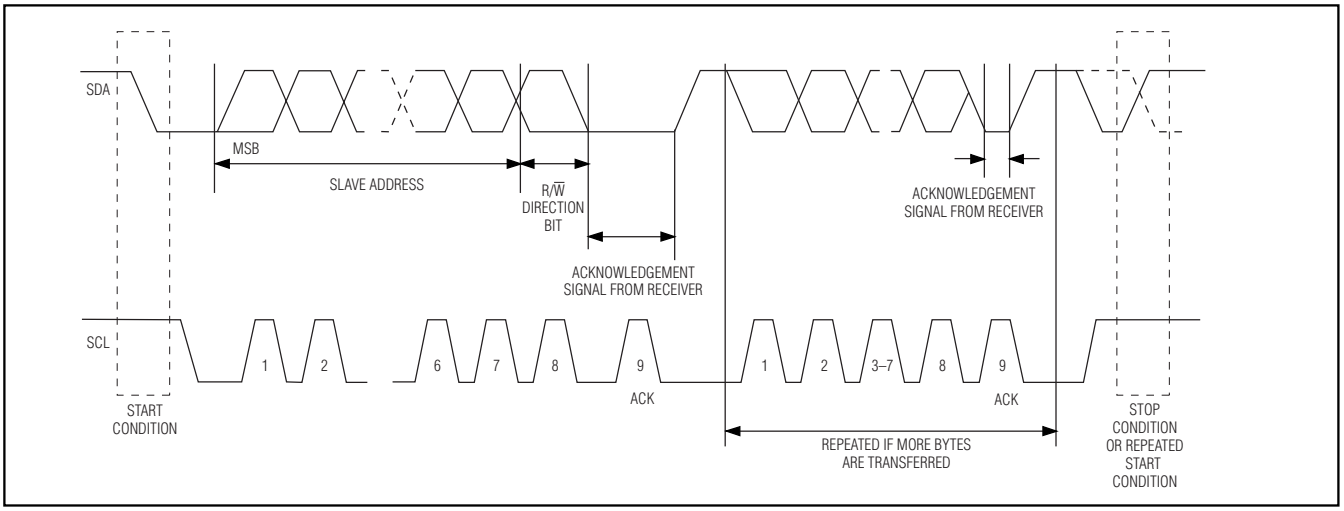

Figure 4. 2-Wire Data Transfer Protocol

must be read from the RANGE register (last five bits). In this example, 12h (18 decimal) was read from the RANGE register. OS - 2 for this case is 10h (16 decimal). This is the value that is written to the OFFSET register.

Finally, the two-byte DAC value needs to be determined. Since OS - 2 only sets the range of frequencies, the DAC selects one frequency within that range as shown in Equation 3.

$$f_{MASTER\ OSCILLATOR} = (\text{MIN FREQUENCY OF SELECTED OFFSET RANGE}) + (\text{DAC value} \times 10\text{kHz})$$

Valid values of DAC are 0 to 1023 (decimal) and 10kHz is the step size. Equation 4 is derived from rearranging Equation 3 and solving for DAC.

$$\text{DAC VALUE} = \frac{(f_{MASTER\ OSCILLATOR} - \text{MIN FREQUENCY OF SELECTED OFFSET RANGE})}{10\text{kHz STEP SIZE}}$$

$$\text{DAC VALUE} = \frac{(88.4736\text{MHz} - 81.92\text{MHz})}{10\text{kHz STEP SIZE}} = 655.36 \approx 655 \text{ (decimal)} \quad (4)$$

Since the two-byte DAC register is left justified, 655 is converted to hex (028Fh) and bit-wise shifted left six places. The value to be programmed into the DAC register is A3C0h.

In summary, the DS1086 is programmed as follows:

PRESCALER = 03h (4% peak dither) or 13h (2% peak dither)

OFFSET = OS - 2 or 10h (if range was read as 12h)

DAC = A3C0h

Notice that the DAC value was rounded. Unfortunately, this means that some error is introduced. In order to calculate how much error, a combination of Equation 1 and Equation 3 is used to calculate the expected output frequency. See Equation 5.

$$f_{OUTPUT} = \frac{(\text{MIN FREQUENCY OF SELECTED OFFSET RANGE}) + (\text{DAC VALUE} \times 10\text{kHz STEP SIZE})}{\text{prescaler}}$$

$$f_{OUTPUT} = \frac{(81.92\text{MHz}) + (655 \times 10\text{kHz})}{8} = \frac{88.47\text{MHz}}{8} = 11.05875\text{MHz} \quad (5)$$

The expected output frequency is not exactly equal to the desired frequency of 11.0592MHz. The difference is 450Hz. In terms of percentage, Equation 6 shows that the expected error is 0.004%. The expected error assumes typical values and does not include deviations from the typical as specified in the electrical tables.

$$\%\text{ERROR}_{EXPECTED} = \frac{f_{DESIRED} - f_{EXPECTED}}{f_{DESIRED}} \times 100$$

$$\%\text{ERROR}_{EXPECTED} = \frac{11.0592\text{MHz} - 11.05875\text{MHz}}{11.0592\text{MHz}} \times 100 = \frac{450\text{Hz}}{11.0592\text{MHz}} \times 100 = 0.004\% \quad (6)$$

Example #2: ***Calculate the register values needed to generate a desired output frequency of 100MHz.***

Since the desired frequency is already within the valid master oscillator frequency range, the prescaler is set to divide by 1, and hence, PRESCALER = 00h (for 4% peak dither) or 10h (for 2% peak dither).

$$f_{MASTER\ OSCILLATOR} = 100.0\text{MHz} \times 2^0 = 100.0\text{MHz} \quad (7)$$

Next, looking at Table 2, OS + 1 provides a range of frequencies centered around the desired frequency. In order to determine what value to write to the OFFSET register, the RANGE register must first be read. Assuming 12h was read in this example, 13h (OS + 1) is written to the OFFSET register.

Finally, the DAC value is calculated as shown in Equation 8.

$$\text{DAC VALUE} = \frac{(100.0\text{MHz} - 97.28\text{MHz})}{10\text{kHz STEP SIZE}} = 272.00 \text{ (decimal)} \quad (8)$$

The result is then converted to hex (0110h) and then left-shifted, resulting in 4400h to be programmed into the DAC register.

In summary, the DS1086 is programmed as follows:

PRESCALER = 00h (4% peak dither) or 10h (2% peak dither)

OFFSET = OS + 1 or 13h (if RANGE was read as 12h)

DAC = 4400h

$$f_{OUTPUT} = \frac{(97.28\text{MHz}) + (272 \times 10\text{kHz})}{2^0} = \frac{100.0\text{MHz}}{1} = 100.0\text{MHz} \quad (9)$$

DS1086 Spread-Spectrum EconOscillator

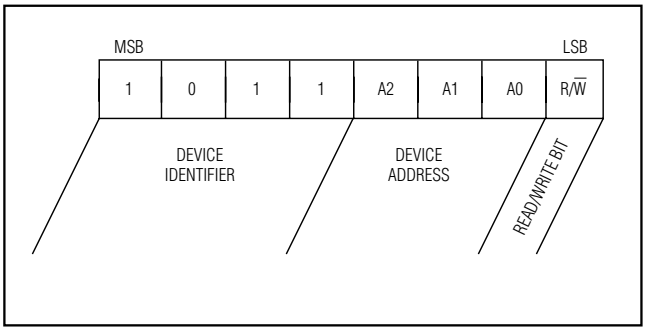

Figure 5. Slave Address

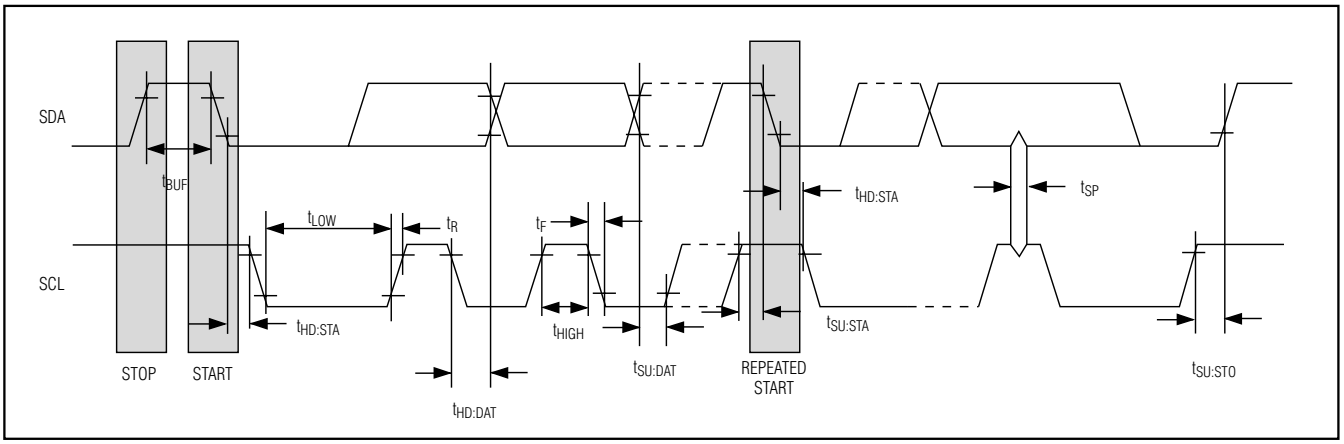

Figure 6. 2-Wire AC Characteristics

Since the expected output frequency is equal to the desired frequency, the calculated error is 0%.

2-Wire Serial Port Operation

2-WIRE SERIAL DATA BUS

The DS1086 communicates through a 2-wire serial interface. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1086 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figures 4 and 6):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1086 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the byte has been received. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1086 EEPROM is being written to, it is not able to perform additional responses. In this case, the slave DS1086 sends a not acknowledge to any data transfer request made by the master. It resumes normal operation when the EEPROM operation is complete.

A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figures 4, 5, 6, and 7 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

1) Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2) Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1086 can operate in the following two modes:

Slave receiver mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1086 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Slave Address

Figure 5 shows the first byte sent to the device. It includes the device identifier, device address, and the R/$\overline{W}$ bit. The device address is determined by the ADDR register.

Registers/Commands

See Table 1 for the complete list of registers/commands and Figure 7 for an example of using them.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1086, decouple the power supply with 0.01µF and 0.1µF high-quality, ceramic, surface-mount capacitors. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. These capacitors should be placed as close to pins 3 and 4 as possible.

Stand-Alone Mode

SCL and SDA cannot be left floating when they are not used. If the DS1086 never needs to be programmed in-circuit, including during production testing, SDA and SCL can be tied high. The SPRD pin must be tied either high or low.

DS1086 Spread-Spectrum EconOscillator

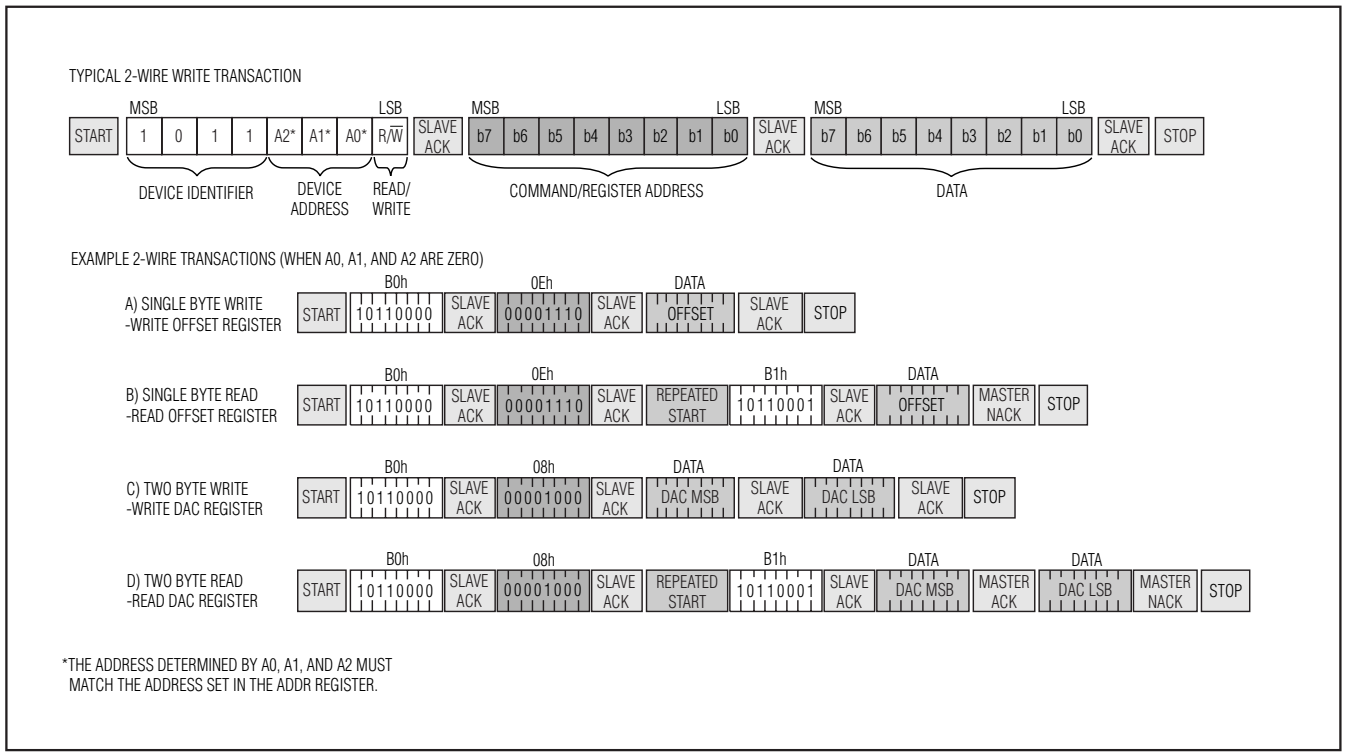

Figure 7. 2-Wire Transactions

Chip Topology

TRANSISTOR COUNT: 10,000

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.