



STV7697A

PLASMA DISPLAY PANEL SCAN DRIVER

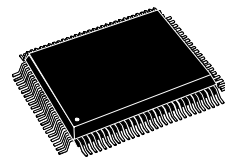
FEATURES

- 64 Outputs Plasma Display Driver
- 170V Absolute Maximum Rating
- 5V Supply for Logic
- -200/850 mA Peak Output Current
- 1000 mA Source / Sink Output Diode
- 64-Bit Shift Register (15 MHz)
- Blank Control
- Complementary Output Control
- BCD Technology
- 100 Pin-PQFP Package or Dice.

DESCRIPTION

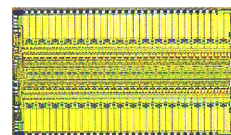
The STV7697A is a scan driver for Plasma Display Panel (PDP) implemented in ST's proprietary BCD technology. Using a 64-bit cascable 15 MHz shift register, it drives 64 high current & high voltage outputs. By serially connecting several STV7697A, any vertical pixel definition can be performed. The STV7697A is supplied with a separated 160V power output supply and a 5V logic supply. All command inputs are CMOS compatible.

The STV7697A package is a 100 pin-PQFP.



PQFP100 (14 x 20 x 2.80 mm)
(Full Plastic Quad Flat Pack)

ORDER CODE: STV7697A



ORDER CODE: STV7697A/WAF (1)
(1): Unsawn Tested Wafer

Version 4.8

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2 PIN ASSIGNMENT

2.1 PQFP100 package

Pin Number	Symbol	Type	Function
33-37-44-48-81-84-97-100	V _{PP}	Supply	High voltage supply of power outputs
41 - 90	V _{CC}	Supply	5 V logic supply
34-35-36-45-46-47-82-83-98-99	V _{SSP}	Ground	Ground of power outputs
38-43	V _{SSSUB}	Ground	Substrate ground
39-40-42-94	V _{SSLOG}	Ground	Logic ground
1 to 32, 49 to 80	OUT 64 to OUT 1	Output	Power output
91	SOUT (SIN)	Output	Shift register data output (forward)
85	POL	Input	Polarity selection
86	BLK	Input	Output blanking command
87	F/R	Input	Selection of shift direction
89	SIN (SOUT)	Input	Shift register data input (forward)
92	STB	Input	Latch of data to outputs
93	CLK	Input	Clock of data shift register
88-95-96	NC	-	

2.2 Power outputs

Output N°	Pin N°	Output N°	Pin N°	Output N°	Pin N°	Output N°	Pin N°
1	80	17	64	33	32	49	16
2	79	18	63	34	31	50	15
3	78	19	62	35	30	51	14
4	77	20	61	36	29	52	13
5	76	21	60	37	28	53	12
6	75	22	59	38	27	54	11
7	74	23	58	39	26	55	10
8	73	24	57	40	25	56	9
9	72	25	56	41	24	57	8
10	71	26	55	42	23	58	7
11	70	27	54	43	22	59	6
12	69	28	53	44	21	60	5
13	68	29	52	45	20	61	4
14	67	30	51	46	19	62	3
15	66	31	50	47	18	63	2
16	65	32	49	48	17	64	1

3 PADS DIMENSIONS (in μm)/ PADS POSITIONS

The reference is the centre of the die ($x=0$, $y=0$)

TOP SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	Size: y
V _{PP}	2468.5	4135.0	75.0	90.0
V _{SSP}	2313.5	4135.0	75.0	90.0
V _{SSP}	2188.5	4135.0	75.0	90.0
V _{PP}	2063.5	4134.5	75.0	90.0
V _{SSLOG}	1620.0	4135.0	75.0	90.0
CLK	1430.0	4135.0	75.0	90.0
STB	-781.0	4135.0	75.0	90.0
SOUT	-612.5	4135.0	75.0	90.0
V _{CC}	-335.5	4144.5	75.0	90.0
SIN	379.5	4135.0	75.0	90.0
F/R	548.0	4135.0	75.0	90.0
BLK	1082.0	4135.0	75.0	90.0
POL	1853.0	4135.0	75.0	90.0
V _{PP}	2021.5	4140.0	75.0	90.0
V _{SSP}	2156.5	4140.0	75.0	90.0
V _{SSP}	2291.5	4140.0	75.0	90.0
V _{PP}	2454.5	4129.5	75.0	90.0

BOTTOM SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	Size: y
OUT34	2468.0	4087.5	75.0	90.0
OUT33	2318.0	4089.5	75.0	90.0
V _{PP}	2182.0	4089.5	75.0	90.0
V _{SSP}	2047.0	4093.0	75.0	90.0
V _{SSP}	1912.0	4093.0	75.0	90.0
V _{SSP}	1777.0	4093.0	75.0	90.0
V _{PP}	1642.0	4089.5	75.0	90.0
V _{SSSUB}	-683.0	4088.0	75.0	90.0
V _{SSLOG}	-382.5	4088.0	75.0	90.0
V _{SSLOG}	419.5	4087.5	75.0	90.0
V _{CC}	618.5	4087.5	75.0	90.0
V _{SSLOG}	951.0	-4087.5	75.0	90.0
V _{SSSUB}	1308.0	-4087.5	75.0	90.0
V _{PP}	1438.5	-4087.5	75.0	90.0
V _{SSP}	1797.5	-4093.5	75.0	90.0
V _{SSP}	1932.5	-4093.5	75.0	90.0
V _{SSP}	2067.5	-4093.5	75.0	90.0
V _{PP}	2193.0	-4093.5	75.0	90.0
OUT32	2318.0	-4093.5	75.0	90.0
OUT31	2468.5	-4093.5	75.0	90.0

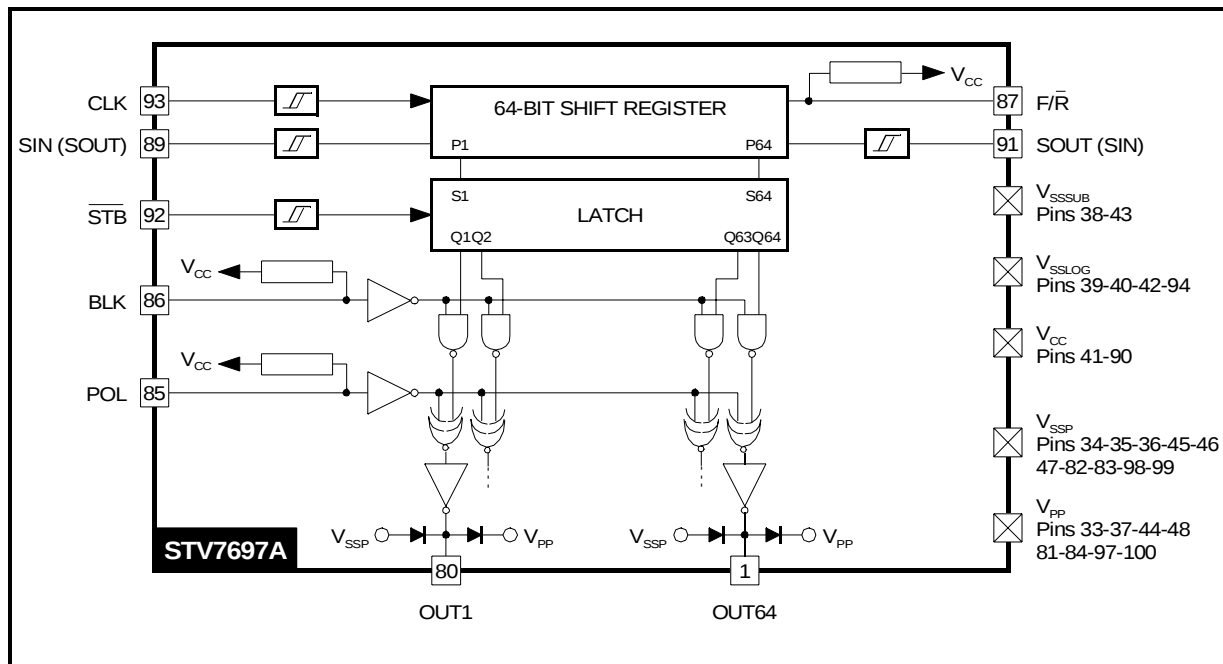
RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	Size: y
OUT1	2647.0	3697.0	90.0	75.0
OUT2	2647.0	3484.0	90.0	75.0
OUT3	2647.0	3238.5	90.0	75.0
OUT4	2647.0	2992.5	90.0	75.0
OUT5	2647.0	2743.0	90.0	75.0
OUT6	2647.0	2506.5	90.0	75.0
OUT7	2647.0	2264.0	90.0	75.0
OUT8	2647.0	2018.0	90.0	75.0
OUT9	2647.0	1774.5	90.0	75.0
OUT10	2647.0	1529.0	90.0	75.0
OUT11	2647.0	1285.5	90.0	75.0
OUT12	2647.0	1040.0	90.0	75.0
OUT13	2647.0	796.5	90.0	75.0
OUT14	2647.0	551.0	90.0	75.0
OUT15	2647.0	307.5	90.0	75.0
OUT16	2647.0	62.0	90.0	75.0
OUT17	2647.0	-181.5	90.0	75.0
OUT18	2647.0	-427.0	90.0	75.0
OUT19	2647.0	-670.5	90.0	75.0
OUT20	2647.0	-916.0	90.0	75.0
OUT21	2647.0	-1159.5	90.0	75.0
OUT22	2647.0	-1405.0	90.0	75.0
OUT23	2647.0	-1648.5	90.0	75.0
OUT24	2647.0	-1894.0	90.0	75.0
OUT25	2647.0	-2137.5	90.0	75.0
OUT26	2647.0	-2383.5	90.0	75.0
OUT27	2647.0	-2627.0	90.0	75.0
OUT28	2647.0	-2872.5	90.0	75.0
OUT29	2647.0	-3116.0	90.0	75.0
OUT30	2647.0	-3363.0	90.0	75.0

LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	Size: y
OUT35	-2646.5	-3363.0	90.0	75.0
OUT36	-2646.5	-3116.0	90.0	75.0
OUT37	-2646.5	-2872.5	90.0	75.0
OUT38	-2646.5	-2627.0	90.0	75.0
OUT39	-2646.5	-2383.5	90.0	75.0
OUT40	-2646.5	-2137.5	90.0	75.0
OUT41	-2646.5	-1894.0	90.0	75.0
OUT42	-2646.5	-1648.5	90.0	75.0
OUT43	-2646.5	-1405.0	90.0	75.0
OUT44	-2646.5	-1159.5	90.0	75.0
OUT45	-2646.5	-916.0	90.0	75.0
OUT46	-2646.5	-670.5	90.0	75.0
OUT47	-2646.5	-427.0	90.0	75.0
OUT48	-2646.5	-181.5	90.0	75.0
OUT49	-2646.5	62.0	90.0	75.0
OUT50	-2646.5	307.5	90.0	75.0
OUT51	-2646.5	551.0	90.0	75.0
OUT52	-2646.5	796.5	90.0	75.0
OUT53	-2646.5	1040.0	90.0	75.0
OUT54	-2646.5	1285.5	90.0	75.0
OUT55	-2646.5	1529.0	90.0	75.0
OUT56	-2646.5	1774.5	90.0	75.0
OUT57	-2646.5	2018.0	90.0	75.0
OUT58	-2646.5	2264.0	90.0	75.0
OUT59	-2646.5	2506.5	90.0	75.0
OUT60	-2646.5	2743.0	90.0	75.0
OUT61	-2646.5	2949.5	90.0	75.0
OUT62	-2646.5	3228.5	90.0	75.0
OUT63	-2646.5	3487.0	90.0	75.0
OUT64	-2646.5	3763.0	90.0	75.0

4 BLOCK DIAGRAM



5 CIRCUIT DESCRIPTION

The STV7697A contains all the logic and the power circuits necessary to drive rows of a Plasma Display Panel (P. D. P.). The state of the displayed line is loaded into the shift register. Data are shifted at each low to high transition of the (CLK) shift clock. After 64 shifts the first bit is available at the serial output. This output can be used to cascade several drivers to perform any vertical resolution.

The forward / reverse ($F/\bar{R}$) input is used to select the direction of the shift register, data input/output status is set according to the selected direction. SIN, CLK, $\overline{STB}$ inputs are Smith trigger inputs. If not used on the application, $F/\bar{R}$, BLK, POL logical inputs are internally pulled to level "1". The maximum frequency of the shift clock is 15 MHz.

All the data are memorized into the latch stage when the strobe input ($\overline{STB}$) is pulled high.

Blanking input (BLK) forces the power outputs to high level when pulled high with polarity input (POL) at high level and forced to low level with POL at low level.

The level of the power output is inverted when the polarity command (POL) is pulled high.

Sustain current must not be sunk in the power output to V_{PP} when the power supply is applied.

V_{SSLOG} and V_{SSSUB} must be connected as close as possible to the logical reference ground of the application.

Table 1. Shift Register Truth Table

Input		Input/Output		Shift Register Function
$F/\bar{R}$	CLK	SIN	SOUT	Output Q
H	Rise	IN	OUT	Forward Shift
H	H or L	IN	OUT	Steady
L	Rise	OUT	IN	Reverse Shift
L	H or L	OUT	IN	Steady

Table 2. Power Output Truth Table

Qn (1)	$\overline{STB}$	BLK	POL	Driver Output	Comments
X	X	H	H	All H	Forced to High
X	X	H	L	All L	Forced to Low
H	L	L	L	H	Copy Data
L	L	L	L	L	Copy Data
H	L	L	H	L	Copy Inverted Data
L	L	L	H	H	Copy Inverted Data
X	H	L	L	Qn	Data Latched
X	H	L	H	$\overline{Qn}$	Inverted Data Latched

Note 1: Qn is the parallel output of the shift register (n = 1 to 64). Qn takes the value of serial input (SIN) after "n" shift clock periods.

6 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Range	-0.3, +7	V
V_{PP}	Driver Supply Range	-0.3, +170	V
V_{PP_waf}	Driver supply range - Die package	-0.3, +150	V
V_{IN}	Logic Input Voltage Range	-0.3, $V_{CC} + 0.3$	V
V_{OUT}	Logic Output Voltage Range	-0.3, $V_{CC} + 0.3$	V
V_{POUT}	Driver Output Voltage Range	-0.3, V_{PP}	V
I_{POUT}	Driver Output Current (3) (5)	-250/+850	mA
I_{DOUT}	Diode Output Current (4) (5)	±1000	mA
T_{oper}	Operating Temperature	-20, +85	°C
T_{jmax}	Junction Temperature (2)	+125	°C
T_{stg}	Storage Temperature	-50,+150	°C

ESD susceptibility

Human Body Model:100pF, 1.5kΩ.

All pins withstand ±2.2kV except power outputs: 1.7kV in positive voltage discharge.

7 THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance (2) Max	50	°C/W
P_{oper}	Operating Power Dissipation ($T_{amb} = 25^{\circ}C$) Max	2	W
T_{joper}	Operating Junction Temperature (2) Max	+125	°C

Note 2:For PQFP100 packaging.

Note 3:Through one power output.

Note 4:Through one power output with $V_{PP} = V_{SSP}$ (see test diagram).

Note 5:These parameters are measured during ST's internal qualification which includes temperature characterization on standard batches and on corners batches of the process. These parameters are not tested on the parts.

8 ELECTRICAL CHARACTERISTICS

($V_{CC} = 5\text{ V}$, $V_{PP} = 160\text{ V}$, $V_{SSP} = 0\text{ V}$, $V_{SSLOG} = V_{SSSUB} = 0\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $f_{CLK} = 15\text{ MHz}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current (all inputs high)		-	-	100	μA
I_{CCL}	Logic Supply Current	$f_{CLK} = 8\text{ MHz}$, $SIN = 1010$	-	5.3	-	mA
V_{PP}	Power Output Supply Voltage		15	-	160	V
V_{PP_waf}	Power Output Supply Voltage (Die package)		15		140	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	μA
OUTPUT						
OUT1-OUT64						
V_{POUTH}	Power Output High Level (voltage drop versus V_{PP} , $V_{PP}=90\text{V}$)	$I_{POUTH} = -10\text{ mA}$ $I_{POUTH} = -40\text{ mA}$	5 10	3 5	- -	V V
I_{POUTH_peak}	Power Output Peak Current (9)	$V_{PP} = 130\text{V}$		-200		mA
V_{POUTL}	Power Output Low Level	$I_{POUTL} = 200\text{ mA}$	-	3.1	10	V
I_{POUTL_peak}	Power Output Peak Current (6)	$V_{POUTL} = 30\text{V}$ $V_{CC} = 5\text{V}$		650		mA
V_{DOUTH1}	Output Diode High Level	$I_{DOUTH} = +400\text{ mA}$ (7) (8)	-	2	-	V
V_{DOUTL1}	Output Diode Low Level	$I_{DOUTL} = -400\text{ mA}$ (7) (8)	-	-1.5	-	V
V_{DOUTH2}	Output Diode High Level	$I_{DOUTH} = +1000\text{ mA}$ (7)		5		V
V_{DOUTL2}	Output Diode Low Level	$I_{DOUTL} = -1000\text{ mA}$ (7)		-3		V
SOUT/SIN						
V_{OH}	Logic Output High Level	$I_{OH} = 1\text{ mA}$	4	-	-	V
V_{OL}	Logic Output Low Level	$I_{OL} = -1\text{ mA}$	-	-	0.4	V
INPUT (CLK, F/R, STB, POL, BLK, SIN/SOUT)						
V_{IH}	Input High Level		$0.8 V_{CC}$	-	-	V
V_{IL}	Input Low Level		-	-	$0.2V_{CC}$	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$	-	-	10	μA
I_{IL}	Low Level Input Current CLK, SIN/SOUT, STB, F/R, BLK, POL	$V_{IL} = 0\text{ V}$	- -	- 70	10 100	μA μA

Note 6: Peak current: pulse mode 720 Hz, 200ns pulse width, $V_{CC}=5\text{ V}$.

Note 7: Compatible with power dissipation (see [Figure 2. Test Configuration](#)).

Note 8: The typical value increases when more than one output is activated.

Note 9: These parameters are measured during ST's internal qualification which includes temperature characterization on standard batches and on corners batches of the process. These parameters are not tested on the parts.

9 AC TIMINGS REQUIREMENTS

($V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_{amb} = -20\text{ to }+85^{\circ}\text{C}$, input signals max leading edge & trailing edge (t_R , t_F) = 10 ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	66	-	-	ns
t_{WHCLK}	Duration of clock (CLK) pulse at high level	15	-	-	ns
t_{LHCLK}	Duration of clock (CLK) pulse at low level	15	-	-	ns
t_{SDAT}	Set-up Time of data input before clock low to high transition	10	-	-	ns
t_{HDATA}	Hold Time of data input after clock low to high transition	10	-	-	ns
t_{SFR}	Forward/reverse ($F/\bar{R}$) Set-up Time before low to high transition	100	-	-	ns
t_{DSTB}	Minimum Delay to latch STB after clock low to high transition	10	-	-	ns
t_{STB}	Strobe $\overline{STB}$ Pulse Duration	20	-	-	ns
t_{BLK}	Blank (BLK) Pulse Duration	500	-	-	ns
t_{POL}	Polarity (POL) Pulse Duration	500	-	-	ns

10 AC TIMINGS CHARACTERISTICS

($V_{CC} = 5\text{ V}$, $V_{PP} = 90\text{ V}$, $V_{SSP} = 0\text{ V}$, $V_{SSLOG} = V_{SSSUB} = 0\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, $f_{CLK} = 15\text{ MHz}$,
 $V_{ILMax.} = 0.2 V_{CC}$, $V_{IHMin.} = 0.8 V_{CC}$, $V_{OH} = 4.0\text{ V}$, $V_{OL} = 0.4\text{ V}$, $C_L = 15\text{ pF}$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	66	-	-	ns
t_{RDATA} t_{FDATA}	Logical Data Output Rise Time Logical Data Output Fall Time	- -	20 11	- -	ns ns
t_{PHL1}	Delay of logic data output change high to low transition after CLK transition	-	45	80	ns
t_{PLH1}	Delay of logic data output change low to high transition after CLK transition	-	48	80	ns
t_{PHL2}	Delay of power output change high to low transition after CLK transition	-	120	180	ns
t_{PLH2}	Delay of power output change low to high transition after CLK transition	-	120	180	ns
t_{PHL3}	Delay of power output change high to low transition after BLK transition	-	110	165	ns
t_{PLH3}	Delay of power output change low to high transition after BLK transition	-	110	165	ns
t_{PHL4}	Delay of power output change high to low transition after POL transition	-	-	160	ns
t_{PLH4}	Delay of power output change low to high transition after POL transition	-	-	160	ns
t_{ROUT}	Power Output Rise Time (10)	-	120	200	ns
t_{FOUT}	Power Output Fall Time (10)	-	40	100	ns

Note 10: One output among 64, loading capacitor $C_{OUT} = 200\text{ pF}$, other outputs at low level.

Figure 1. AC Characteristics Waveform

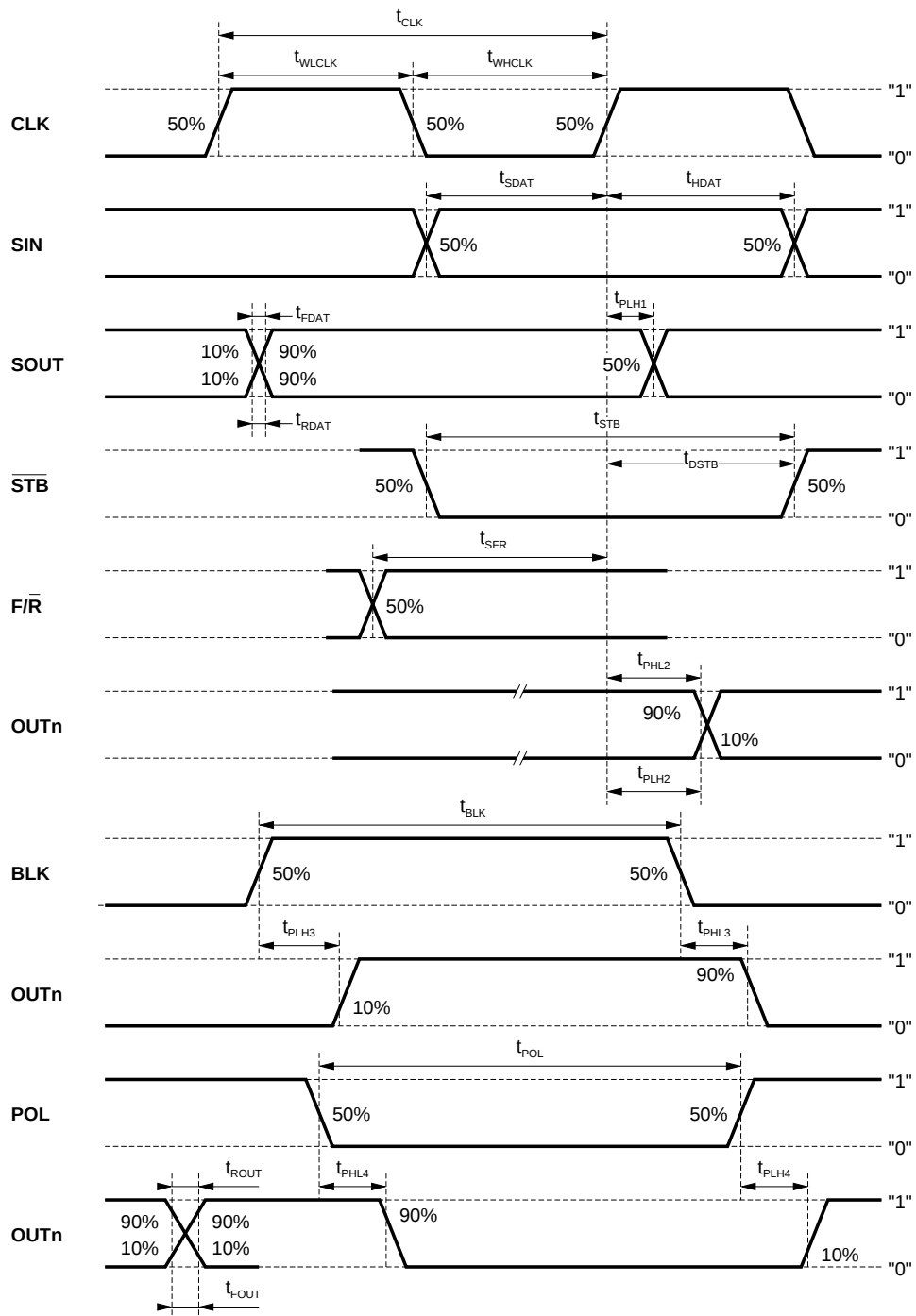
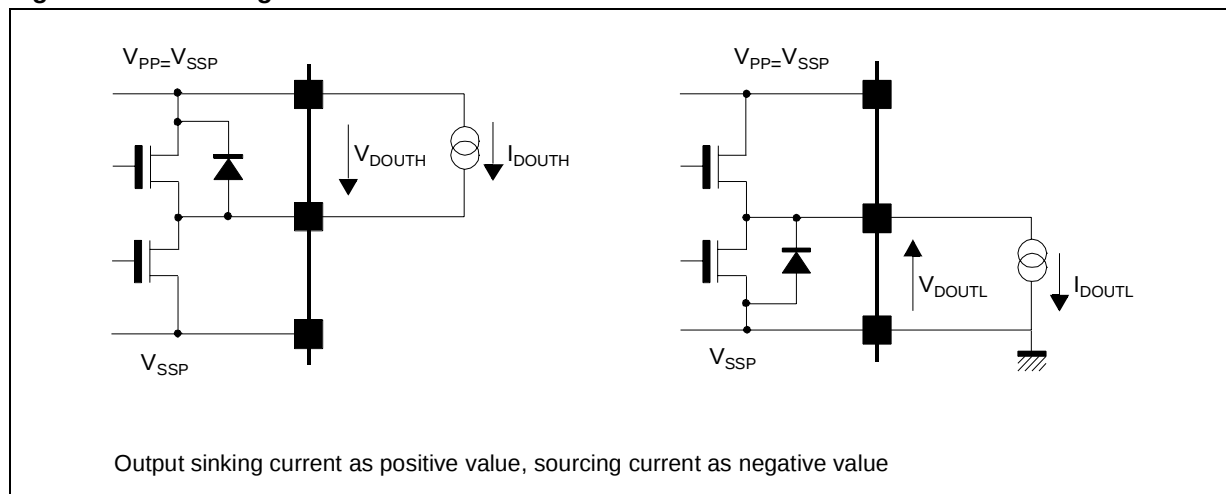


Figure 2. Test Configuration



11 INPUT/OUTPUT SCHEMATICS

Figure 3. $\overline{F/R}$, BLK, POL, HIZ

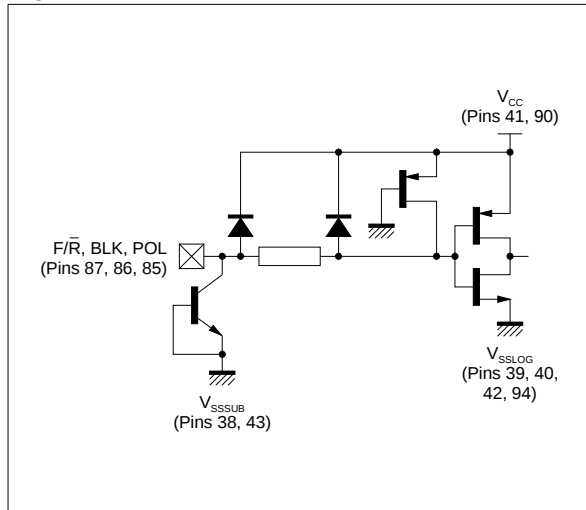


Figure 5. SIN, SOUT Input

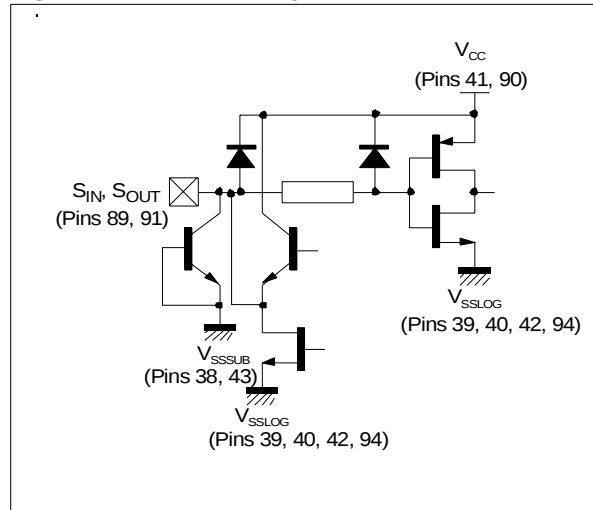


Figure 4. CLK, $\overline{STB}$

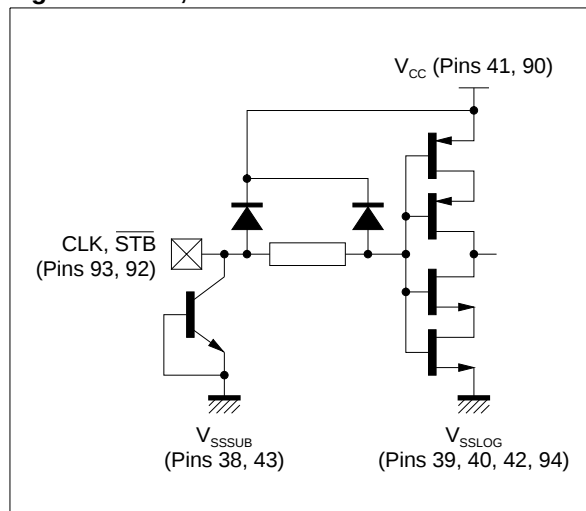
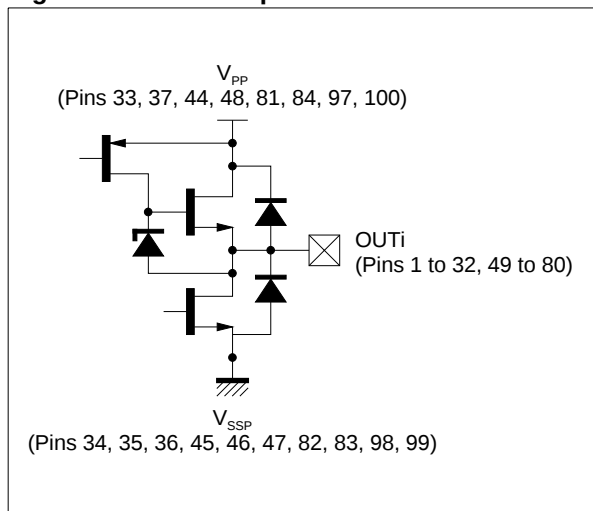


Figure 6. Power Output



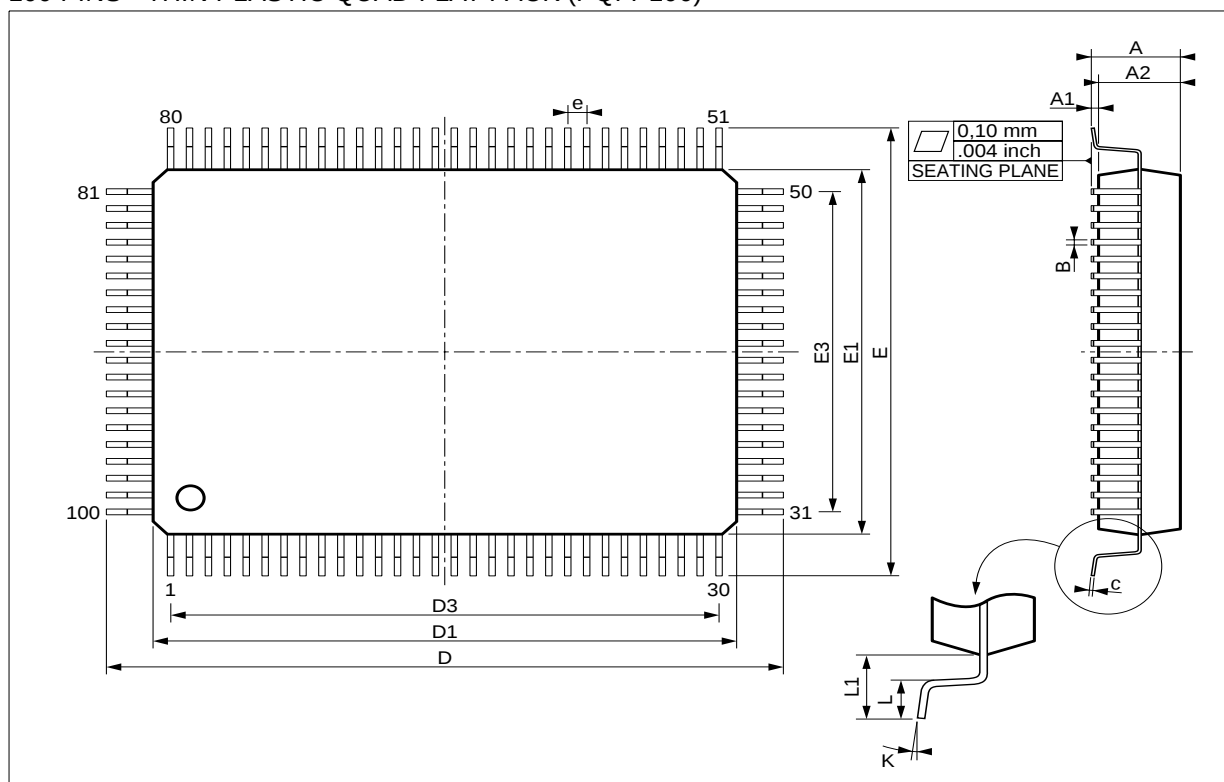
12 TESTED WAFER DISCLAIMER

All wafers are tested and guaranteed to comply with all datasheet limits up to the point of wafer sawing for a period of ninety (90) days from the delivery date.

We remind you that it is the customer's responsibility to test and qualify their application in which the die is used. ST Microelectronics is ready to support the customer when qualifying the product.

13 PACKAGE MECHANICAL DATA

100 PINS - THIN PLASTIC QUAD FLAT PACK (PQFP100)



Dimensions	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (Min.), 7° (Max.)					

14 Revision History

Table 1 Summary of Modifications

Version	Date	Description
4.7	23 January 2003	Changed "TQFP" to "PQFP" on pages 2, 3 and 4. Global change of f_{CLK} from 20 to 15 MHz and t_{CLK} Min. from 50 to 66 ns.
4.8	30 January 2003	Global change of f_{CLK} from 20 to 15 MHz and t_{CLK} Min. from 50 to 66 ns.

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