

UCC3952A-1, UCC3952A-2, UCC3952A-3, UCC3952A-4 SINGLE-CELL LITHIUM-ION BATTERY PROTECTION IC

SLUS463C – AUGUST 2000 – REVISED MARCH 2001

AVAILABLE OPTIONS

TA	PACKAGES BCC-18 (GSH)	NORMAL TO OVERCHARGE			OVERVOLTAGE TO NORMAL RECOVERY			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
-20°C to 70°C	UCC3952AGSH-1	4.15	4.2	4.25	3.85	3.90	3.95	V
	UCC3952AGSH-2	4.20	4.25	4.30	3.90	3.95	4.00	V
	UCC3952AGSH-3	4.25	4.30	4.35	3.95	4.00	4.05	V
	UCC3952AGSH-4	4.30	4.35	4.40	4.00	4.05	4.10	V

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage (PACK+ to BNEG)	7 V
Maximum forward voltage (PACK+ to PACK-)	16 V
Maximum reverse voltage (where PACK+ to BNEG = 5V)	-8 V
Maximum cell continuous charge current	3.5 A
Junction temperature, T _J	-55°C to 150°C
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Data Book for thermal limitations and considerations of packages. All voltages are referenced to GND.

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**electrical characteristics, $T_A = -20^\circ\text{C}$ to 70°C , all voltages are with respect to BNEG
(unless otherwise stated)**

state transition threshold

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	
V_{OV}	Normal to overcharge voltage	UCC3952A-1		4.15	4.20	4.25	V
			$T_A = 25^\circ\text{C}$	4.175	4.20	4.235	
		UCC3952A-2		4.20	4.25	4.30	V
			$T_A = 25^\circ\text{C}$	4.225	4.25	4.285	
		UCC3952A-3		4.25	4.30	4.35	V
			$T_A = 25^\circ\text{C}$	4.275	4.30	4.335	
		UCC3952A-4		4.30	4.35	4.40	V
			$T_A = 25^\circ\text{C}$	4.325	4.35	4.385	
V_{OVR}	Overcharge to normal recovery voltage	UCC3952A-1		3.85	3.90	3.95	V
			$T_A = 25^\circ\text{C}$	3.87	3.90	3.94	
		UCC3952A-2		3.90	3.95	4.00	V
			$T_A = 25^\circ\text{C}$	3.92	3.95	3.99	
		UCC3952A-3		3.95	4.00	4.05	V
			$T_A = 25^\circ\text{C}$	3.97	4.00	4.04	
		UCC3952A-4		4.00	4.05	4.10	V
			$T_A = 25^\circ\text{C}$	4.02	4.05	4.09	
V_{UV}	Normal to undercharge			2.25	2.35	2.45	V
			$T_A = 25^\circ\text{C}$	2.26	2.35	2.44	
V_{UVR}	Undercharge to normal recovery			2.55	2.65	2.75	V
			$T_A = 25^\circ\text{C}$	2.57	2.65	2.73	
t_{dOD}	Overdischarge delay time			10	25	40	ms
			$T_A = 25^\circ\text{C}$	13.5	25	36	
t_{dOV}	Overvoltage delay time			1.0	1.75	2.5	s
			$T_A = 25^\circ\text{C}$	1.15	1.75	2.3	

short circuit protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS	
I_{THLD}	Discharge current limit	PACK+ = 3.7 V		3.5	5	6.5	A
		PACK+ = 3.7 V, $T_A = 25^\circ\text{C}$		3.8	5	6.3	
t_{dDLY}	Discharge current delay	PACK+ = 3.7 V, $I_I = 6.5 \text{ A}$		1	2	3.0	ms
		PACK+ = 3.7 V, $I_I = 6.5 \text{ A}, T_A = 25^\circ\text{C}$		1.05	2	2.9	
R_{RESET}	Discharge current reset resistance	PACK+ = 3.7 V		7.5			$\text{M}\Omega$
		PACK+ = 3.7 V, $T_A = 25^\circ\text{C}$		7.4			

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electrical characteristics, $T_A = -20^\circ\text{C}$ to 70°C , all voltages are with respect to BNEG (unless otherwise stated) (continued)

bias

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	$V_{UV} < V_{PACK} < V_{OV}$		5	8	μA
		$V_{UV} < V_{PACK} < V_{OV}$, $T_A = 25^\circ\text{C}$		5	7.5	
I_{DDov}	Operating supply current in overvoltage	$V_{OV} < V_{PACK}$		11	24	μA
		$V_{(OV)} < V_{(PACK)}$, $T_A = 25^\circ\text{C}$		11	22	
I_{SD}	Shutdown current	$V_{(PACK)} = 2.0 \text{ V}$			2.5	μA
		$V_{(PACK)} = 2.0 \text{ V}$, $T_A = 25^\circ\text{C}$			2.25	
V_{min}	Minimum cell voltage when all circuits are fully functional				1.7	V

FET switch

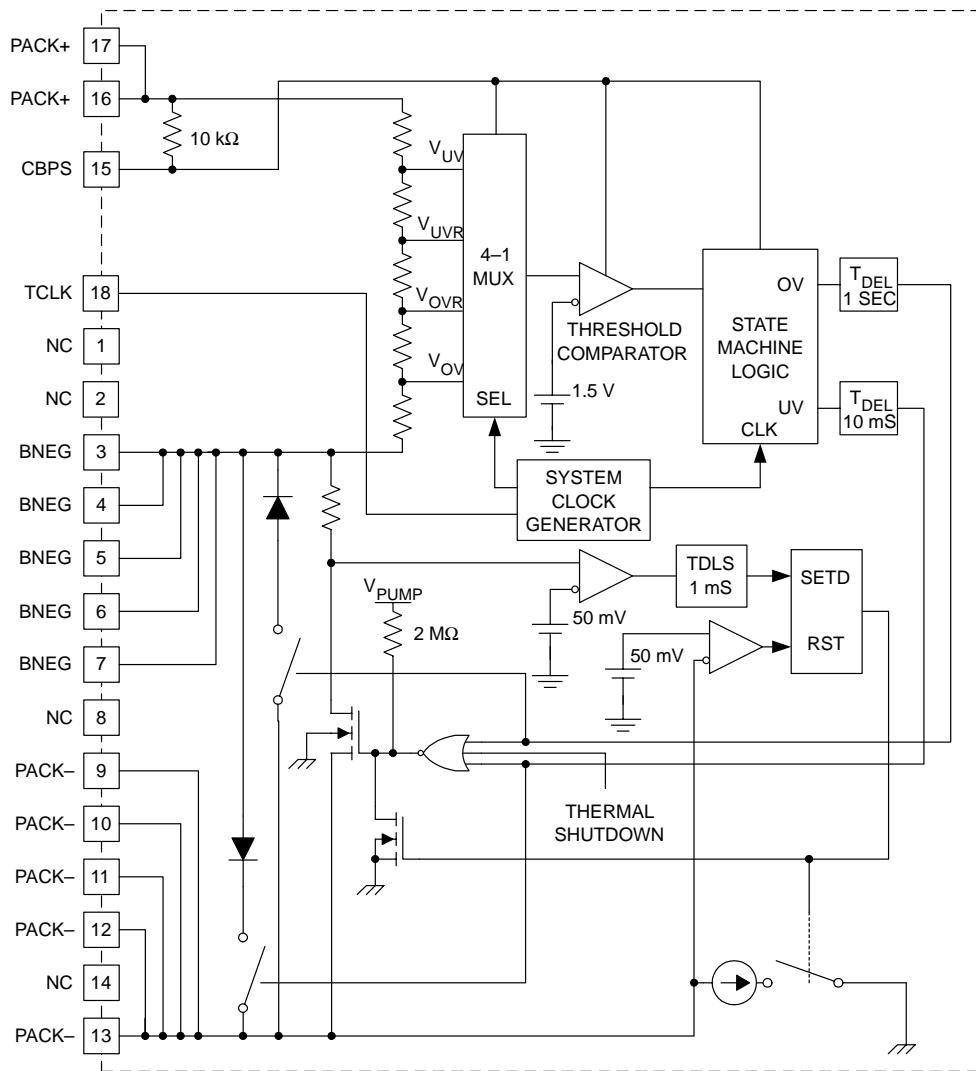
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{PACK-}	Voltage at PACK–	$V_{PACK} > V_{OV}$, $1 \text{ mA} < I_{SWITCH} < 2 \text{ A}$, Battery overcharged state switch permits discharge current only.		100	400	mV
		$V_{PACK} > V_{OV}$, $1 \text{ mA} < I_{SWITCH} < 2 \text{ A}$, Battery overcharged state switch permits discharge current only, $T_A = 25^\circ\text{C}$		100	350	mV
	Series resistance of the device	$PACK+ = 2.5 \text{ V}$, $-2 \text{ mA} < I_{SWITCH} < -1 \text{ A}$, Battery overdischarged state switch permits charge current only.	-600	-100		mV
		$PACK+ = 2.5 \text{ V}$, $-2 \text{ mA} < I_{SWITCH} < -1 \text{ A}$, Battery overdischarged state switch permits charge current only, $T_A = 25^\circ\text{C}$	-540	-100		mV
R_{ON}	Series resistance of the device	$PACK+ = 2.5 \text{ V}$, In normal mode (when not in OV or UV). This value includes package and bondwire resistance.		60	80	$\text{m}\Omega$
		$PACK+ = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$ In normal mode (when not in OV or UV). This value includes package and bondwire resistance.		60	70	$\text{m}\Omega$

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{(SD)}$		Thermal shutdown temperature (see Note 2)			135	$^\circ\text{C}$

NOTE 2: This parameter is ensured by design and is not production tested.

APPLICATION INFORMATION



UDG-98205

Figure 1. Detailed Block Diagram

UCC3952A-1, UCC3952A-2, UCC3952A-3, UCC3952A-4 SINGLE-CELL LITHIUM-ION BATTERY PROTECTION IC

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pin descriptions

BNEG

Connect the negative terminal of the battery to this pin.

PACK+

Connect to the positive terminal of the battery. This pin is available to the user.

CBPS

This power supply bypass pin is connected to PACK+ through an internal 3-k Ω resistor. An external 0.1- μ F capacitor must be connected between this pin and BNEG.

PACK-

The negative terminal of the battery pack (negative terminal available to the user). The internal FET switch connects this terminal to the BNEG terminal to give the battery pack user appropriate access to the battery. In an overcharged state, only discharge current is permitted. In an overdischarged state, only charge current is permitted.

TCLK

Production test mode pin. This pin is used to provide a high-frequency clock to the IC during production testing. In an application, this pin is left unconnected or tied to BNEG.

APPLICATION INFORMATION

battery voltage monitoring

The battery cell voltage is sampled by connecting a resistor divider across it and comparing the resulting voltage to a precision internal reference voltage. Under normal conditions (cell voltage is below the overvoltage threshold and above the undervoltage threshold), the UCC3952A consumes less than 8 μ A of current and the internal MOSFET is fully turned on with the aid of a charge pump.

When the cell voltage falls below the undervoltage threshold for two consecutive samples, the IC disconnects the load from the battery pack and enters a super-low-power mode. The pack remains in this state until it detects the application of a charger, at which point charging is enabled. The requirement of two consecutive readings below the undervoltage threshold filters out momentary drops in cell voltage due to load transients, preventing nuisance trips.

If the cell voltage exceeds the overvoltage threshold for the overcharge delay time, charging is disabled; however, discharge current is still allowed. This feature of the IC is explained further in the *controlled charge/discharge mode* section of this document.

overcurrent monitoring and protection

Discharge current is continuously monitored via an internal sense resistor. In the event of excessive current, an overcurrent condition is declared if the high current persists for t_{dDLY} . This delay allows for charging of the system bypass capacitors without tripping the overcurrent protection. A 0.1- μ F capacitor on the CBPS pin provides momentary holdup for the IC to assure proper operation in the event that a hard short suddenly pulls the cell voltage below the minimum operating voltage.

Once the overcurrent condition has been declared, the internal MOSFET turns off. To return the device to normal operation, the UCC3952A needs to have a load impedance greater than 7.5 M Ω placed across PACK+ to PACK-. This typically can be achieved by removing the battery pack from the system. At this point, the pack returns to its normal state of operation.

controlled charge/discharge mode

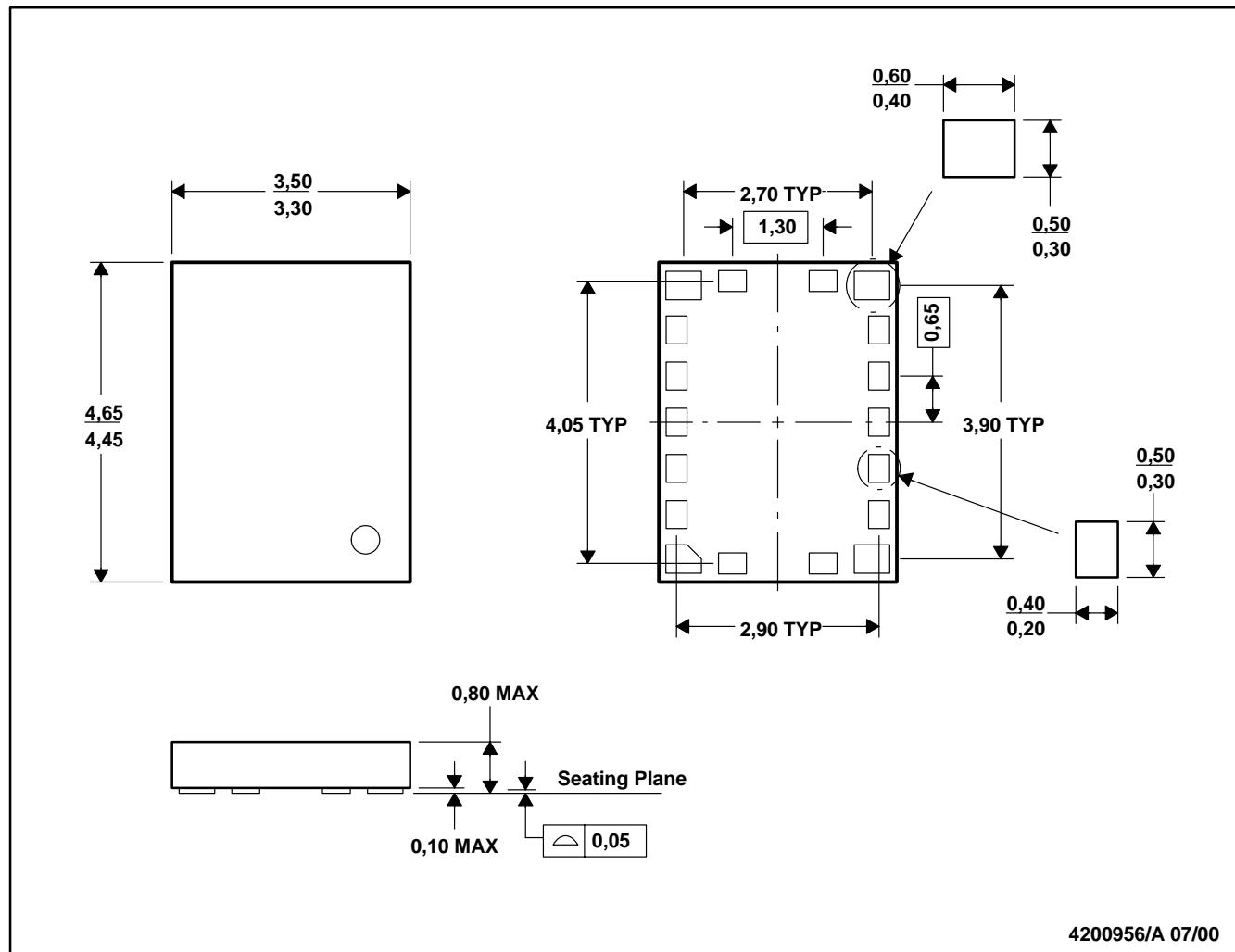
When the chip senses an overvoltage condition, it prevents any additional charging, but allows discharge. This is accomplished by activating a linear control loop, which controls the gate of the MOSFET based on the differential voltage across its drain-to-source terminals. The linear loop attempts to regulate the differential voltage across the MOSFET to 100 mV. When a light load is applied to the part, the loop adjusts the impedance of the MOSFET to maintain 100 mV across it. As the load increases, the impedance of the MOSFET is decreased to maintain the 100-mV control. At heavy loads (still below the overcurrent limit), the loop does not maintain regulation and drives the gate of the MOSFET to the battery voltage (not the charge-pump output voltage). The MOSFET $R_{DS(on)}$ in the overvoltage state is higher than $R_{DS(on)}$ during normal operation. The voltage drop (and associated power loss) across the internal MOSFET in this mode of operation is still significantly lower than the typical solution of two external back-to-back MOSFETs, where the body diode is conducting.

When the chip senses an undervoltage condition, it disconnects the load from the battery pack and shuts itself down to minimize current drain from the battery. Several circuits remain powered and detect placement of the battery pack into a charger. Once the charger presence is detected, the linear loop is activated and the chip allows charging current into the battery. This linear control mode of operation is in effect until the battery voltage reaches a level of V_{UVR} , at which time normal operation is resumed.

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GSH (R-PLGA-N18) PLASTIC LAND GRID ARRAY



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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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