

DATA SHEET

BF1202; BF1202R; BF1202WR N-channel dual-gate PoLo MOS-FETs

Product specification
Supersedes data of 2000 Mar 29

2010 Sep 16



N-channel dual-gate PoLo MOS-FETs BF1202; BF1202R; BF1202WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

- VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

DESCRIPTION

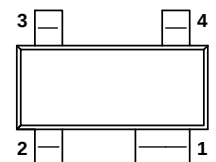
Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1202, BF1202R and BF1202WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Marking code legend:

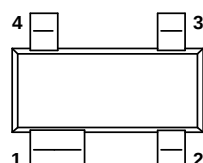
- * = - : made in Hong Kong
- * = p : made in Hong Kong
- * = t : made in Malaysia



Top view MSB035

BF1202R marking code: LE*

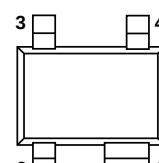
Fig.2 Simplified outline (SOT143R).



Top view MSB014

BF1202 marking code: LD*

Fig.1 Simplified outline (SOT143B).



Top view MSB842

BF1202WR marking code: LE*

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$ y_{fs} $	forward transfer admittance		25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1		–	1.7	2.2	pF
C_{rss}	reverse transfer capacitance	$f = 1 \text{ MHz}$	–	15	30	fF
F	noise figure	$f = 800 \text{ MHz}$	–	1.1	1.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	105	–	dB μ V
T_j	operating junction temperature		–	–	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

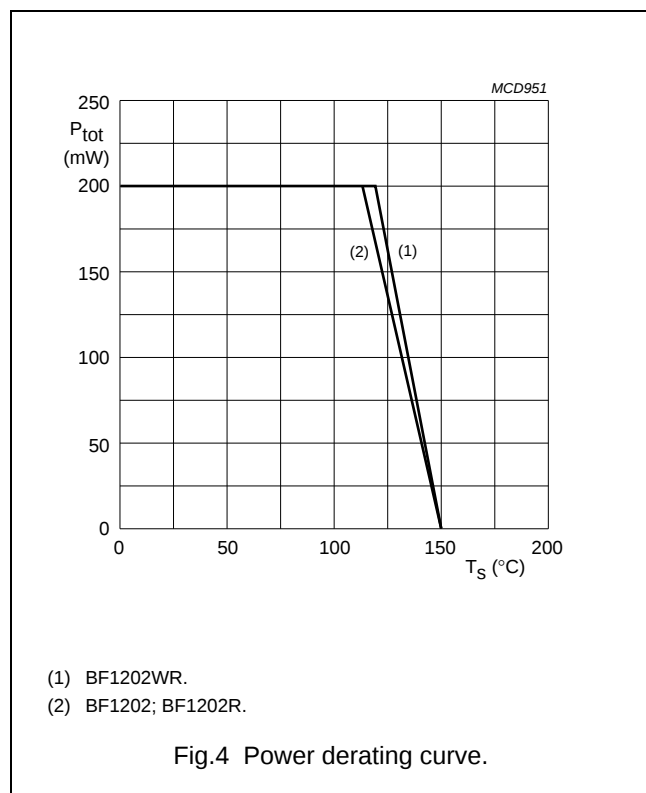
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	10	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation				
	BF1202; BF1202R	$T_s \leq 113\text{ }^{\circ}\text{C}$; note 1	–	200	mW
	BF1202WR	$T_s \leq 119\text{ }^{\circ}\text{C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	150	$^{\circ}\text{C}$

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point		
	BF1202; BF1202R	185	K/W
	BF1202WR	155	K/W



N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 120\text{ k}\Omega$; note 1	8	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\text{ V}$	–	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 12\text{ mA}$; unless otherwise specified.

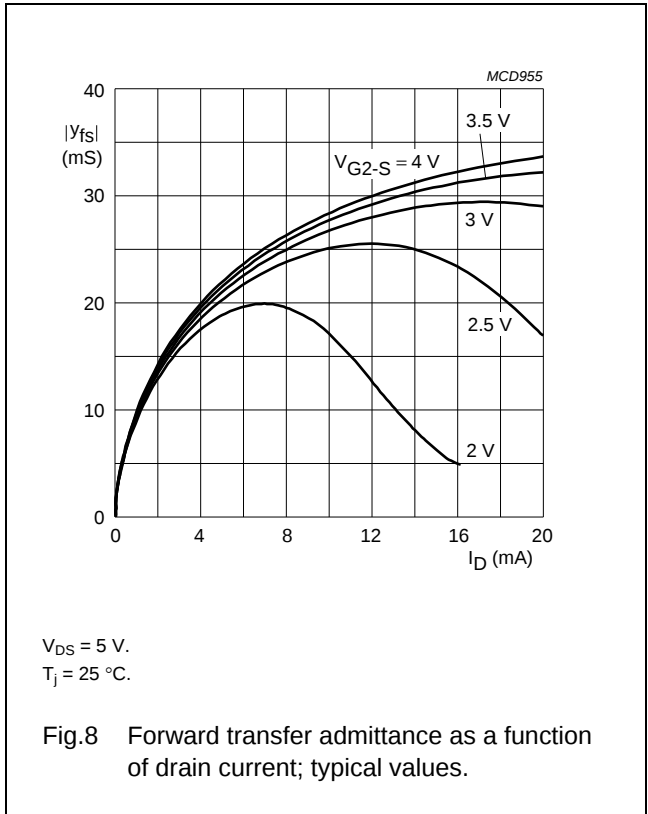
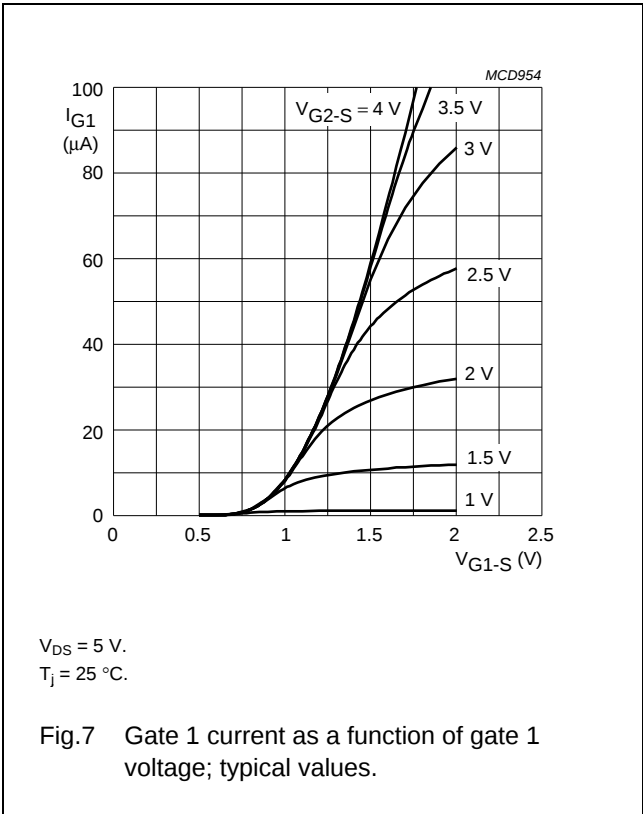
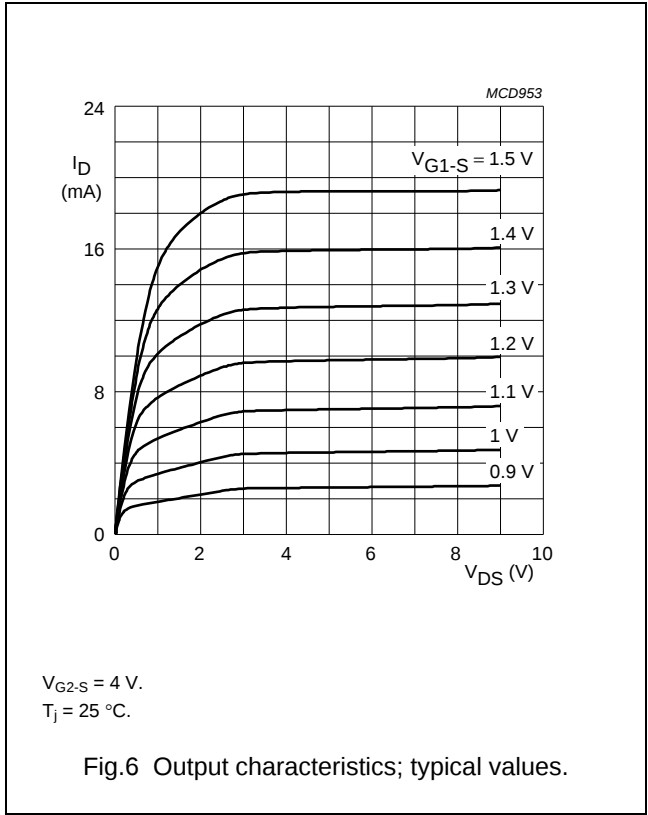
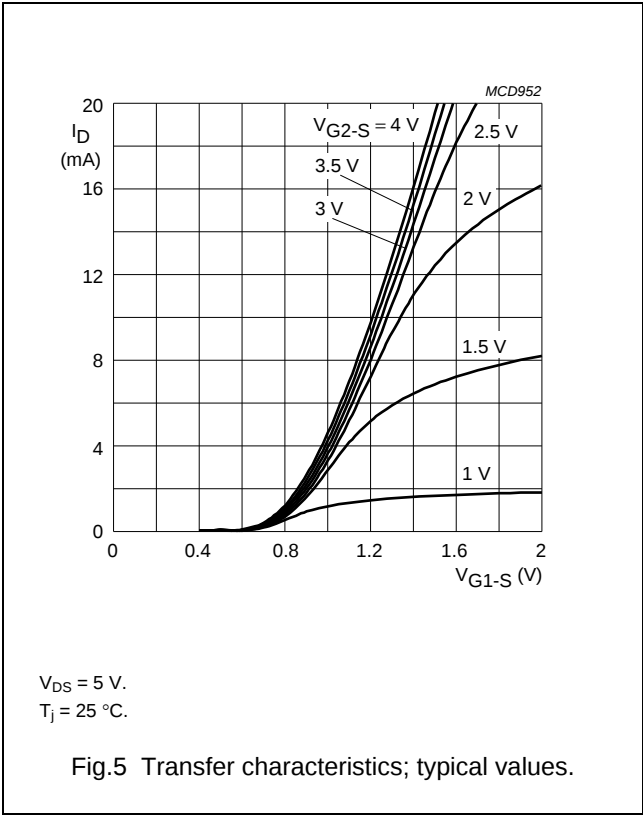
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	9	11	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	0.9	1.5	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.1	1.8	dB
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	34.5	–	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	30.5	–	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	26.5	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1				
		at 0 dB AGC	90	–	–	dB μ V
		at 10 dB AGC	–	92	–	dB μ V
		at 40 dB AGC	100	105	–	dB μ V

Note

1. Measured in Fig.21 test circuit.

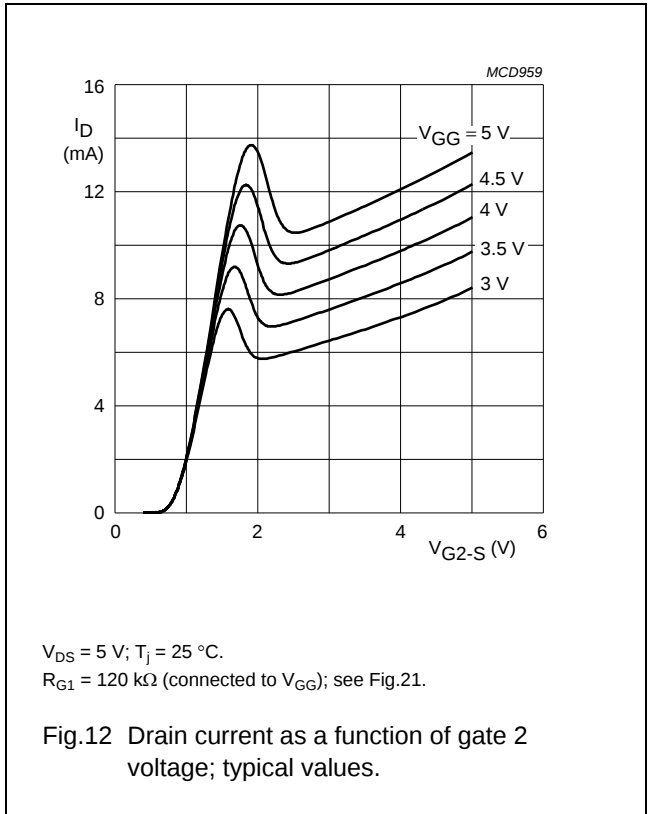
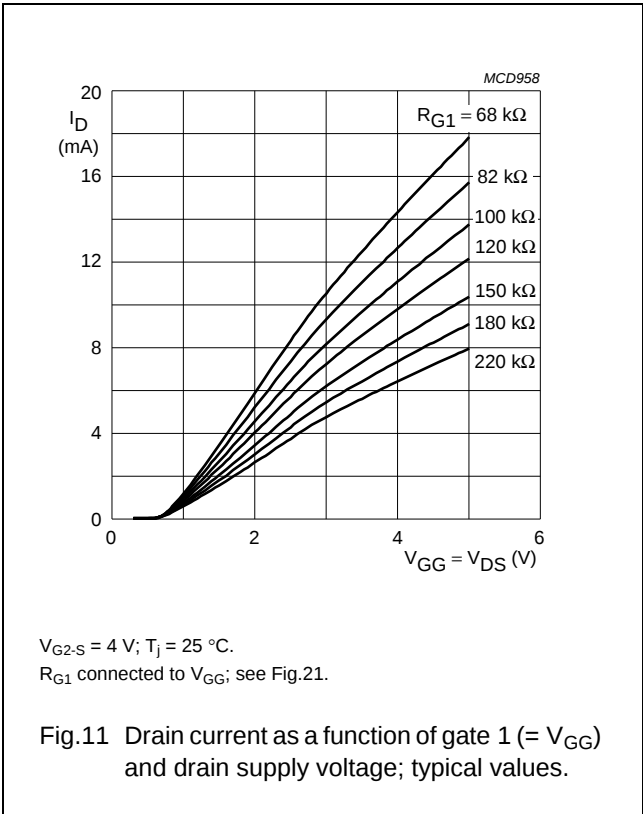
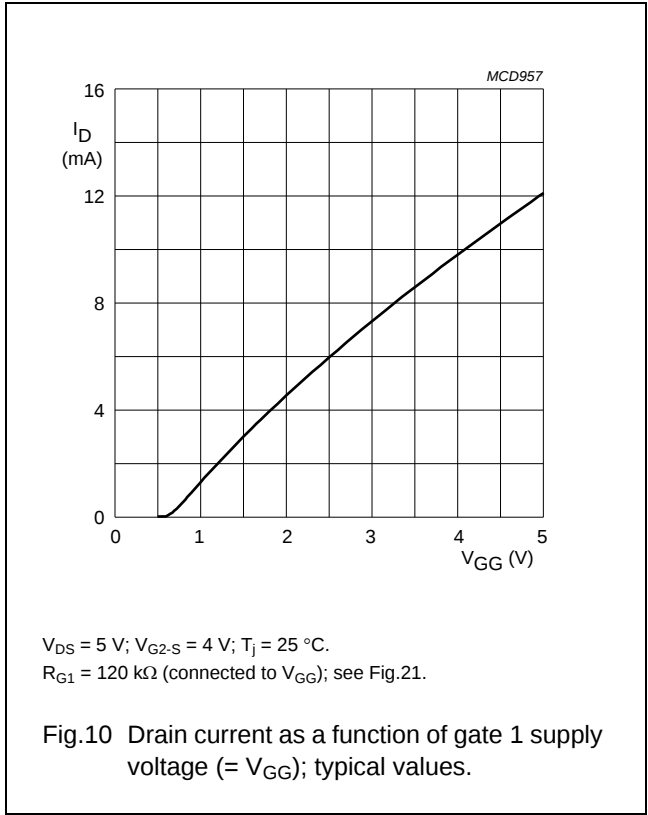
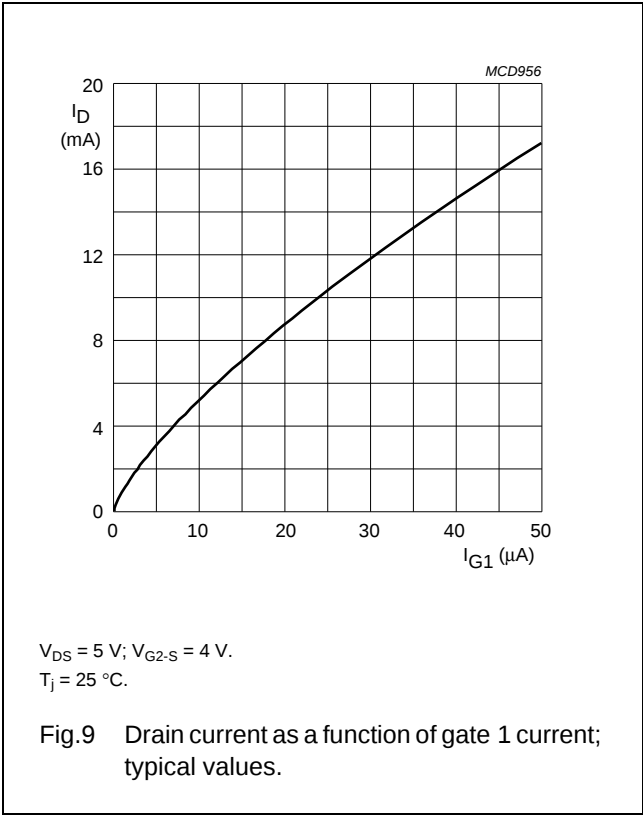
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR



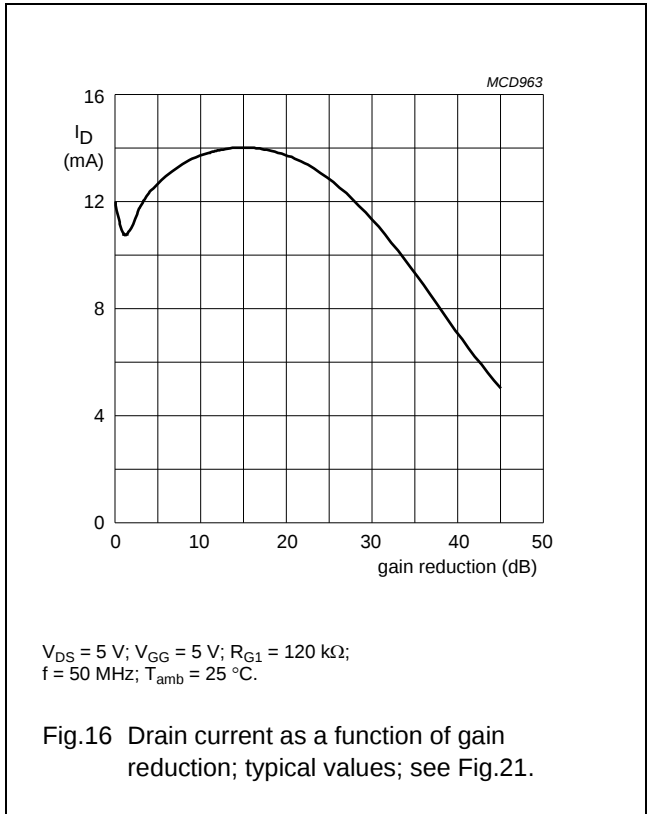
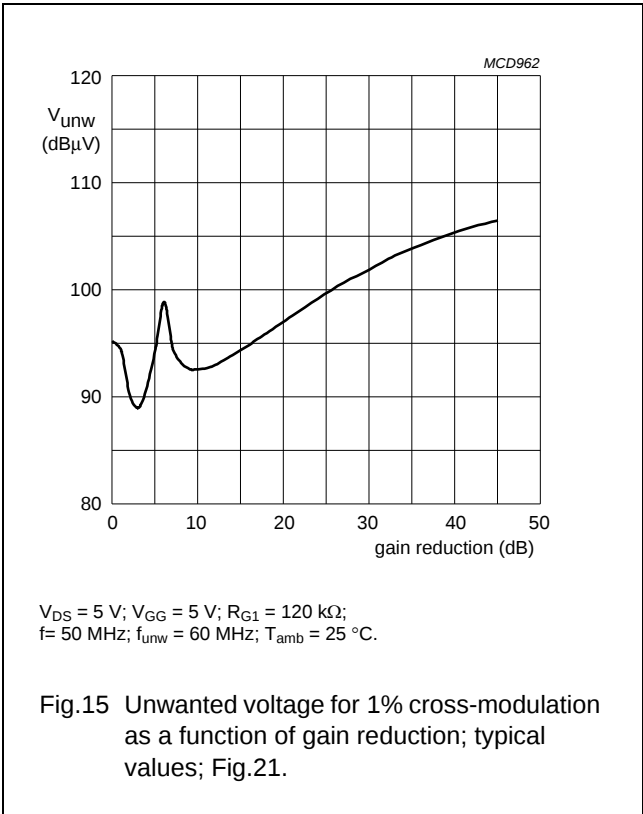
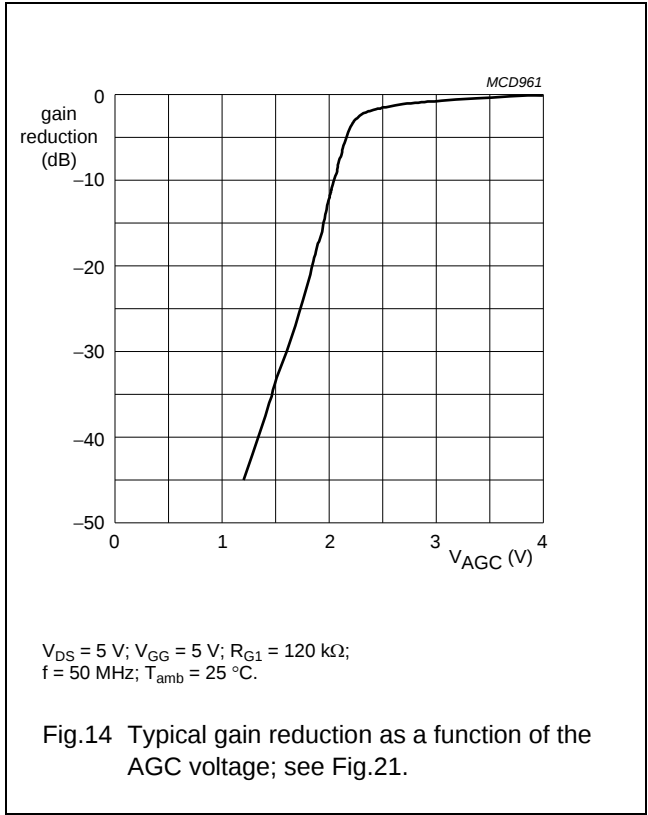
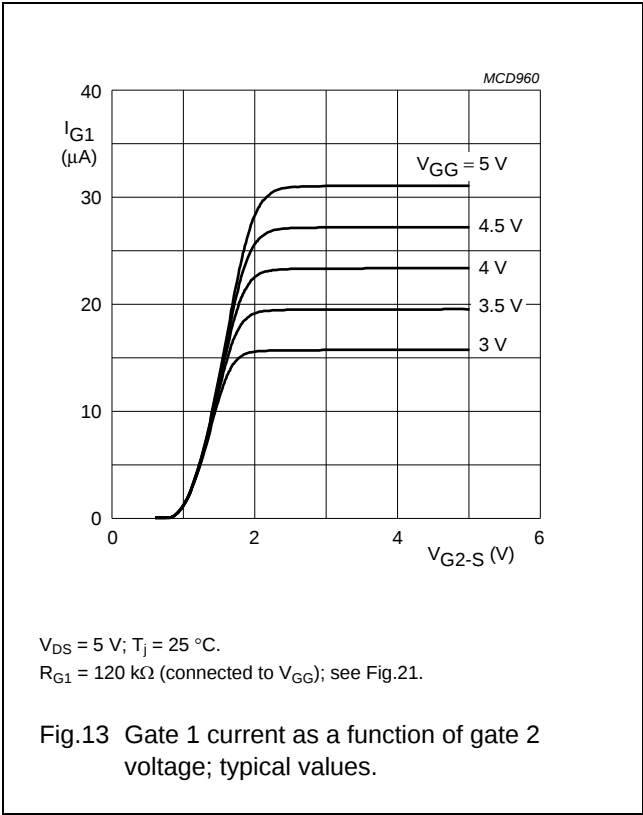
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR



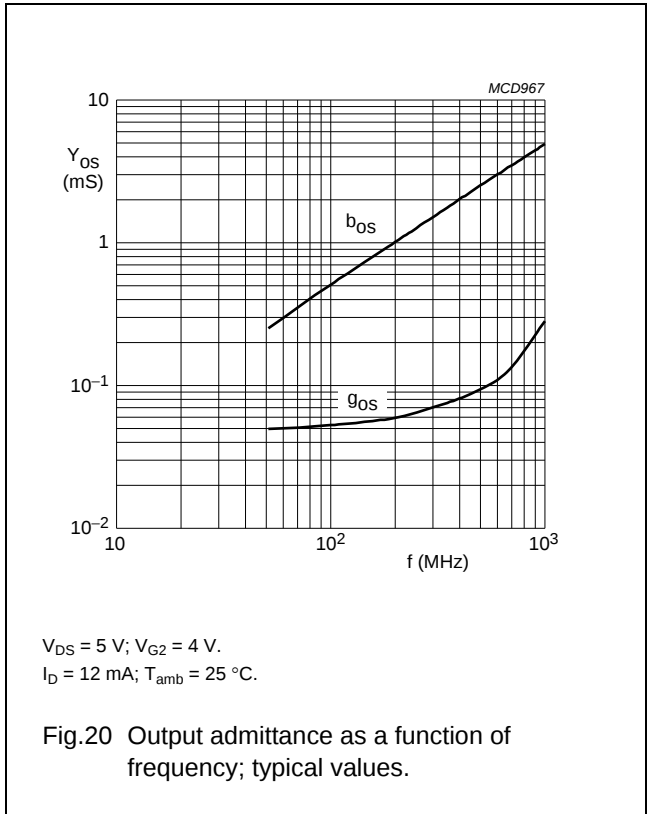
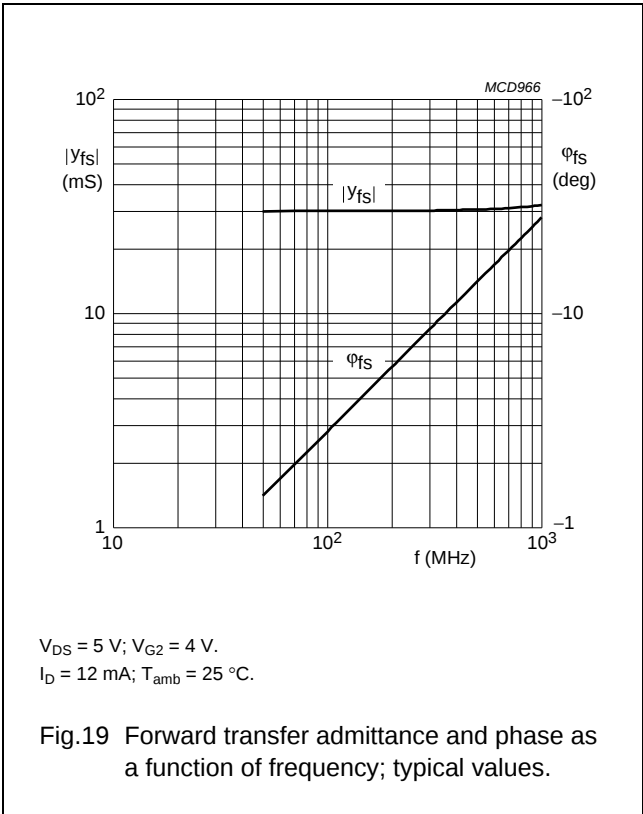
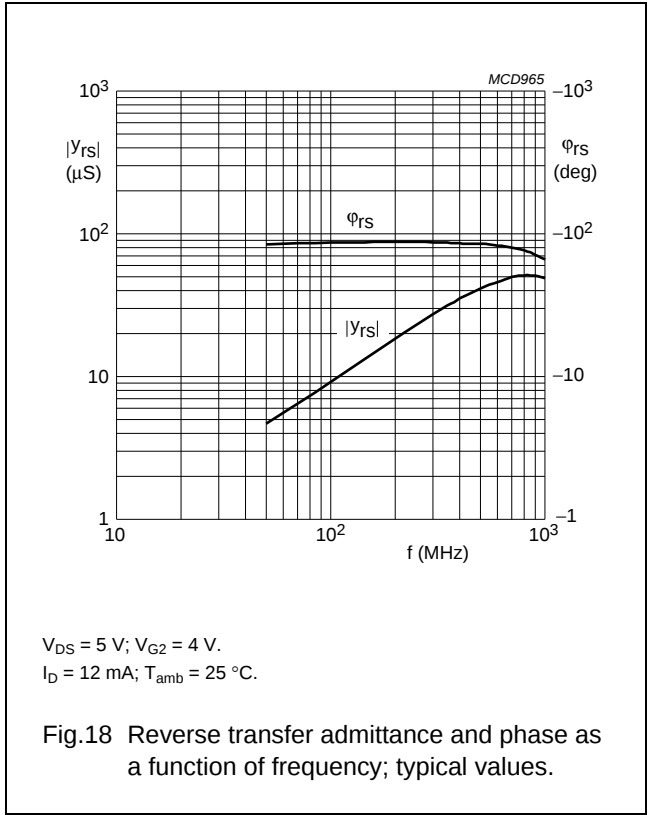
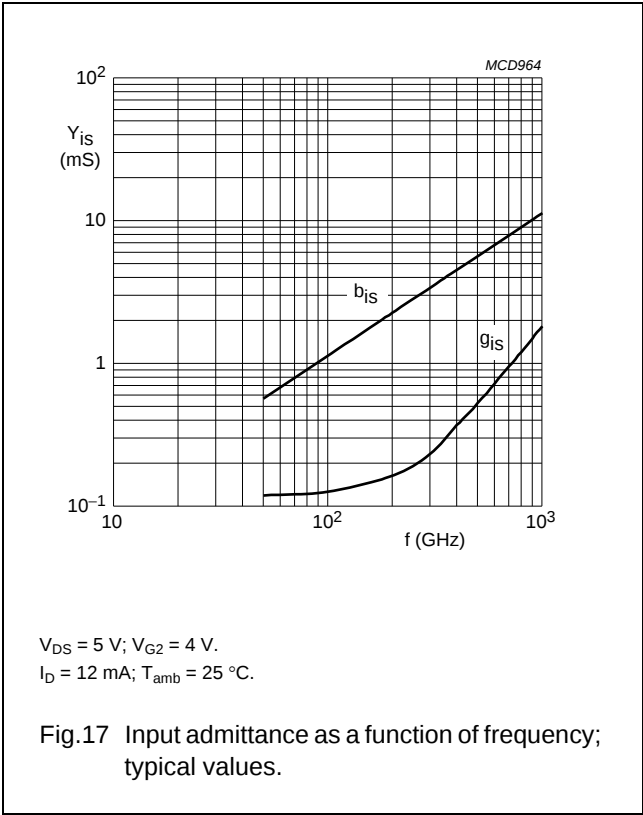
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR



N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR



N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

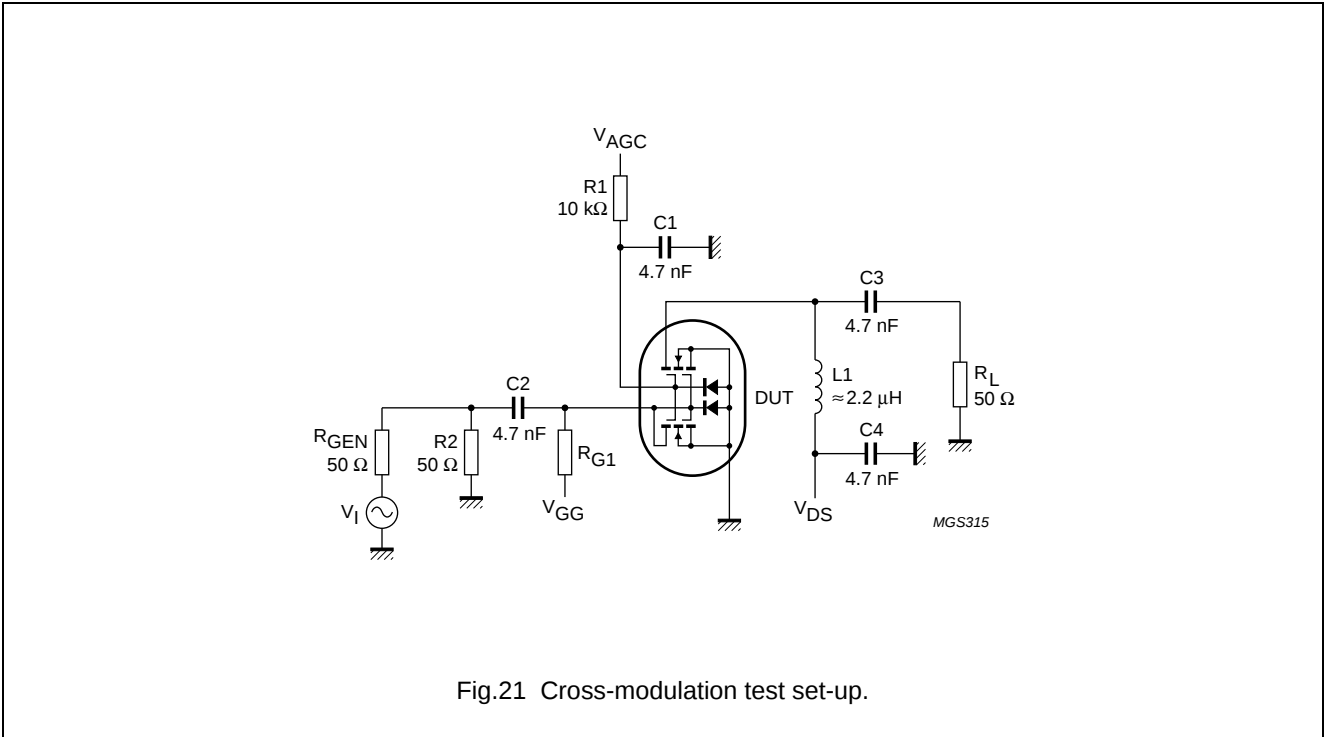


Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	−3.26	2.989	176.2	0.0005	92.6	0.995	−1.50
100	0.988	−6.52	3.017	172.5	0.0009	88.0	0.995	−3.01
200	0.984	−12.99	2.990	165.0	0.0018	82.5	0.994	−5.95
300	0.977	−19.39	2.949	157.6	0.0027	78.2	0.992	−8.86
400	0.965	−25.65	2.913	150.3	0.0036	75.4	0.990	−11.79
500	0.951	−31.76	2.853	143.2	0.0039	71.8	0.988	−14.65
600	0.936	−37.68	2.793	136.3	0.0042	69.9	0.986	−17.41
700	0.919	−43.42	2.727	129.5	0.0044	68.9	0.984	−20.10
800	0.903	−48.94	2.664	123.0	0.0043	68.5	0.980	−22.69
900	0.887	−54.25	2.593	116.7	0.0041	70.7	0.975	−25.27
1000	0.870	−59.34	2.518	110.5	0.0038	72.4	0.970	−27.90

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
400	0.9	0.805	28.5	50
800	1.1	0.725	47.2	40

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B

0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A _{1 max}	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

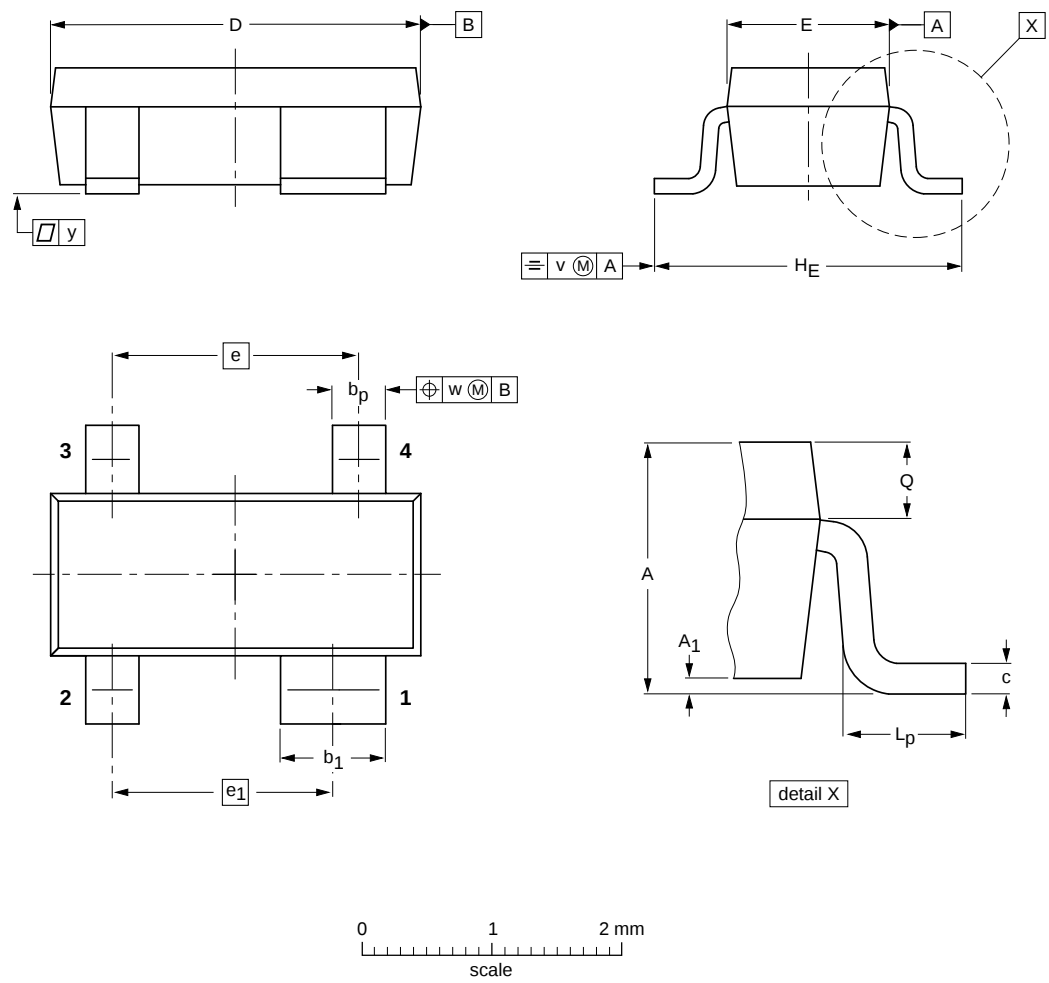
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						04-11-16 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _P	b ₁	c	D	E	e	e ₁	H _E	L _P	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

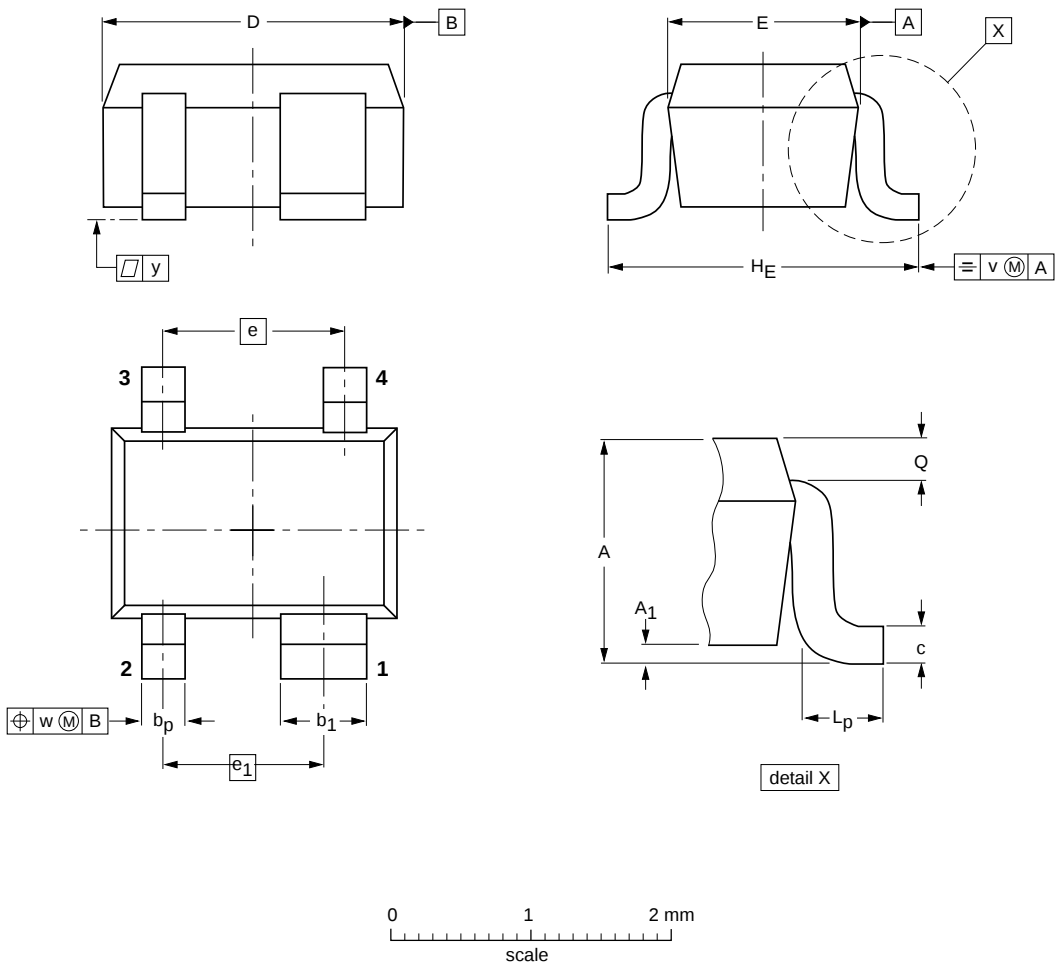
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			04-11-16 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

DISCLAIMERS

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe

property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R; BF1202WR

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

NXP Semiconductors

provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for the marking codes and the package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: salesaddresses@nxp.com

© NXP B.V. 2010

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R77/03/pp15

Date of release: 2010 Sep 16

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP:](#)

[BF1202,215](#) [BF1202R,215](#) [BF1202WR,135](#) [BF1202WR,115](#)