

LCD Module Calibrator

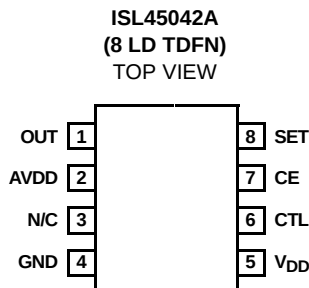
The V_{COM} voltage of an LCD panel needs to be adjusted to remove flicker. The ISL45042A can be used to digitally adjust a panel's V_{COM} voltage by controlling its output sink current. The output of the ISL45042A is connected to an external voltage divider and an external V_{COM} buffer amplifier. In this application, the user can control the V_{COM} voltage with 7-bit accuracy (128 steps). Once the desired V_{COM} setting is obtained, the settings can be stored in the non-volatile EEPROM memory, which would then be automatically recalled during every power-up.

The V_{COM} adjustment and non-volatile memory programming is through a single interface pin (CTL). Once the desired programmed value is obtained, the Counter Enable pin (CE) can be used to prevent further adjustment or programming.

The full-scale sink current of the ISL45042A is set using an external resistor connected to the SET pin. The full-scale sink current determines the lowest voltage of the external voltage divider.

The ISL45042A is available in an 8 Ld 3mmx3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

Pinout



Features

- 128-Step Adjustable Sink Current Output
- 2.6V to 3.6V Logic Supply Voltage Operating Range
- 4.5V to 20V Analog Supply Voltage Range
- Rewritable EEPROM for storing the optimum V_{COM} value
- Output Adjustment Enable/Disable Control
- Output Guaranteed Monotonic Over-Temperature
- Two Pin Adjustment, Programming and Enable
- Ultra Thin 8 Ld 3mmx3mm DFN (0.8mm max)
- Pb-Free (RoHS compliant)

Applications

- LCD Panels

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45042AIRZ	42AZ	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL45042AIRZ-T*	42AZ	-40 to +85	8 Ld 3x3 TDFN Tape and Reel	L8.3x3A
ISL45042AIRZ-TK*	42AZ	-40 to +85	8 Ld 3x3 TDFN Tape and Reel	L8.3x3A

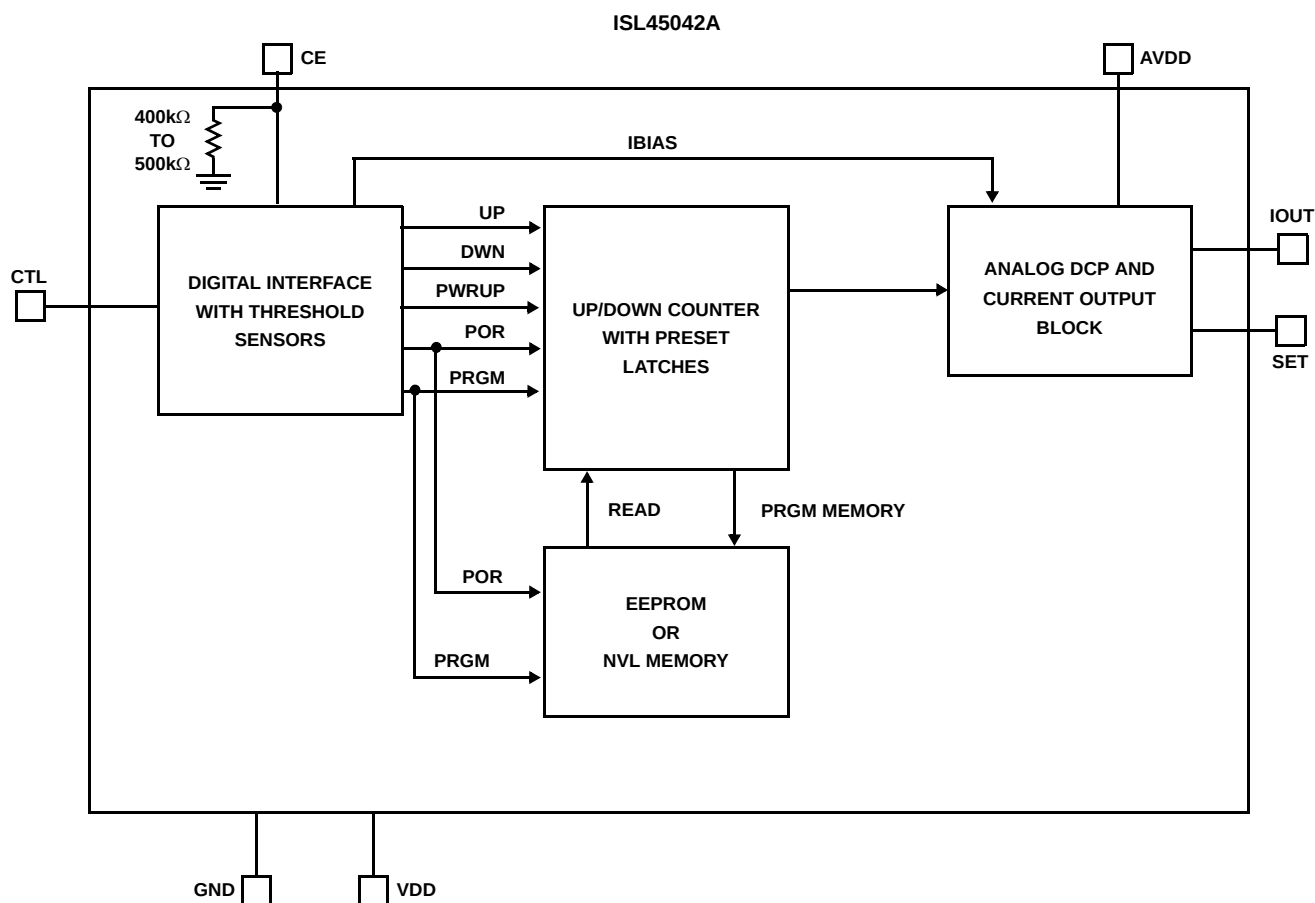
*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	FUNCTION
OUT	Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function in "Pin Descriptions" on page 2 for the maxim adjustable sink current setting.
AVDD	High-Voltage Analog Supply. Connects to top of external resistor divider to determine the V_{COM} voltage. Typically 10V to 20V. Bypass to GND with 0.1 μ F de-coupling capacitor.
N/C	No Connect. Not internally connected.
GND	Ground connection.
V _{DD}	ISL45042A power supply input. Bypass to GND with 0.1 μ F de-coupling capacitor.
CTL	Internal Counter Up/Down Control and Internal EEPROM Programming Control Input. If CE is high, a mid-to-low transition increments the 7-bit counter, raising the DAC setting, increasing the OUT sink current, and lowering the divider voltage at OUT. A mid-to-high transition decrements the 7-bit counter, lowering the DAC setting, decreasing the OUT sink current, and increasing the divider voltage at OUT. Applying 4.9V and above with appropriately arranged timing will overwrite EEPROM with the contents in the 7-bit counter. See EEPROM Programming section in "Electrical Specifications" table on page 4 for details.
CE	Counter Enable Pin. Connect CE to VDD to enable adjustment of the output sink current. Float or connect CE to GND to prevent further adjustment or programming (note: the CE pin has an internal pull-down resistor).
SET	Maximum Sink Current Adjustment Point. Connect a resistor from the SET pin to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.

Block Diagram



Absolute Maximum Ratings

V_{DD} to GND	+4V
Input Voltages to GND	
SET, CE	 -0.3V to +4V
AVDD	 -0.3V to +20V
CTL	 -0.3V to +17V
Output Voltages to GND	
OUT	 -0.3V to +20V
ESD Rating	
Human Body Model	
Device	 2.75kV
CTL to GND (No EEPROM Disruption)	8kV

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package	 47	 12
Moisture Sensitivity (see Technical Brief TB363)		
All Packages	 Level 1	
Maximum Junction Temperature (Plastic Package)	 +150°C	
Maximum Storage Temperature Range	 -65°C to +150°C	
Pb-free Reflow Profile	see link below	
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp	
Erase/Write Cycles	 10,000	
Data Retention	 10 years @ +85°C	

Operating Conditions

Temperature Range	
ISL45042AIR	 -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC} , the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications Test Conditions: $V_{DD} = 3V$, $AV_{DD} = 10V$, $OUT = 5V$, $R_{SET} = 24.9k\Omega$; Unless Otherwise Specified.
 Typicals are at $T_A = +25^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
DC CHARACTERISTICS							
V_{DD} Supply Range	V_{DD}	For Programming	0 to 85	3	-	3.6	V
		For Operation	Full	2.6	-	3.6	V
V_{DD} Supply Current	I_{DD}	CE = V_{DD} (Note 7)	Full	-	-	50	μA
		CE = GND	Full	-	-	20	μA
AVDD Supply Range	AVDD		Full	4.5	-	20	V
AVDD Supply Current	IAVDD	(Note 4)	Full	-	-	20	μA
CTL High Voltage	CTL _{IH}	$2.6V < V_{DD} < 3.6V$	Full	$0.7 \cdot V_{DD}$	-	$0.8 \cdot V_{DD}$	V
CTL Low Voltage	CTL _{IL}	$2.6V < V_{DD} < 3.6V$	Full	$0.2 \cdot V_{DD}$	-	$0.3 \cdot V_{DD}$	V
CTL High Rejected Pulse Width	CTL _{IHRPW}		Full	20	-	-	μs
CTL Low Rejected Pulse Width	CTL _{ILRPW}		Full	20	-	-	μs
CTL High Minimum Pulse Width	CTL _{IHMPW}		Full	-	-	200	μs
CTL Low Minimum Pulse Width	CTL _{ILMPW}		Full	-	-	200	μs
CTL Minimum Time Between Counts	CTL _{MTC}		Full	-	-	10	μs
CTL Input Current	ICTL	CTL = GND	Full	-	-	10	μA
		CTL = V_{DD}	Full	-	-	10	μA
CTL Input Capacitance	CTL _{CAP}	(Note 6)	Full	-	10	-	pF
CE Input Low Voltage	CE _{IL}	$2.6V < V_{DD} < 3.6V$	Full	-	-	0.4	V
CE Input High Voltage	CE _{IH}	$2.6V < V_{DD} < 3.6V$	Full	$0.64 \cdot V_{DD}$	-	-	V
CE Minimum Start-Up Time	CE _{ST}	(Note 6)	Full	-	1	-	ms
CTL EEPROM Program Voltage	CTL _{PROM}	$2.6V < V_{DD} < 3.6V$, (Note 3)	Full	4.9	-	15.75	V

Electrical Specifications Test Conditions: $V_{DD} = 3V$, $AV_{DD} = 10V$, $OUT = 5V$, $R_{SET} = 24.9k\Omega$; Unless Otherwise Specified.
Typicals are at $T_A = +25^\circ C$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
CTL EEPROM Programming Signal Time	CTL_{PT}	>4.9V	Full	200	-	-	μs
Programming Time	P_T		Full	-	-	100	ms
SET Voltage Resolution	SET_{VR}	(Note 5)	Full	7	7	7	Bits
SET Differential Nonlinearity	SET_{DN}	Monotonic Over-Temperature	Full	-	-	± 1	LSB
SET Zero-Scale Error	SET_{ZSE}		Full	-	-	± 2	LSB
SET Full-Scale Error	SET_{FSE}		Full	-	-	± 8	LSB
SET Current	$ISET$	Through R_{SET} (Note 8)	Full	-	20	-	μA
SET External Resistance	SET_{ER}	To GND, $AV_{DD} = 20V$	Full	10	-	200	$k\Omega$
		To GND, $AV_{DD} = 4.5V$	Full	2.25	-	45	$k\Omega$
AV_{DD} to SET Voltage Attenuation	AV_{DD} to SET		Full	-	1:20	-	V/V
OUT Settling Time	OUT_{ST}	to ± 0.5 LSB Error Band (Note 6)	Full	-	20	-	μs
OUT Voltage Range	V_{OUT}		Full	$V_{SET} + 0.5V$	-	13	V
OUT Voltage Drift	OUT_{VD}	(Note 6)	25 to 55	-	<10	-	mV

NOTES:

- CTL signal only needs to be greater than 4.9V to program EEPROM.
- Tested at $AV_{DD} = 20V$.
- The Counter value is set to mid-scale ± 4 LSB's in the Production.
- Simulated and Determined via Design and NOT Directly Tested.
- Simulated Maximum Current Draw when Programming EEPROM is 23mA; should be considered when designing Power Supply.
- A Typical Current of 20 μA is Calculated using the $AV_{DD} = 10V$ and $R_{SET} = 24.9k\Omega$. Reference "RSET Resistor" on page 6.
- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

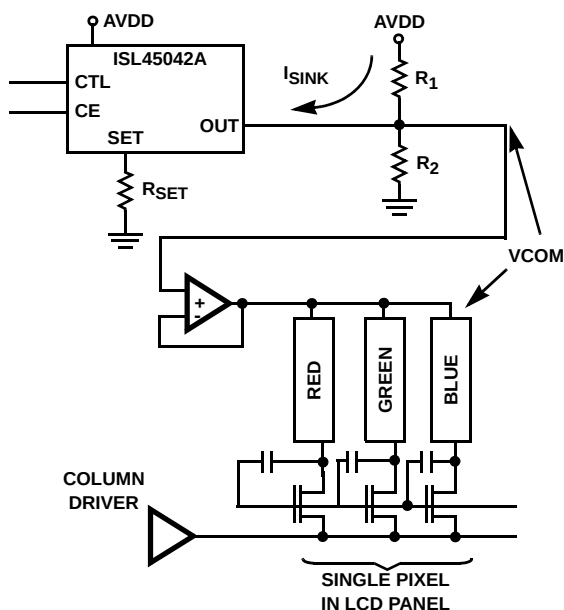


FIGURE 1. VCOM ADJUSTMENT IN AN LCD PANEL

Application Information

The application circuit to adjust the V_{COM} voltage in an LCD panel is shown in Figure 1. The ISL45042A has a 128-step sink current resolution. The output is connected to an external voltage divider, that results in decreasing the output V_{COM} voltage as you increase the ISL45042A sink current.

CTL Pin

The adjustment of the output V_{COM} voltage and the programming of the non-volatile memory are provided through a single pin called CTL when the CE pin is high.

The output V_{COM} voltage is increased with a mid ($V_{DD}/2$) to high transition ($0.8 \cdot V_{DD}$) on the CTL pin. The output V_{COM} voltage is decreased with a mid ($V_{DD}/2$) to low transition ($0.3 \cdot V_{DD}$) on the CTL pin (see Figure 7). Once the minimum or maximum value is reached on the 128 steps, the device will not overflow or underflow beyond that minimum or maximum value.

Programming of the non-volatile memory occurs when the CTL pin exceeds 4.9V. The CTL signal needs to remain above 4.9V for more than 200 μs . The level and timing

needed to program the non-volatile memory is given in Figure 2. It then takes a maximum of 100ms for the programming to be completed inside the device.

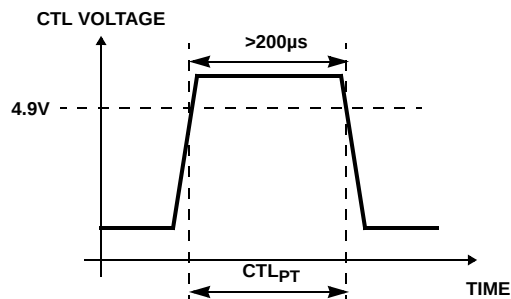


FIGURE 2. EEPROM PROGRAMMING

When the part is programmed, the counter setting is loaded into the non-volatile memory. This value will be loaded from the nonvolatile memory during initial power-up or when the CE pin is pulled low.

Once the programming is completed, it is recommended that the user float the CLT pin. The CTL pin is internally tied to a resistor network connected to ground. If left floating, the voltage at the CTL pin will equal $V_{DD}/2$. Under these conditions, no additional pulses will be seen by the Up/Down counter via the CTL pin. To prevent further programming, ground the CE pin.

CTL should have a noise filter to reduce bouncing or noise on the input that could cause unwanted counting when the CE pin is high. The board should have an additional ESD protection circuit, with a series $1k\Omega$ resistor and a shunt $0.01\mu F$ capacitor connected on the CTL pin, (see Figure 3).

To avoid unintentional adjustment, the ISL45042A guarantees to reject CTL pulses shorter than $20\mu s$.

During Initial Power-up (only), to avoid the possibility of a false pulse (since the internal comparators come up in an unknown state), the very first CTL pulse is ignored. See Figure 7 for the timing information.

CE Pin

To adjust the output voltage, the CE pin must be pulled high (V_{DD}). The CE pin has an internal pull-down resistor to prevent unwanted reprogramming of the EEPROM. The impedance of this resistor is $400k\Omega$ to $500k\Omega$ (see $R_{INTERNAL}$ in Figure 6).

The CE pin has a Schmitt trigger on the input to prevent false triggering during slow transitions of the CE pin. Transitions of the CE pin are recommended to be less than $10\mu s$.

Replacing Existing Mechanical Potentiometer Circuits

Figure 4 shows the common adjustment mechanical circuits and equivalent replacement with the ISL45042A.

Expected Output Voltage

The ISL45042A provides an output sink current, which lowers the voltage on the external voltage divider (V_{COM} output voltage). Equations 1 and 2 can be used to calculate the output current (I_{OUT}) and output voltage (V_{OUT}) values.

$$I_{OUT} = \frac{\text{Setting}}{128} \times \frac{AV_{DD}}{20(R_{SET})} \quad (\text{EQ. 1})$$

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2} \right) AV_{DD} \left(1 - \frac{\text{Setting}}{128} \times \frac{R_1}{20(R_{SET})} \right) \quad (\text{EQ. 2})$$

NOTE: Where setting is an integer between 1 and 128.

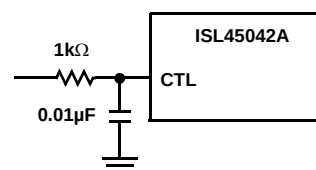


FIGURE 3. EXTERNAL ESD PROTECTION ON CTL PIN

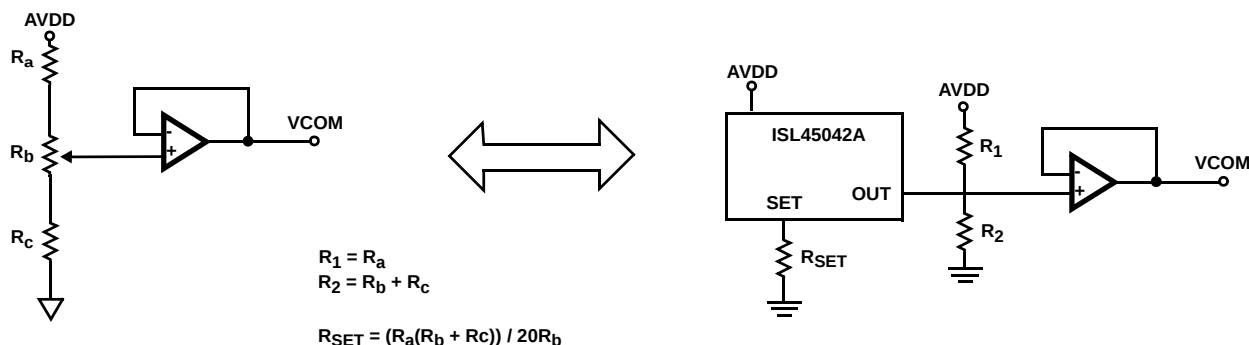


FIGURE 4. EXAMPLE OF THE REPLACEMENT FOR THE MECHANICAL POTENTIOMETER CIRCUIT USING THE ISL45042A

Table 1 gives the calculated value of V_{OUT} for resistors values of: $R_{SET} = 24.9k\Omega$, $R_1 = 200k\Omega$, $R_2 = 243k\Omega$, and $AV_{DD} = 10V$.

TABLE 1. CALCULATED VCOM OUTPUT VOLTAGES

SETTING VALUE	V_{OUT}
1	5.468
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109
90	3.936
100	3.764
110	3.592
128	3.282

R_{SET} Resistor

The external R_{SET} resistor sets the full-scale sink current that determines the lowest voltage of the external voltage divider R_1 and R_2 (see Figure 1). The voltage difference between the V_{OUT} pin and I_{SET} pin (see Figure 5) has to be greater than 1.75V. This will keep the output MOS transistor in the saturation region. Expected current settings and 7-bit accuracy occurs when the output MOS transistor is operating in the saturation region. Figure 5 shows the internal connection for the output MOS transistor. The value of the AV_{DD} supply sets the voltage at the source of the output transistor. This voltage is equal to $(\text{Setting}/128) \times (AV_{DD}/20)$. The I_{SET} current is therefore equal to $(\text{Setting}/128) \times (AV_{DD}/20 \times R_{SET})$. The value of the Drain voltage is found using Equation 2. The values of R_1 and R_2 in Equation 2, should be determined (setting equal to 128) so the minimum value of V_{OUT} is greater than $1.75V + AV_{DD}/20$.

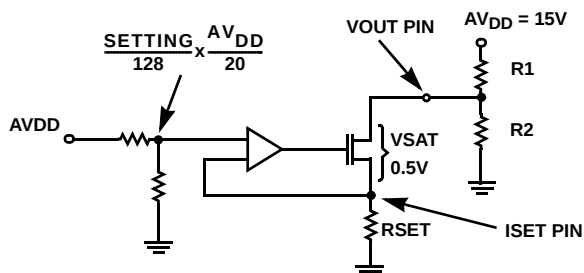


FIGURE 5. OUTPUT CONNECTION CIRCUIT EXAMPLE

Power Supply Sequence

The recommendation for power supply sequence would be to power down the part first (V_{DD} , AV_{DD}), after 100ms if programming has occurred, and then power-down the control power supplies (CTL, CE).

Verifying the Programmed Value

The following sequence can be used to verify the programmed value without having to sequence the V_{DD} supply. To verify the programmed value, follow the following steps. The ISL45042A will read memory contents and be set to that value when the CE pin is grounded.

1. Power-up the ISL45042A.
2. CE pin = V_{DD} .
3. Change counter value with CTL pin to desired value.
4. CTL = more than 4.9V and 200ms. Counter value programmed.
5. Change the counter value with CTL pin to a different value.
6. CE pin = Ground.
7. Check that the output value is the one programmed in Step 4.

Generating V_{DD} and CE supply from a Larger Voltage Source

The CE pin has an internal pull-down resistor (see $R_{INTERNAL}$ in Figure 6). The impedance of this resistor is $400k\Omega$ to $500k\Omega$. If your design is using a resistor divider network to generate the 3.3V supply (for both V_{DD} and CE to enable programming) from a larger voltage source, the $400k\Omega$ (worst case) resistor needs to be taken into account as a parallel resistance when the CE pin is connected to this source. Another design concern is to be able to provide enough supply current during programming. The ISL45042A draws about 2mA during this process. Recommended resistor values are shown in Figure 6. This design will result in an additional 0.83mA quiescent current flowing through resistors R_A and R_B .

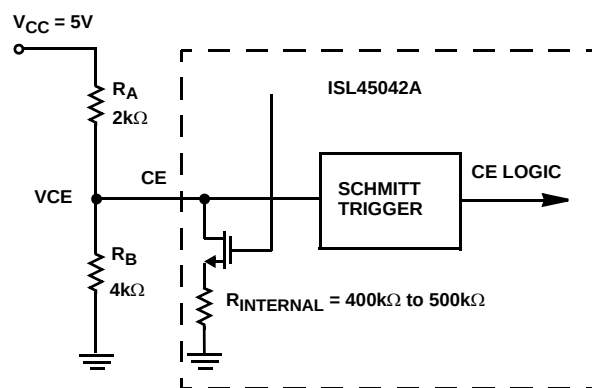


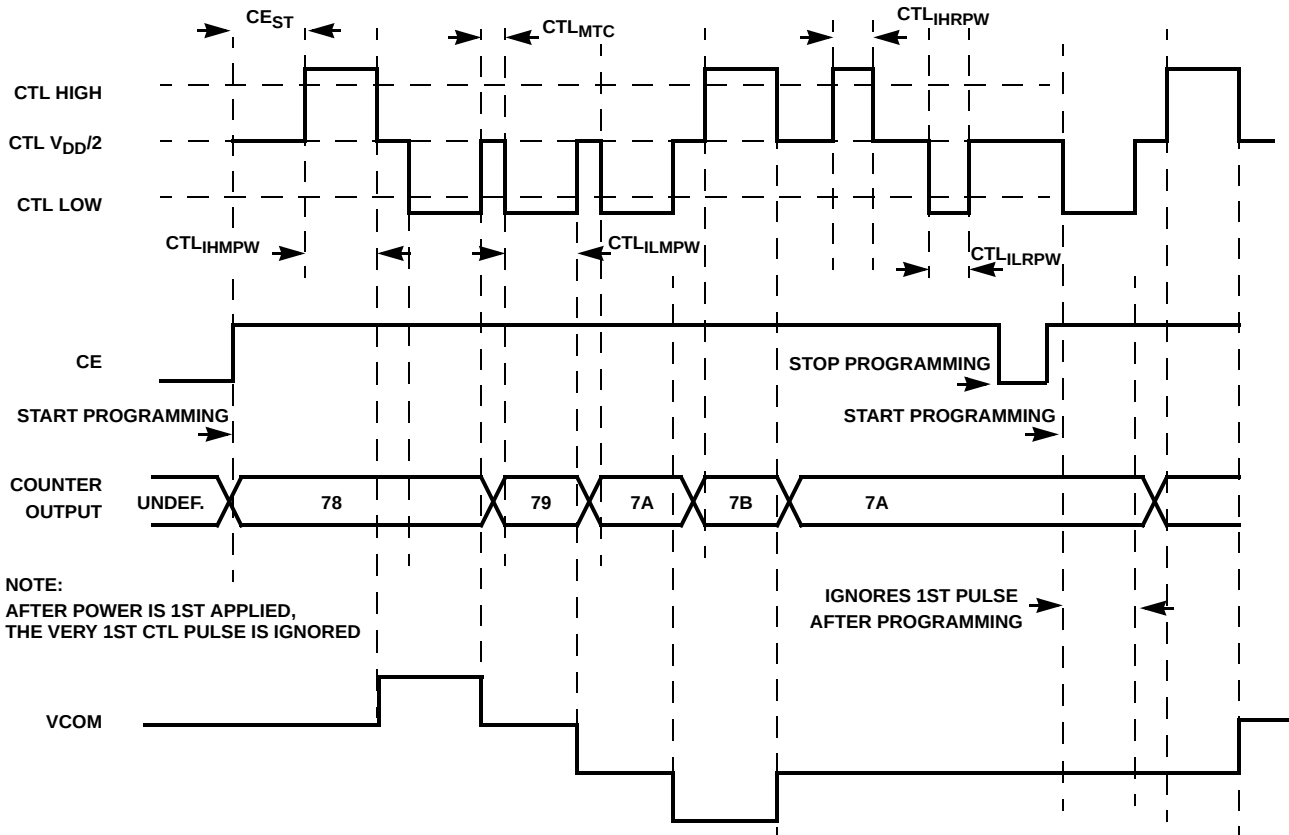
FIGURE 6. APPLICATION GENERATING V_{DD} AND V_{CE} VOLTAGES

ISL45042A Truth Table

The ISL45042A truth table is shown in Table 2. For proper operation the CE should be disabled (pulled low) before powering the device down to assure that the glitches and transients will not cause unwanted EEPROM overwriting.

TABLE 2. TRUTH TABLE

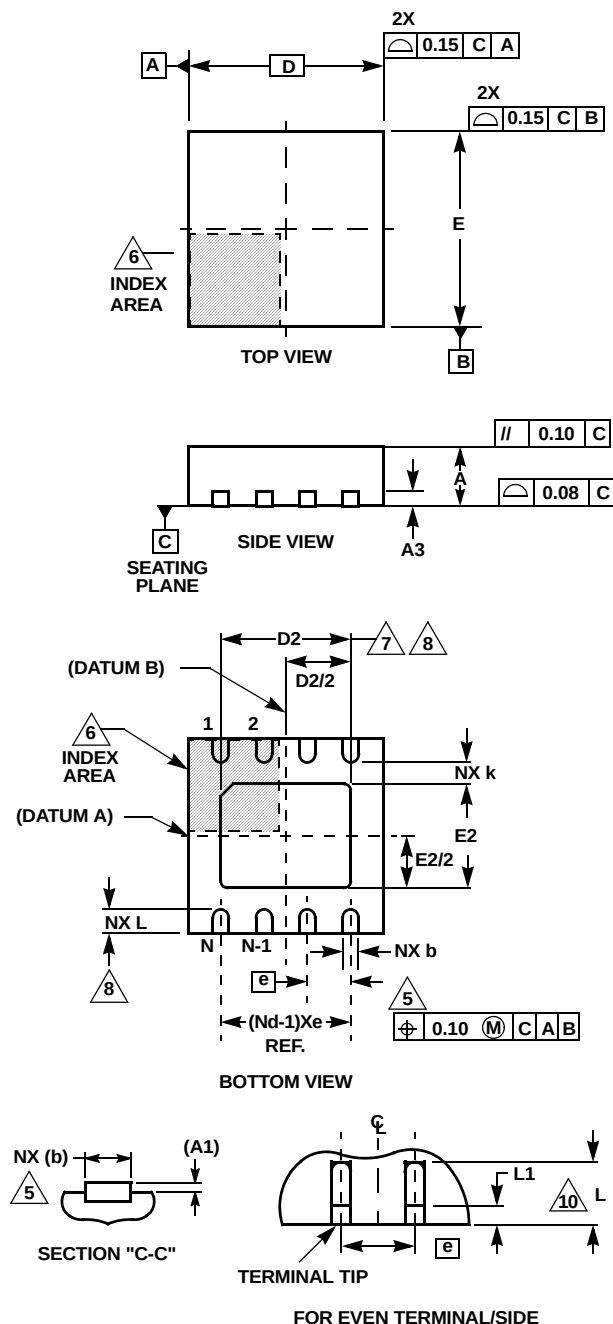
INPUT			OUTPUT		
CTL	CE	VDD	OUT	ICC	MEMORY
Mid to Hi	Hi	VDD	Increment	Normal	X
Mid to Lo	Hi	VDD	Decrement	Normal	X
X	Lo	VDD	No Change	Increased	Read
>4.9V	Hi	VDD	No Change	Increased	Program



THE TIMING DIAGRAM ABOVE SHOWS POST POWER-UP TIMING.

FIGURE 7. ISL45042A TIMING DIAGRAM

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3	0.20 REF			-
b	0.25	0.30	0.35	5, 8
D	3.00 BSC			-
D2	2.20	2.30	2.40	7, 8, 9
E	3.00 BSC			-
E2	1.40	1.50	1.60	7, 8, 9
e	0.65 BSC			-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N	8			2
Nd	4			3

Rev. 3 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the "L" min dimension.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com