High Voltage, Low Noise, Inductorless EL Lamp Driver

Features

- No external components required when using an external EL clock frequency
- EL frequency can be set by an external resistor
- Low Noise
- DC to AC converter
- Drives up to 5.3nF (approx. 1.5in^2 lamp) load
- Output voltage regulation
- Enable function
- EL Lamp dimming

Applications

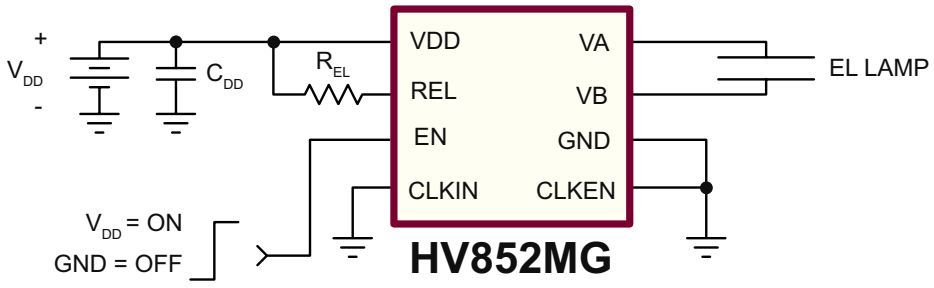
- Cellular phone keypad
- Watches
- Small handheld wireless devices
- MP3 Players

General Description

The Supertex HV852 is a high voltage, low noise, inductorless EL (electroluminescent) lamp driver. It is designed to drive EL lamps of up to 1.5in^2, with capacitive values up to 5.3nF over an input voltage range of 2.4 to 5.0V. The HV852 converts a low voltage DC input to a high voltage AC output across an EL lamp. It uses a charge pump scheme to boost the input voltage eliminating the need for an external inductor, diode, and high voltage capacitor commonly found in conventional topologies.

The charge pump circuit discharges its energy into an EL lamp through a high voltage H-bridge. Once the voltage reaches its regulated limit, it is turned off to conserve power. The EL lamp is then discharged to ground and the H-bridge changes state to allow the charge pump to charge the EL lamp in the opposite direction.

Typical Application Circuit



EL Lamp frequency set by R_{EL}

Ordering Information

Device	Package Options	
	8-Lead MSOP *3.00x3.00mm body* *1.10mm height (max)* *0.65mm pitch*	10-Lead DFN *3.00x3.00mm body* *0.80mm height (max)* *0.50mm pitch*
HV852	HV852MG-G	HV852K7-G

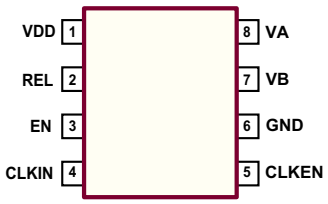
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

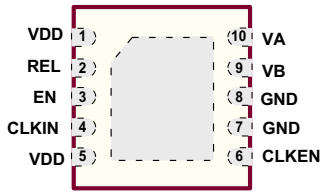
Parameter	Value
V_{DD}, supply voltage	-0.5V to 6.5V
Operating temperature	-25°C to +85°C
Storage temperature	-65°C to +150°C
Power dissipation: 8-Lead MSOP	300mW
Power dissipation: 10-Lead DFN	1.6W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configurations



8-Lead MSOP
(top view)



10-Lead DFN
(top view)

Note:
Pads are at the bottom of the package. Center heat slug is at ground potential.

Product Marking

Top Marking

Bottom Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
____= "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead MSOP (MG)

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead DFN (K7)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Input voltage	2.4	-	5.0	V	---
f_{EL}	EL lamp frequency	50	-	500	Hz	---
C_{load}	EL lamp capacitance	0	-	5.3	nF	---
T_A	Operating temperature	-25	-	+85	°C	---

Electrical Characteristics *(Over recommended operating conditions unless otherwise specified: T_A = 25ºC, V_{DD} = 3.5V)*

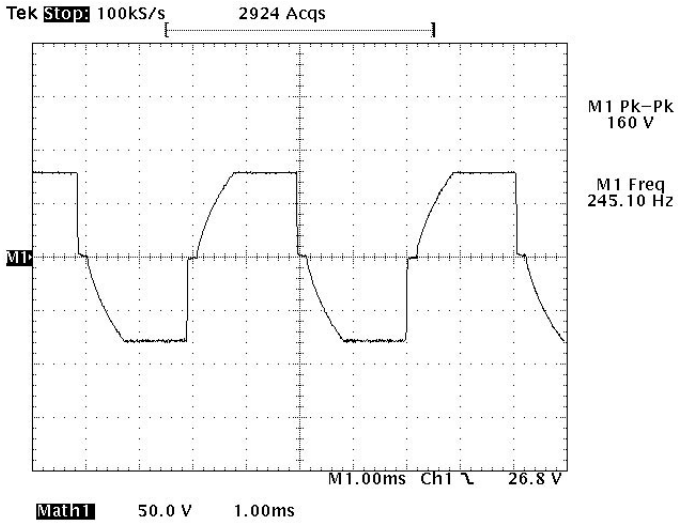
Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{DDQ}	Quiescent current	-	-	200	nA	EN = 0V
V_A or V_B	Peak output voltage	72	82	92	V	No load
V_A-V_B	Peak to peak output voltage	144	164	184	V	
I_{DD}	Operating current	-	15.2	30	mA	See Figure 1, V_{DD} = 3.5V, R_{EL} = 1.5MΩ, Load = 3.3nF+1kΩ
V_A or V_B	Peak output voltage	72	82	92	V	
V_A-V_B	Peak to peak output voltage	144	164	184	V	
f_{EL}	EL lamp frequency	210	250	300	Hz	
t_{rout}	Output voltage rise time	-	640	-	µs	1.0in² lamp, 10 to 90% of final value

Logic Inputs

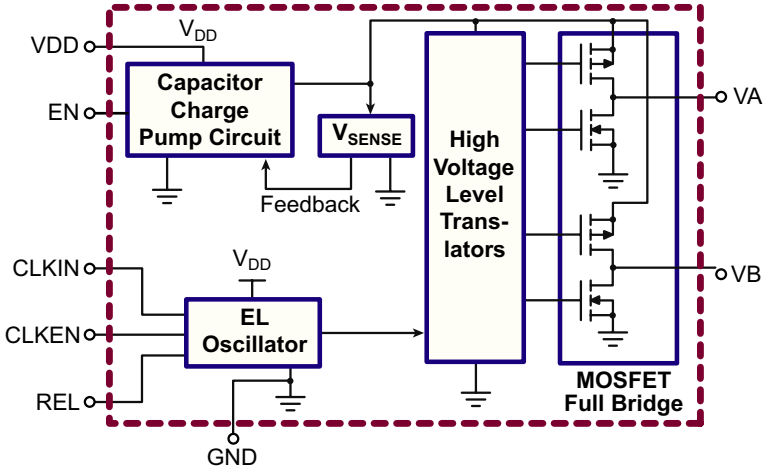
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input logic low voltage	0	-	0.5	V	---
V_{IH}	Input logic high voltage	1.75	-	V_{DD}	V	V_{DD} = 2.4 to 4.3V. T_A = -25 to 85ºC
		2.0	-	V_{DD}	V	4.3 < V_{DD} ≤ 5.0V. T_A = -25 to 85ºC
I_{IL}	Input logic low current	-	-	1.0	µA	V_{IL} = 0V, V_{DD} = 2.4 - 5.0V
I_{IH}	Input logic high current	-	-	1.0	µA	V_{IH} = V_{DD} = 2.4 - 5.0V
t_{rEN}	Enable input rise time (for delay turn on)	0.01	-	10	ms	Using external R-C circuit, see Figure 2
t_{fEN}	Enable input fall time (for delay turn off)	10µ	-	5.0	s	
C_{in}	Logic input capacitance	-	-	10	pF	---

Typical Output Waveform *(refer to Figure 1)*

Test Conditions:
HV852 driving a 1.0in² EL lamp
V_{DD}= 3.6V and R_{EL}= 1.5MΩ,
V_A-V_B waveform



Functional Block Diagram

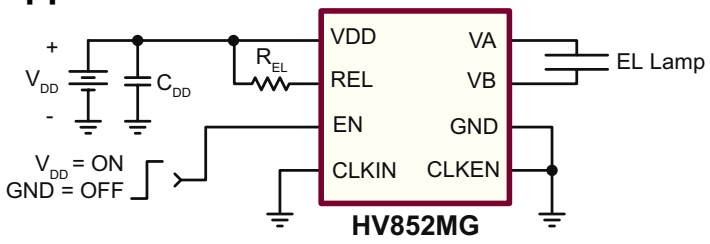


Typical Performance

(The following was the observed performance when driving a 1.0in² green lamp)

Load	R_{EL} (MΩ)	V_{DD} (V)	I_{DD} (mA)	V_A-V_B (V)	f_{EL} (Hz)
3.3nF+1kΩ	1.5	2.4	17.56	154	245
		3.0	17.53	158	
		3.6	17.44	158	
		4.2	17.65	158	
		5.0	18.35	158	

Figure 1: Typical Application



Note:

C_{DD} = 2.2µF, 6.3V ceramic capacitor

Figure 2: Push Button Turn on with Delay Turn off

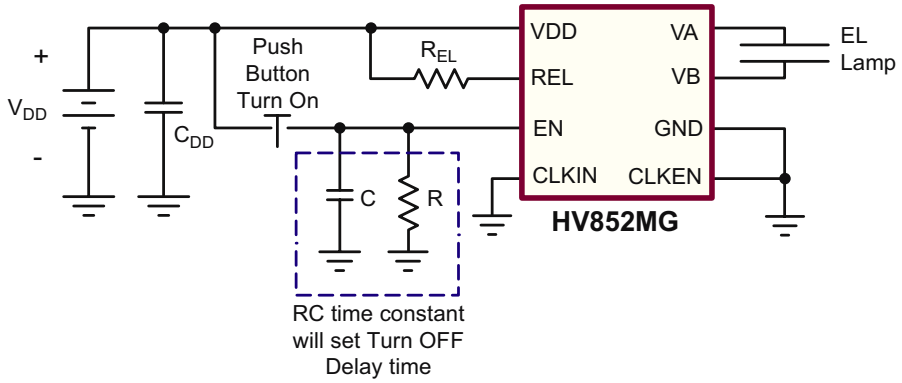
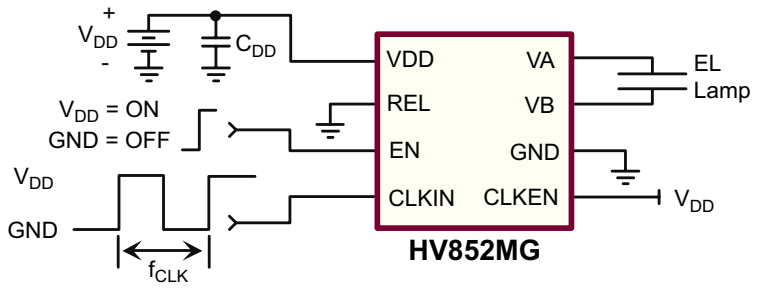


Figure 3: Independent Programmable Output Frequency (f_{EL})



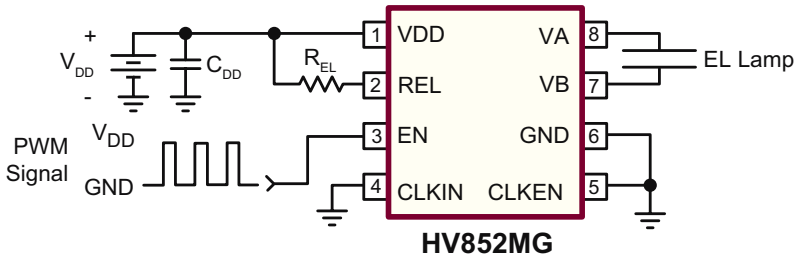
EL Lamp frequency set by an external clock

Note:
$f_{EL} = f_{CLK}/128$

EL Lamp Dimming Using PWM

EL lamp dimming can be achieved by applying a PWM signal to the ENABLE pin. EL Lamp brightness is proportional to the PWM signal duty cycle. This is done by pulse skipping the output pulses. The PWM frequency should be kept below the EL frequency but above 50Hz to avoid flickering.

Figure 4: PWM Dimming Circuit

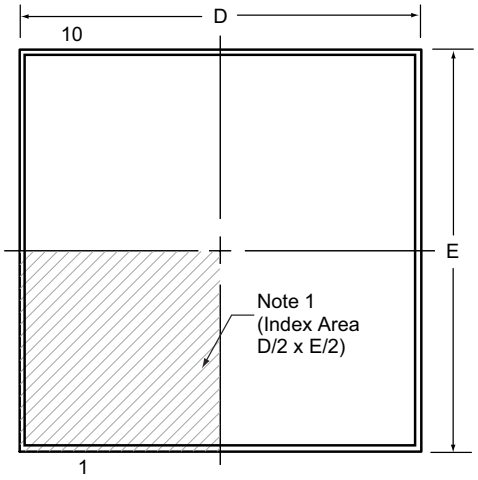


Pin Description

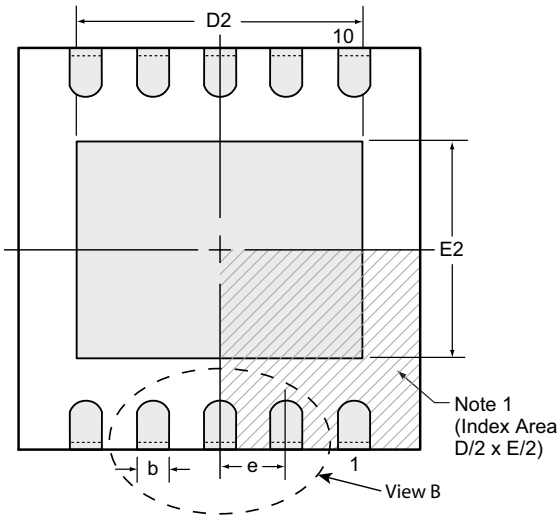
Name	8-Lead MSOP	10-Lead DFN	Description
VDD	1	1, 5	Input supply voltage pin.
REL	2	2	An external resistor to VDD will set the EL lamp frequency. The EL frequency is inversely proportional to the R_{EL} resistor value. A 1.5MΩ resistor would provide a nominal lamp frequency of 250Hz. $f_{EL} = \frac{(1.5M\Omega)\ (250Hz)}{R_{EL}}$ When using an external clock to set the EL lamp frequency, the REL pin should be connected to ground.
EN	3	3	Enable input pin. Logic high will turn the device on. An external R-C circuit can be added for a delayed turn off.
CLKIN	4	4	Logic input pin. An external logic clock applied to this pin can be used to set the EL lamp frequency (see Figure 3). The EL lamp frequency is the external clock frequency divided by 128. This is useful for applications requiring the EL lamp to be synchronized to a system clock. Connect to ground when not in use.
CLKEN	5	6	Logic input pin. Logic high will cause the EL lamp frequency to be set by the CLKIN input. Logic low will cause the EL lamp frequency to be set by the external R_{EL} resistor.
GND	6	7, 8	IC ground pin.
VB	7	9	EL lamp driver output pin. The EL lamp is connected across VA and VB terminals.
VA	8	10	EL lamp driver output pin. The EL lamp is connected across VA and VB terminals.

10-Lead DFN Package Outline (K7)

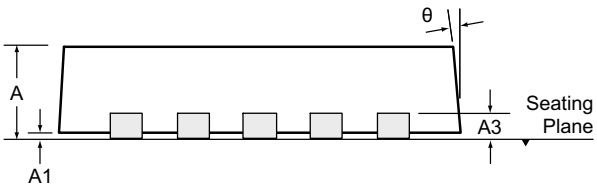
3.00x3.00mm body, 0.80mm height (max), 0.50mm pitch



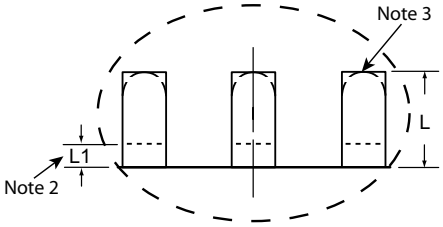
Top View



Bottom View



Side View



View B

Notes:

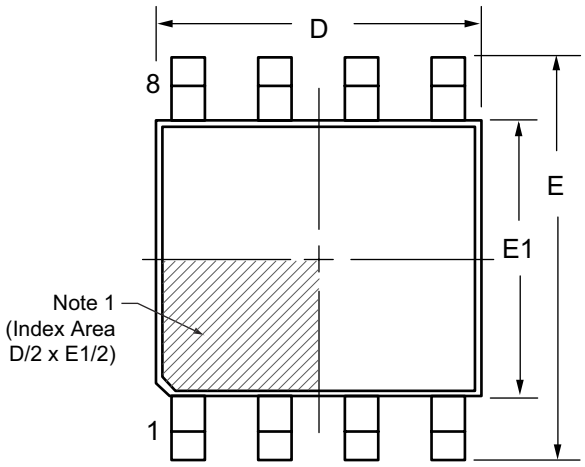
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85*	2.20	2.85*	1.40	0.50 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15*	2.70	3.15*	1.75		0.50	0.15	14°

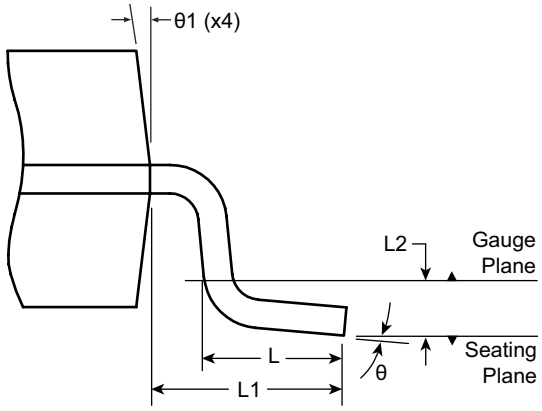
JEDEC Registration MO-229, Variation WEED-5, Issue C, Aug. 2003.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
Supertex Doc.#: *DSPD-10DFNK73X3P050, Version D041309.*

8-Lead MSOP Package Outline (MG)

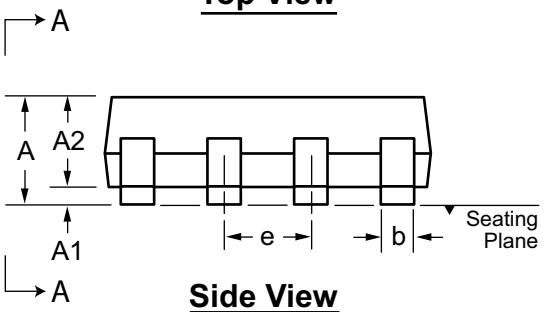
3.00x3.00mm body, 1.10mm height (max), 0.65mm pitch



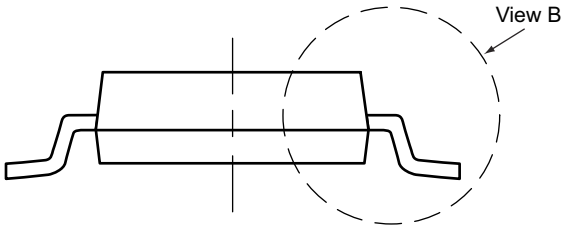
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.22	2.80*	4.65*	2.80*	0.65 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.38	3.20*	5.15*	3.20*		0.80			8°	15°

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8MSOPMG, Version H041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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