

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>. This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/SW201.

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
SW201-803Q	Quad SPST JFET Analog Switch

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T16	16-Lead ceramic dual-in-line package (CERDIP)

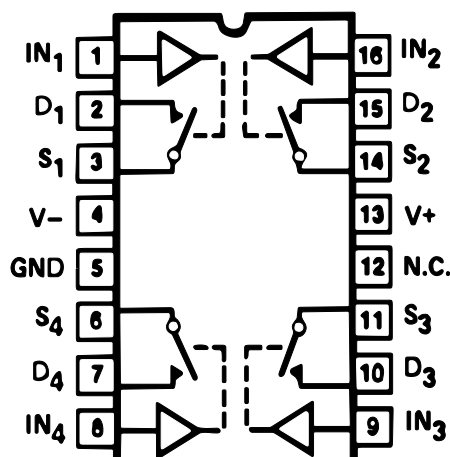


Figure 1 - Terminal connections.

2.1.1 SW201 Logic Table:

Control Logic	
Logic Input	Switch State
0	ON
1	OFF

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range.....	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	900mW
Lead Temperature (Soldering, 60 sec.).....	+300°C
Maximum Junction Temperature (T_J)	+150°C
V+ Supply to V- Supply	36V
V+ Supply to Ground.....	36V
Logic Input Voltage Range	(-4V or V-) to V+ Supply
Analog Input Voltage	
Continuous	V- Supply to V+ Supply +20V
1% Duty Cycle and Driving all 4 inputs	
with 500µs pulse	V- Supply -15V to V+ Supply +20V
Maximum Current Through Any Pin	30mA

3.1 Thermal Characteristics:

Thermal Resistance, Q (cerdip) Package	
Junction-to-Case (Θ_{JC}) =	29°C/W Max
Junction-to-Ambient (Θ_{JA}) =	91°C/W Max

4.0 **Electrical Table:**

TABLE I						
Parameter See notes at end of table	Symbol	Conditions VS = ±15V Unless otherwise specified	Sub- group	Limit Min	Limit Max	Units
Positive Supply Current	I+	All channels OFF or ON	1 2,3		9 13.5	mA
Negative Supply Current	I-	All Channels OFF or ON	1 2,3		6.0 8.5	
Ground Current	I _G	All Channels OFF or ON	1 2,3		4 6	
Logic "0" Input Current	I _{IL}		1 2,3		5 10	μA
Logic "1" Input Current (Note 1)	I _{IH}		1 2,3		5 10	
"ON" Resistance	R _{ON}	V _A = -10V to 10V; I _S = 1mA	1 2,3		80 110	Ω
ΔR _{ON} vs. V _A	ΔR _{ON}	V _A ≤ 10V, I _S = 1mA	1		15	%
R _{ON} Match Between Switches (Note 3)	R _{ON} (Match)	V _A = 0V, I _D = 100μA	1 2,3		15 20	
Analog Current Range (Note 2)	I _A	V _S = ±10V	1 2,3	10 7		mA
Analog Voltage Range (Note 2)	V _A	I _S = 1mA	1,2,3	±10		
Source Current "OFF" Condition	I _{S(OFF)}	V _S = +10V, V _D = -10V	1 2		2 60	nA
		V _S = -10V, V _D = +10V	1 2		2 60	
Drain Current "OFF" Condition	I _{D(OFF)}	V _S = +10V, V _D = -10V	1 2		2 60	
		V _S = -10V, V _D = +10V	1 2		2 60	
Leakage Current "ON" Condition	I _{D(ON)} + I _{S(ON)}	V _S = V _D = ±10V	1 2		2 100	
Logic "0" Input Voltage	V _{IL}		1,2,3		0.8	V
Logic "1" Input Voltage	V _{IH}		1,2,3	2		V
Turn-On-Time	t _{ON}	V _S = -5V, R _L = 1KΩ, C _L = 13pF	9		500	nS
Turn-Off-Time	t _{OFF}		9		400	
Break-Before-Make Time	t _{ON-tOFF}		9	50		

TABLE I NOTES:

- Current Tested at VIN = 2V (worst case condition)
- V_A, V_{IH}, V_{IL} is verified by leakage and R_{ON} tests.
- R_{ON} Match specified as a percentage of R_{average} where R_{average} = $\frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 9
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

TABLE II NOTES

1/ PDA applies to Subgroup 1. Exclude delta's from PDA.2/ See Table III for delta parameters. See Table I for test conditions.**4.2 Table III. Burn-in test delta limits.**

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
R _{ON}	80	±15	ohm

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	7/12/2000
B	Update web site address. Under max ratings change T_J to T_I . For RON conditions, change $I_D = 1\text{mA}$ to $I_S = 1\text{mA}$. RON (Match), change subgroups from 1,2 to 2,3. Break before make specification must a minimum. Add subgroup 9 to Group A requirements on Table II. Change BI circuit from condition A to Condition C.	12/20/2001
C	Delete subgroups 4, 5, 6 from Table II, they are not used in Table I. Change paragraph 5.2 from cond. B to Cond. C (BI circuit not changed).	2/21/2002
D	Update web address. Delete burn-in circuit	6/20/2003
E	Update header/footer & add to 1.0 Scope description.	2/22/2008
F	Remove obsolete part numbers and update ASD to Analog Devices Standard	12/1/2011