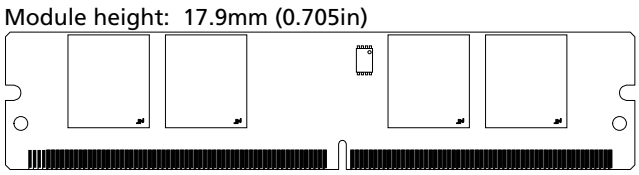
1.35V DDR3L SDRAM ULP Mini-UDIMM

MT18KBS1G72AKZ – 8GB

Features

- 244-pin, ultra low profile (17.9mm), mini unbuffered dual in-line, 82mm, memory module (ULP Mini-UDIMM)
- DDR3L functionality and operations supported as defined in the component data sheet
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 8GB (1 Gig x 72)
- V_{DD} = 1.35V (1.283–1.45V)
- V_{DD} = 1.5V (1.425–1.575V)
- Backward compatible to V_{DD} = 1.5V ±0.075V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank, using 4Gb TwinDie™ devices
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 244-Pin ULP Mini-UDIMM (R/C F)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 244-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

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Table 2: Addressing

Parameter	8GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb TwinDie (1 Gig x 8)
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT41K1G8,[1] 8Gb TwinDie 1.35V DDR3L SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18KBS1G72AKZ-1G6__	8GB	1 Gig x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18KBS1G72AKZ-1G4__	8GB	1 Gig x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18KBS1G72AKZ-1G1__	8GB	1 Gig x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18KBS1G72AKZ-1G4E1.

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Pin Assignments

Table 4: Pin Assignments

244-Pin DDR3 Mini-UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{TT}	31	DQ24	61	V_{DD}	92	DQ40
2	V_{REFDQ}	32	DQ25	62	A2	93	DQ41
3	V_{SS}	33	V_{SS}	63	V_{DD}	94	V_{SS}
4	DQ0	34	DQS3#	64	CK1	95	DQS5#
5	DQ1	35	DQS3	65	CK1#	96	DQS5
6	V_{SS}	36	V_{SS}	66	V_{DD}	97	V_{SS}
7	DQS0#	37	DQ26	67	V_{REFCA}	98	DQ42
8	DQS0	38	DQ27	68	V_{DD}	99	DQ43
9	V_{SS}	39	V_{SS}	69	NC	100	V_{SS}
10	DQ2	40	CB0	70	V_{DD}	101	DQ48
11	DQ3	41	CB1	71	A10	102	DQ49
12	V_{SS}	42	V_{SS}	72	BA0	103	V_{SS}
13	DQ8	43	DQS8#	73	V_{DD}	104	DQS6#
14	DQ9	44	DQS8	74	WE#	105	DQS6
15	V_{SS}	45	V_{SS}	75	CAS#	106	V_{SS}
16	DQS1#	46	CB2	76	V_{DD}	107	DQ50
17	DQS1	47	CB3	77	S1#	108	DQ51
18	V_{SS}	48	V_{SS}	78	ODT1	109	V_{SS}
19	DQ10	49	NC	79	V_{DD}	110	DQ56
20	DQ11	50	RESET#	80	NC	111	DQ57
21	V_{SS}	51	CKE0	81	NC	112	V_{SS}
22	DQ16	52	V_{DD}	82	V_{SS}	113	DQS7#
23	DQ17	53	BA2	83	DQ32	114	DQS7
24	V_{SS}	54	NC	84	DQ33	115	V_{SS}
25	DQS2#	55	V_{DD}	85	V_{SS}	116	DQ58
26	DQS2	56	A11	86	DQS4#	117	DQ59
27	V_{SS}	57	A7	87	DQS4	118	V_{SS}
28	DQ18	58	V_{DD}	88	V_{SS}	119	SA0
29	DQ19	59	A5	89	DQ34	120	SCL
30	V_{SS}	60	A4	90	DQ35	121	SA2
				91	V_{SS}	122	V_{TT}

244-Pin DDR3 Mini-UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
123	V_{TT}	153	DQ29	183	A3	214	DQ45
124	V_{SS}	154	V_{SS}	184	A1	215	V_{SS}
125	DQ4	155	DM3	185	V_{DD}	216	DM5
126	DQ5	156	NC	186	CK0	217	NC
127	V_{SS}	157	V_{SS}	187	CK0#	218	V_{SS}
128	DM0	158	DQ30	188	V_{DD}	219	DQ46
129	NC	159	DQ31	189	V_{DD}	220	DQ47
130	V_{SS}	160	V_{SS}	190	EVENT#	221	V_{SS}
131	DQ6	161	CB4	191	A0	222	DQ52
132	DQ7	162	CB5	192	V_{DD}	223	DQ53
133	V_{SS}	163	V_{SS}	193	BA1	224	V_{SS}
134	DQ12	164	DM8	194	V_{DD}	225	DM6
135	DQ13	165	NC	195	RAS#	226	NC
136	V_{SS}	166	V_{SS}	196	CS0#	227	V_{SS}
137	DM1	167	CB6	197	V_{DD}	228	DQ54
138	NC	168	CB7	198	ODT0	229	DQ55
139	V_{SS}	169	V_{SS}	199	A13	230	V_{SS}
140	DQ14	170	NC	200	V_{DD}	231	DQ60
141	DQ15	171	NC	201	NC	232	DQ61
142	V_{SS}	172	CKE1	202	NC	233	V_{SS}
143	DQ20	173	V_{DD}	203	V_{SS}	234	DM7
144	DQ21	174	A15	204	DQ36	235	NC
145	V_{SS}	175	A14	205	DQ37	236	V_{SS}
146	DM2	176	V_{DD}	206	V_{SS}	237	DQ62
147	NC	177	A12	207	DM4	238	DQ63
148	V_{SS}	178	A9	208	NC	239	V_{SS}
149	DQ22	179	V_{DD}	209	V_{SS}	240	V_{DDSPD}
150	DQ23	180	A8	210	DQ38	241	SA1
151	V_{SS}	181	A6	211	DQ39	242	SDA
152	DQ28	182	V_{DD}	212	V_{SS}	243	V_{SS}
				213	DQ44	244	V_{TT}

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Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

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Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

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DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	6	131	U2	0	18	28
	1	1	5		1	21	144
	2	3	11		2	23	150
	3	5	126		3	17	23
	4	2	10		4	22	149
	5	4	125		5	16	22
	6	7	132		6	19	29
	7	0	4		7	20	143
U4	8	34	89	U5	0	50	107
	9	37	205		1	53	223
	10	39	211		2	55	229
	11	33	84		3	49	102
	12	38	210		4	54	228
	13	32	83		5	48	101
	14	35	90		6	51	108
	15	36	204		7	52	222
U6	0	57	111	U7	0	45	214
	1	62	237		1	46	219
	2	60	231		2	40	92
	3	59	117		3	43	99
	4	61	232		4	44	213
	5	63	238		5	47	220
	6	56	110		6	41	93
	7	58	116		7	42	98
U8	0	CB1	41	U9	0	29	153
	1	CB7	168		1	30	158
	2	CB5	162		2	24	31
	3	CB3	47		3	27	38
	4	CB4	161		4	28	152
	5	CB2	46		5	31	159
	6	CB0	40		6	25	32
	7	CB6	167		7	26	37

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Table 6: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	9	14				
	1	14	140				
	2	12	134				
	3	11	20				
	4	8	13				
	5	15	141				
	6	13	135				
	7	10	19				

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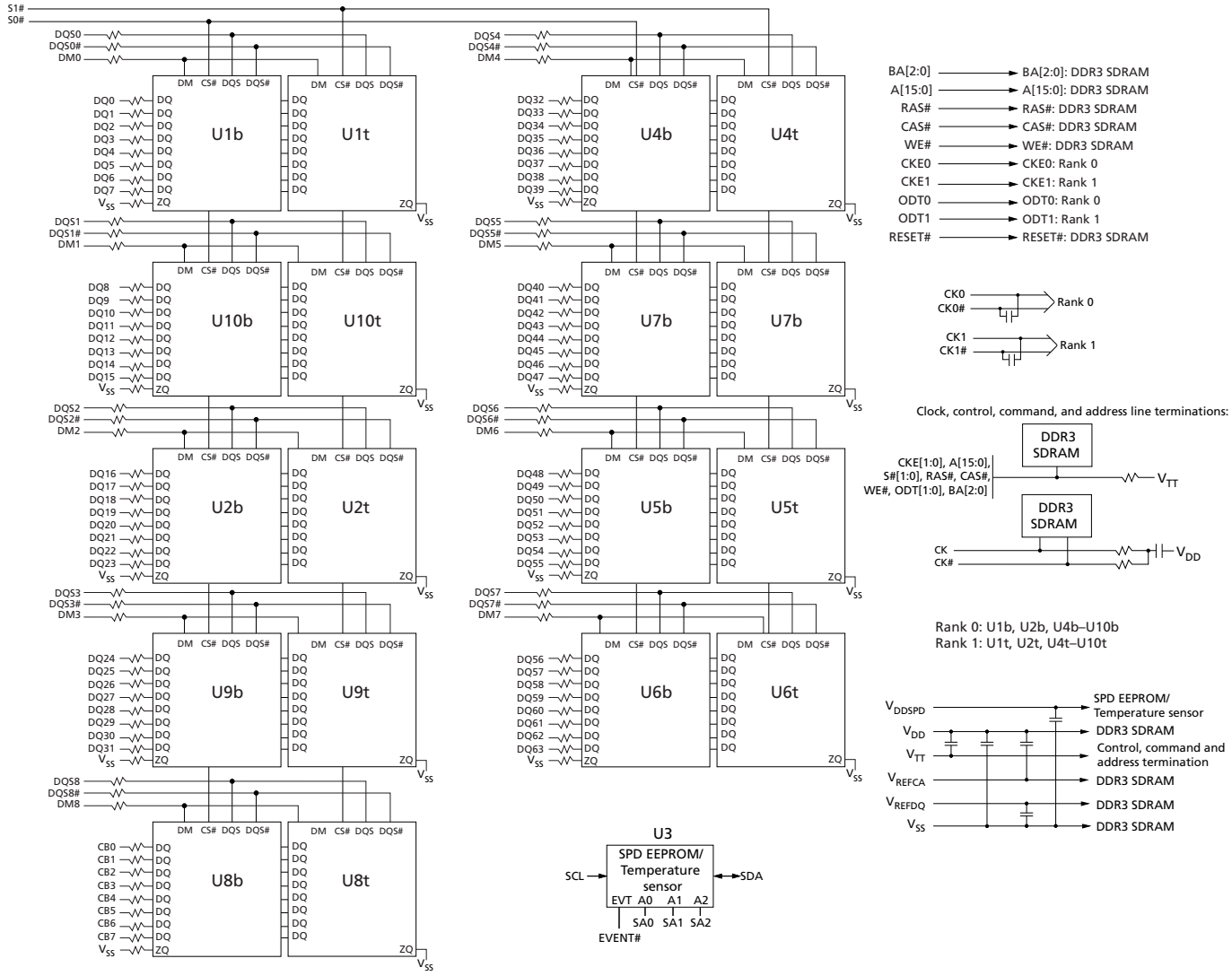
Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 8: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage		1.283	1.35	1.45	V	
			1.425	1.5	1.575	V	1
$V_{REFCA(DC)}$	Input reference voltage command/address bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus		0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	2
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	–36	0	36	µA	
		S#, CKE, ODT, CK, CK#	–18	0	18		
		DM	–4	0	4		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–10	0	10	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–18	0	18	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	3, 4

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Table 8: Operating Conditions (Continued)

Symbol	Parameter		Min	Nom	Max	Unit	Notes
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	3, 4, 5

Notes:
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
2. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
3. T_A and T_C are simultaneous requirements.
4. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
5. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

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DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 9: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

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I_{DD} Specifications

Table 10: DDR3 I_{CDD} Specifications and Conditions – 8GB (Die Revision E)

Values are for the MT41K1G8 DDR3L SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) 1.35V TwinDie component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{CDD0}	639	567	540	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{CDD1}	738	702	675	mA
Precharge power-down current: Slow exit	I_{CDD2P0}	288	288	288	mA
Precharge power-down current: Fast exit	I_{CDD2P1}	432	396	378	mA
Precharge quiet standby current	I_{CDD2Q}	387	369	342	mA
Precharge standby current	I_{CDD2N}	396	369	360	mA
Precharge standby ODT current	I_{CDD2NT}	450	414	387	mA
Active power-down current	I_{CDD3P}	486	459	432	mA
Active standby current	I_{CDD3N}	486	459	432	mA
Burst read operating current	I_{CDD4R}	1557	1404	1251	mA
Burst write operating current	I_{CDD4W}	1269	1134	999	mA
Refresh current	I_{CDD5B}	1539	1476	1440	mA
Self refresh temperature current: MAX T_C = 85°C	I_{CDD6}	360	360	360	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{CDD6ET}	450	450	450	mA
All banks interleaved read current	I_{CDD7}	2124	1854	1584	mA
Reset current	I_{CDD8}	324	324	324	mA

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Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the SPD EEPROM. Refer to JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 11: Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}	–	2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	1.45	V_{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	–	0.55	V
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	–	0.4	V
Input current	I_{IN}	–5.0	5.0	µA
Temperature sensing range	–	–40	125	°C
Temperature sensor accuracy (class B)	–	–1.0	1.0	°C

Table 12: Temperature Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs
SCL clock frequency	^tSCL	10	100	kHz
Data setup time	$^tSU:DAT$	250	–	ns
Start condition setup time	$^tSU:STA$	4.7	–	µs
Stop condition setup time	$^tSU:STO$	4.0	–	µs

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EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

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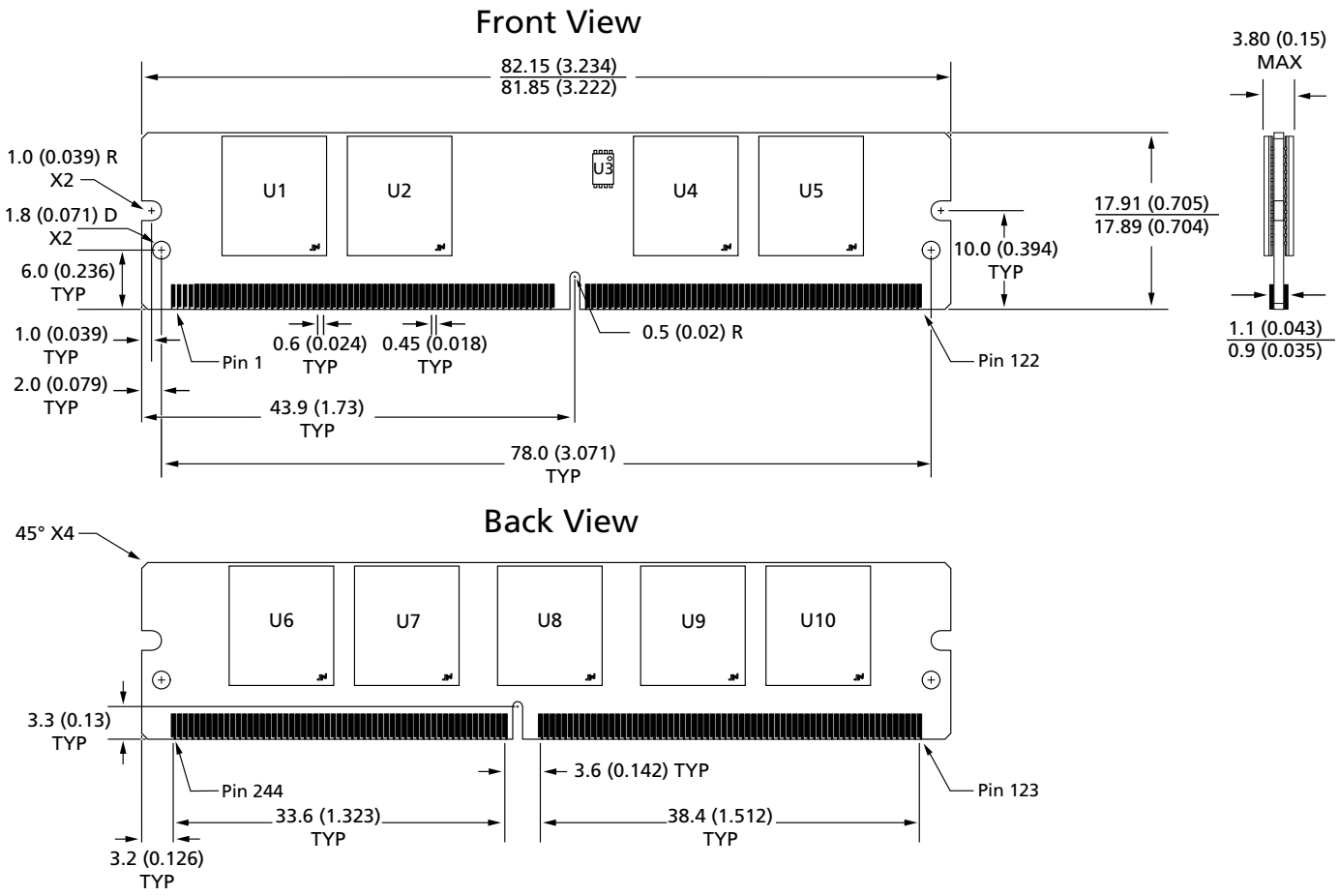
Module Dimensions

Figure 3: 244-Pin DDR3 ULP Mini-UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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