

LM4950 Boomer® Audio Power Amplifier Series

7.5W Mono-BTL or 3.1W Stereo Audio Power Amplifier

General Description

The LM4950 is a dual audio power amplifier primarily designed for demanding applications in flat panel monitors and TV's. It is capable of delivering 3.1 watts per channel to a 4Ω single-ended load with less than 1% THD+N or 7.5 watts mono BTL to an 8Ω load, with less than 10% THD+N from a 12V_{DC} power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4950 does not require bootstrap capacitors or snubber circuits. Therefore, it is ideally suited for display applications requiring high power and minimal size.

The LM4950 features a low-power consumption active-low shutdown mode. Additionally, the LM4950 features an internal thermal shutdown protection mechanism along with short circuit protection.

The LM4950 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4950 is a unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

| | |
|---|------------|
| ■ Quiescent Power Supply Current | 16mA (typ) |
| ■ P _{OUT} (SE) V _{DD} = 12V, R _L = 4Ω, 1% THD+N | 3.1W (typ) |
| ■ P _{OUT} (BTL) V _{DD} = 12V, R _L = 8Ω, 10% THD+N | 7.5W (typ) |
| ■ Shutdown current | 40μA (typ) |

Features

- Pop & click circuitry eliminates noise during turn-on and turn-off transitions
- Low current, active-low shutdown mode
- Low quiescent current
- Stereo 3.1W output, R_L = 4Ω
- Mono 7.5W BTL output, R_L = 8Ω
- Short circuit protection
- Unity-gain stable
- External gain configuration capability

Applications

- Flat Panel Monitors
- Flat panel TV's
- Computer Sound Cards

Typical Application

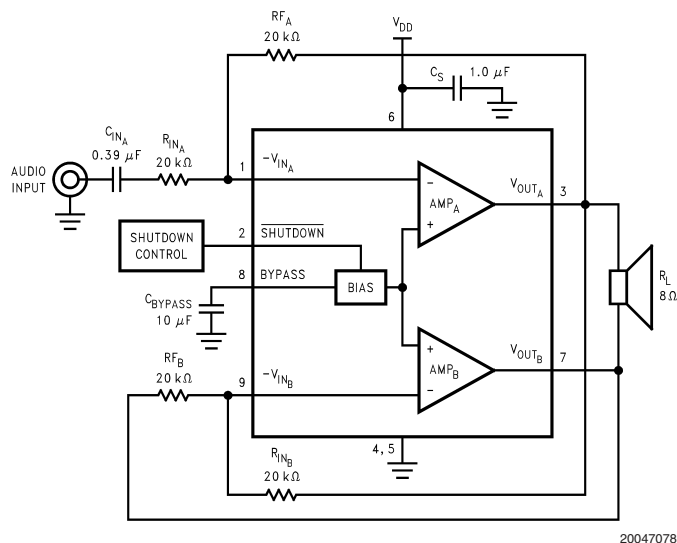
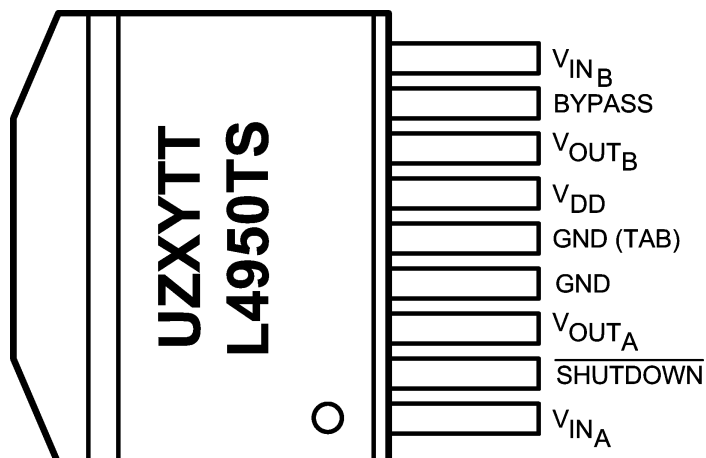


FIGURE 1. Typical Bridge-Tied-Load (BTL) Audio Amplifier Application Circuit

Connection Diagrams

Plastic Package, TO-263



20047070

Top View

U = Wafer Fab Code

Z = Assembly Plant Code

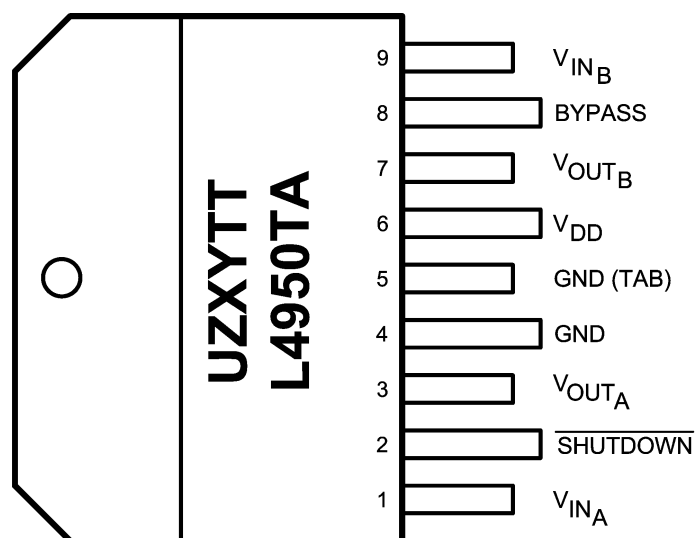
XY = Date Code

TT = Die Traceability

Order Number LM4950TS

See NS Package Number TS9A

Plastic Package, TO-220



20047071

Top View

U = Wafer Fab Code

Z = Assembly Plant Code

XY = Date Code

TT = Die Traceability

Order Number LM4950TA

See NS Package Number TA09A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--------------------------|
| Supply Voltage (pin 6, referenced to GND, pins 4 and 5) | 18.0V |
| Storage Temperature | -65°C to +150°C |
| Input Voltage | |
| pins 3 and 7 | -0.3V to $V_{DD} + 0.3V$ |
| pins 1, 2, 8, and 9 | -0.3V to 9.5V |
| Power Dissipation (Note 3) | Internally limited |
| ESD Susceptibility (Note 4) | 2000V |
| ESD Susceptibility (Note 5) | 200V |

| | |
|-----------------------------|--------|
| Junction Temperature | 150°C |
| Thermal Resistance | |
| θ_{JC} (TS) | 4°C/W |
| θ_{JA} (TS) (Note 3) | 20°C/W |
| θ_{JC} (TA) | 4°C/W |
| θ_{JA} (TA) (Note 3) | 20°C/W |

Operating Ratings

| | |
|---------------------------------|-----------------------------|
| Temperature Range | |
| $T_{MIN} \leq T_A \leq T_{MAX}$ | -40°C $\leq T_A \leq$ 85°C |
| Supply Voltage | 9.6V $\leq V_{DD} \leq$ 16V |

Electrical Characteristics $V_{DD} = 12V$ (Notes 1, 2)

The following specifications apply for $V_{DD} = 12V$, $A_V = 0dB$ (SE) or 6dB (BTL) unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

| Symbol | Parameter | Conditions | LM4950 | | Units (Limits) |
|-----------------|-----------------------------------|---|---------------------|-----------------------|----------------------|
| | | | Typical (Note 6) | Limit (Notes 7, 8) | |
| I_{DD} | Quiescent Power Supply Current | $V_{IN} = 0V$, $I_O = 0A$, No Load | 16 | 30 | mA (max) |
| I_{SD} | Shutdown Current | $V_{SHUTDOWN} = GND$ (Note 9) | 40 | 80 | μA (max) |
| V_{OS} | Offset Voltage | $V_{IN} = 0V$, $R_L = 8\Omega$ | 5 | 30 | mV (max) |
| V_{SDIH} | Shutdown Voltage Input High | | | 2.0 $V_{DD}/2$ | V (min) V (max) |
| V_{SDIL} | Shutdown Voltage Input Low | | | 0.4 | V (max) |
| T_{WU} | Wake-up Time | $C_B = 10\mu F$ | 440 | | ms |
| TSD | Thermal Shutdown Temperature | | 170 | 150 190 | °C (min) °C (max) |
| P_O | Output Power | $f = 1kHz$ $R_L = 4\Omega$ SE, Single Channel, THD+N = 1% $R_L = 8\Omega$ BTL, THD+N = 10% | 3.1 7.5 | 3.0 | W (min) |
| THD+N | Total Harmonic Distortion + Noise | $P_O = 2.5W_{rms}$; $f = 1kHz$; $R_L = 4\Omega$ SE | 0.05 | | % |
| | | $P_O = 2.5W_{rms}$; $A_V = 10$; $f = 1kHz$; $R_L = 4\Omega$, SE | 0.14 | | |
| ϵ_{OS} | Output Noise | A-Weighted Filter, $V_{IN} = 0V$, Input Referred | 10 | | μV |
| X_{TALK} | Channel Separation | $f_{IN} = 1kHz$, $P_O = 1W$, SE Mode $R_L = 8\Omega$ $R_L = 4\Omega$ | 76 70 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE} = 200mV_{p-p}$, $f = 1kHz$, $R_L = 8\Omega$, BTL | 70 | 56 | dB (min) |
| I_{OL} | Output Current Limit | $V_{IN} = 0V$, $R_L = 500m\Omega$ | 5 | | A |

Note 1: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in Absolute Maximum Ratings, whichever is lower. For the LM4950 typical application (shown in Figure 1) with $V_{DD} = 12V$, $R_L = 4\Omega$ stereo operation the total power dissipation is 3.65W. $\theta_{JA} = 20^\circ C/W$ for both TO263 and TO220 packages mounted to 16in² heatsink surface area.

Note 4: Human body model, 100pF discharged through a 1.5 k Ω resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

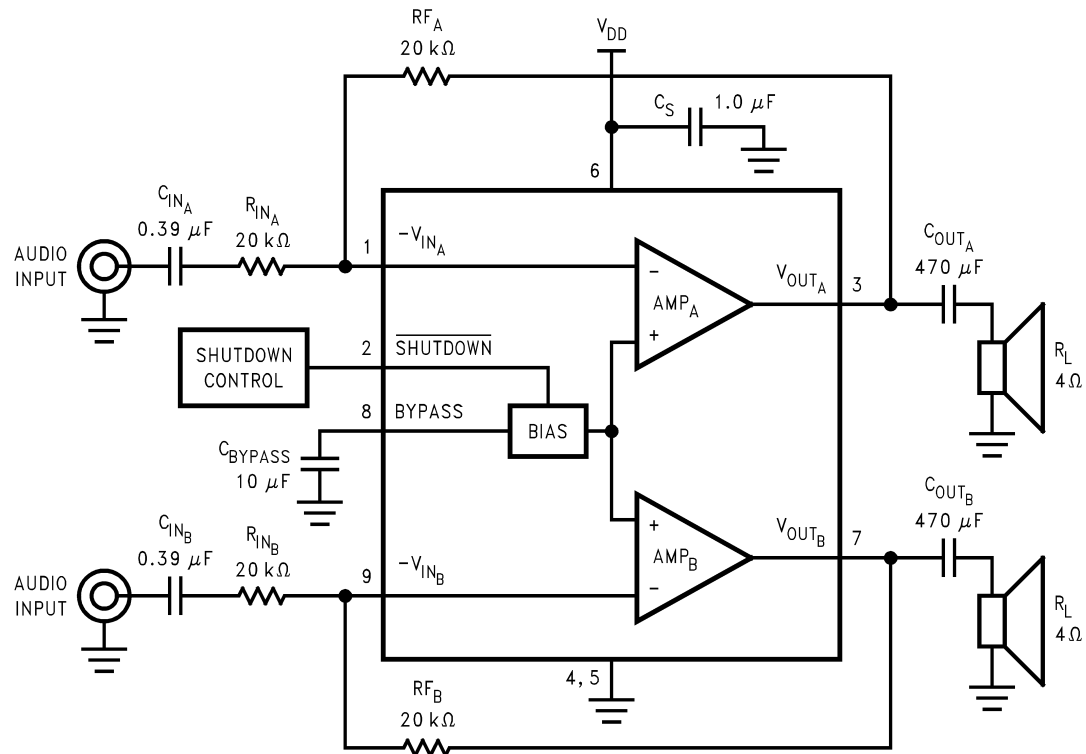
Electrical Characteristics $V_{DD} = 12V$ (Notes 1, 2) (Continued)

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current is measured in a normal room environment. The Shutdown pin should be driven as close as possible to GND for minimum shutdown current.



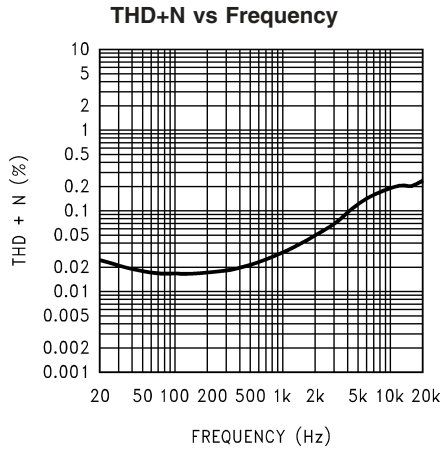
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FIGURE 2. Typical Stereo Single-Ended (SE) Audio Amplifier Application Circuit

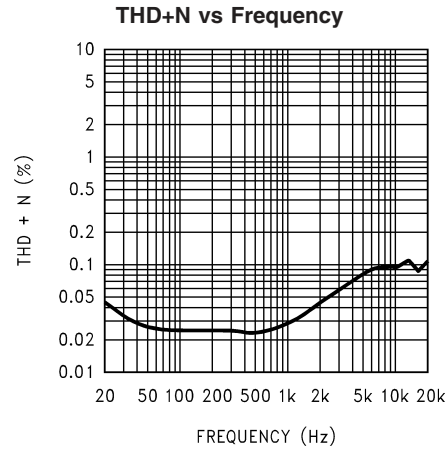
External Components Description Refer to (Figure 1.)

| Components | Functional Description |
|-----------------|---|
| 1. R_{IN} | This is the inverting input resistance that, along with R_F , sets the closed-loop gain. Input resistance R_{IN} and input capacitance C_{IN} form a high pass filter. The filter's cutoff frequency is $f_c = 1/(2\pi R_{IN} C_{IN})$. |
| 2. C_{IN} | This is the input coupling capacitor. It blocks DC voltage at the amplifier's inverting input. C_{IN} and R_{IN} create a highpass filter. The filter's cutoff frequency is $f_c = 1/(2\pi R_{IN} C_{IN})$. Refer to the SELECTING EXTERNAL COMPONENTS , for an explanation of determining C_{IN} 's value. |
| 3. R_F | This is the feedback resistance that, along with R_i , sets closed-loop gain. |
| 4. C_S | The supply bypass capacitor. Refer to the POWER SUPPLY BYPASSING section for information about properly placing, and selecting the value of, this capacitor. |
| 5. C_{BYPASS} | This capacitor filters the half-supply voltage present on the BYPASS pin. Refer to the Application section, SELECTING EXTERNAL COMPONENTS , for information about properly placing, and selecting the value of, this capacitor. |

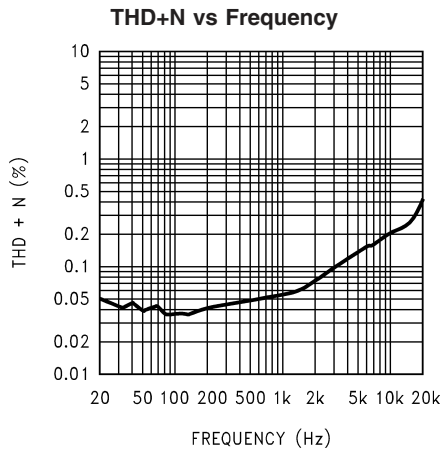
Typical Performance Characteristics



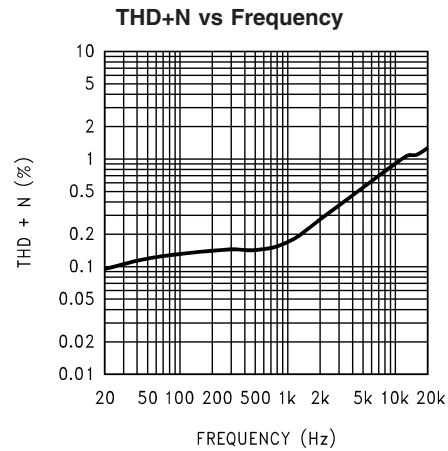
$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $P_{OUT} = 1W$



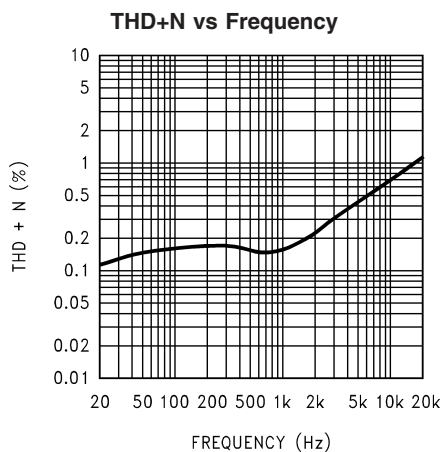
$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $P_{OUT} = 3W$



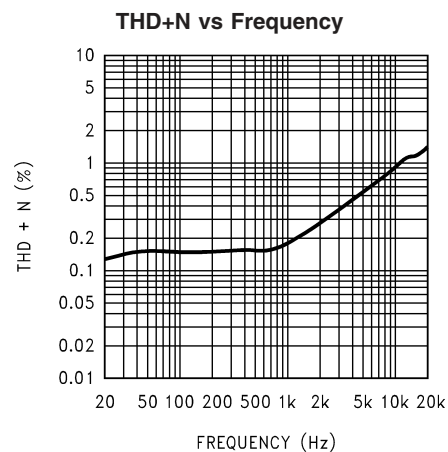
$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $P_{OUT} = 5W$



$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $BT_{LA_V} = 20$, $P_{OUT} = 1W$

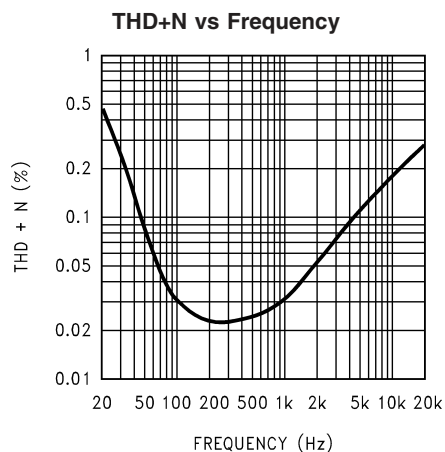


$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $BT_{LA_V} = 20$, $P_{OUT} = 3W$

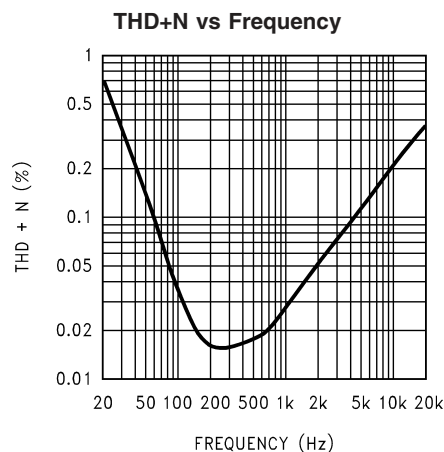


$V_{DD} = 12V$, $R_L = 8\Omega$,
BTL operation, $BT_{LA_V} = 20$, $P_{OUT} = 5W$

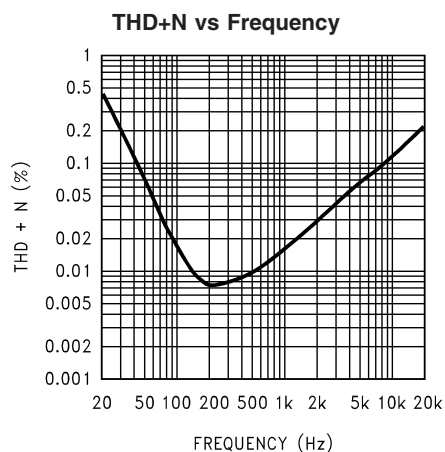
Typical Performance Characteristics (Continued)



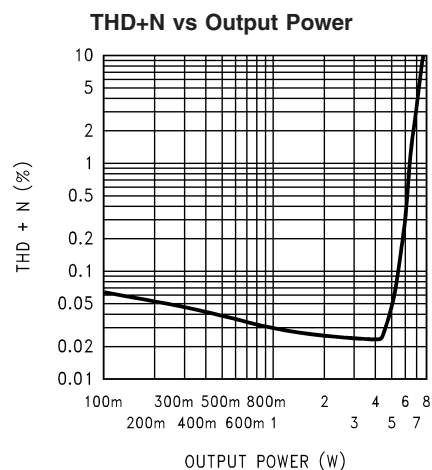
20047099
 $V_{DD} = 12V$, $R_L = 4\Omega$, SE operation,
 both channels driven and loaded (average shown),
 $P_{OUT} = 1W$, $A_V = 1$



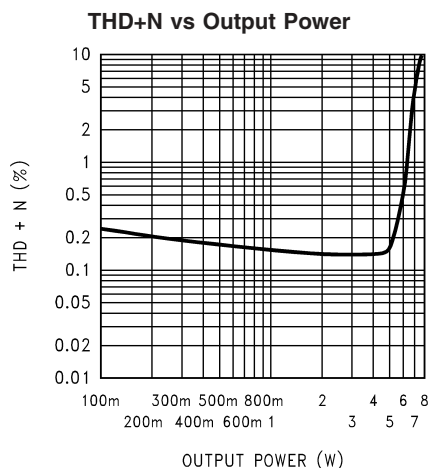
200470A0
 $V_{DD} = 12V$, $R_L = 4\Omega$, SE operation,
 both channels driven and loaded (average shown),
 $P_{OUT} = 2.5W$, $A_V = 1$



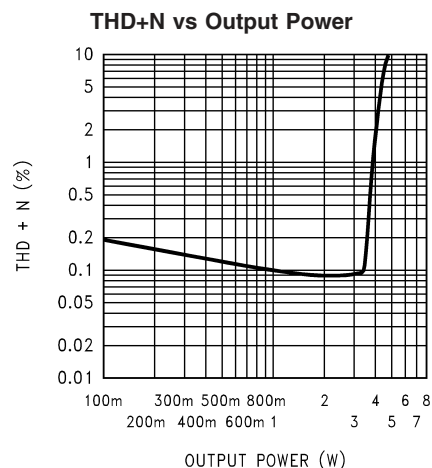
200470A1
 $V_{DD} = 12V$, $R_L = 8\Omega$, SE operation,
 both channels driven and loaded (average shown),
 $P_{OUT} = 1W$, $A_V = 1$



200470A9
 $V_{DD} = 12V$, $R_L = 8\Omega$,
 BTL operation, $f_{IN} = 1kHz$

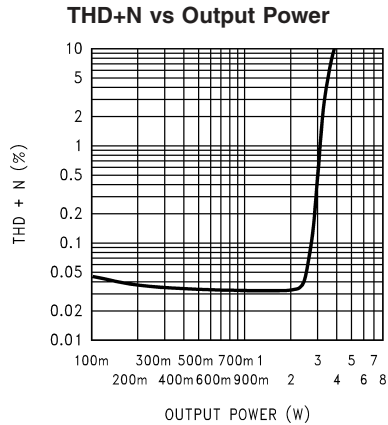


200470D0
 $V_{DD} = 12V$, $R_L = 8\Omega$,
 BTL operation, $BTLA_V = 20$, $f_{IN} = 1kHz$

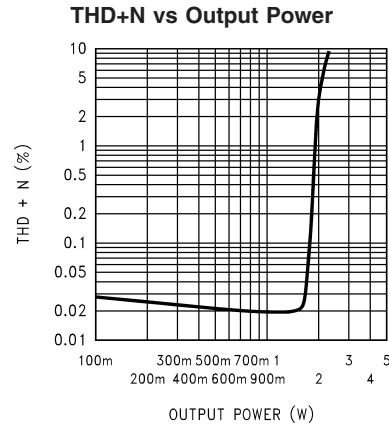


200470D1
 $V_{DD} = 12V$, $R_L = 16\Omega$,
 BTL operation, $BTLA_V = 20$, $f_{IN} = 1kHz$

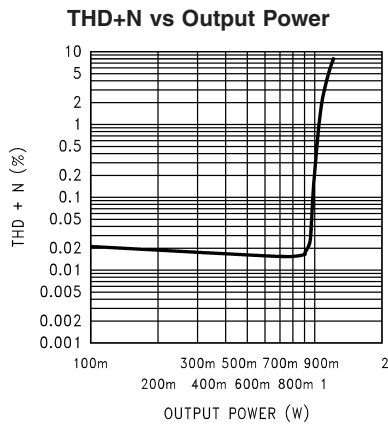
Typical Performance Characteristics (Continued)



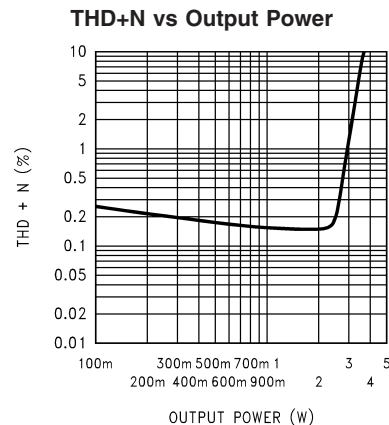
$V_{DD} = 12V$, $R_L = 4\Omega$, SE operation,
both channels driven and loaded (average shown),
 $f_{IN} = 1kHz$



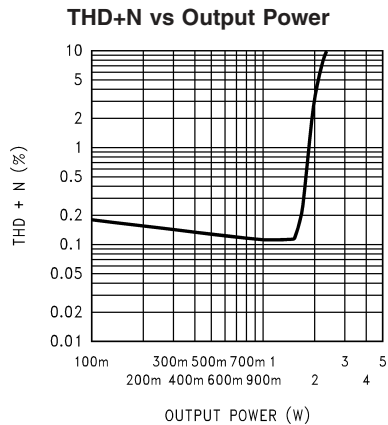
$V_{DD} = 12V$, $R_L = 8\Omega$, SE operation,
both channels driven and loaded (average shown),
 $f_{IN} = 1kHz$



$V_{DD} = 12V$, $R_L = 16\Omega$, SE operation,
both channels driven and loaded (average shown),
 $f_{IN} = 1kHz$

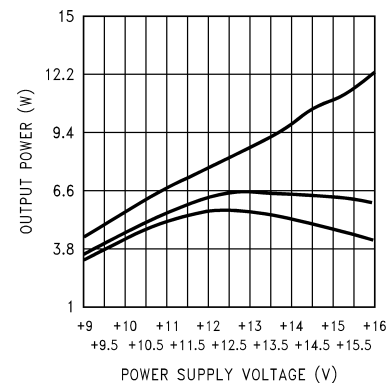


$V_{DD} = 12V$, $R_L = 4\Omega$, SE operation, $A_V = 10$
both channels driven and loaded (average shown),
 $f_{IN} = 1kHz$



$V_{DD} = 12V$, $R_L = 8\Omega$, SE operation, $A_V = 10$
both channels driven and loaded (average shown),
 $f_{IN} = 1kHz$

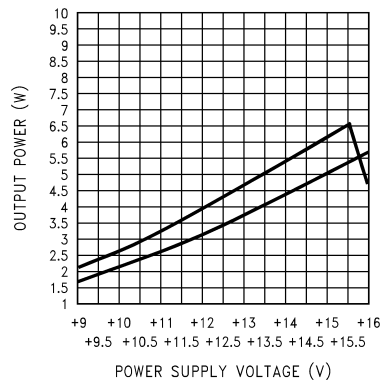
Output Power vs Power Supply Voltage



$R_L = 8\Omega$, BTL, $f_{IN} = 1kHz$,
at (from top to bottom at 12V): THD+N = 10%
THD+N = 1%, THD+N = 0.2%

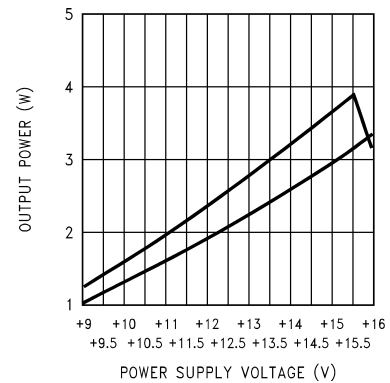
Typical Performance Characteristics (Continued)

Output Power vs Power Supply Voltage



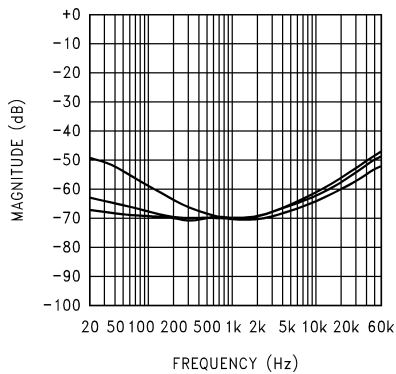
$R_L = 4\Omega$, SE operation,
both channels driven and loaded (average shown),
at (from top to bottom at 12V): THD+N = 10%,
THD+N = 1%

Output Power vs Power Supply Voltage



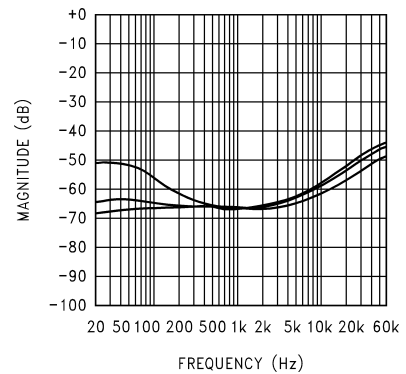
$R_L = 8\Omega$, SE operation, $f_{IN} = 1\text{kHz}$,
both channels driven and loaded (average shown),
at (from top to bottom at 12V): THD+N = 10%,
THD+N = 1%

Power Supply Rejection vs Frequency



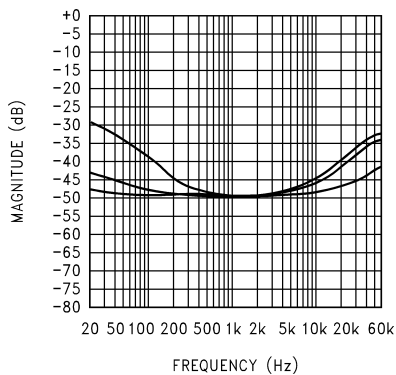
$V_{DD} = 12\text{V}$, $R_L = 8\Omega$, BTL operation,
 $V_{RIPPLE} = 200\text{mV}_{p-p}$, at (from top to bottom at 60Hz):
 $C_{BYPASS} = 1\mu\text{F}$, $C_{BYPASS} = 4.7\mu\text{F}$, $C_{BYPASS} = 10\mu\text{F}$,

Power Supply Rejection vs Frequency



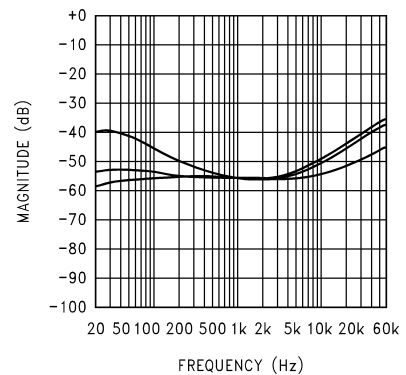
$V_{DD} = 12\text{V}$, $R_L = 8\Omega$, SE operation,
 $V_{RIPPLE} = 200\text{mV}_{p-p}$, at (from top to bottom at 60Hz):
 $C_{BYPASS} = 1\mu\text{F}$, $C_{BYPASS} = 4.7\mu\text{F}$, $C_{BYPASS} = 10\mu\text{F}$,

Power Supply Rejection vs Frequency



$V_{DD} = 12\text{V}$, $R_L = 8\Omega$, BTL operation, $V_{RIPPLE} = 200\text{mV}_{p-p}$,
 $A_V = 20$, at (from top to bottom at 60Hz):
 $C_{BYPASS} = 1\mu\text{F}$, $C_{BYPASS} = 4.7\mu\text{F}$, $C_{BYPASS} = 10\mu\text{F}$

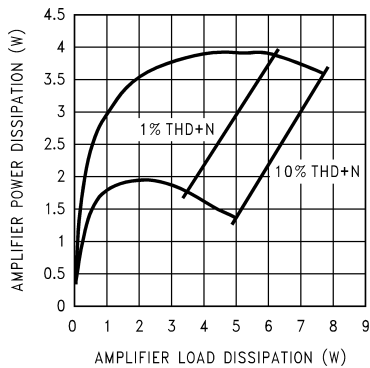
Power Supply Rejection vs Frequency



$V_{DD} = 12\text{V}$, $R_L = 8\Omega$, SE operation, $V_{RIPPLE} = 200\text{mV}_{p-p}$,
 $A_V = 10$, at (from top to bottom at 60Hz):
 $C_{BYPASS} = 1\mu\text{F}$, $C_{BYPASS} = 4.7\mu\text{F}$, $C_{BYPASS} = 10\mu\text{F}$

Typical Performance Characteristics (Continued)

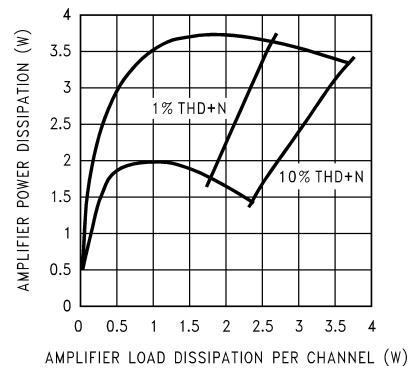
Total Power Dissipation vs Load Dissipation



20047084

$V_{DD} = 12V$, BTL operation, $f_{IN} = 1kHz$,
at (from top to bottom at 3W):
 $R_L = 8\Omega$, $R_L = 16\Omega$

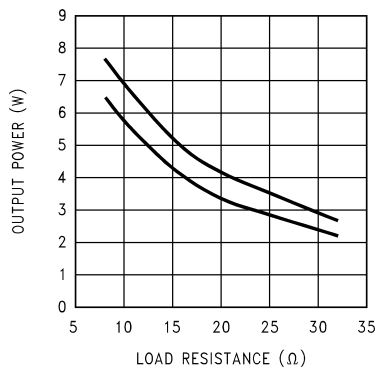
Total Power Dissipation vs Load Dissipation



20047081

$V_{DD} = 12V$, SE operation, $f_{IN} = 1kHz$,
at (from top to bottom at 1W):
 $R_L = 4\Omega$, $R_L = 8\Omega$

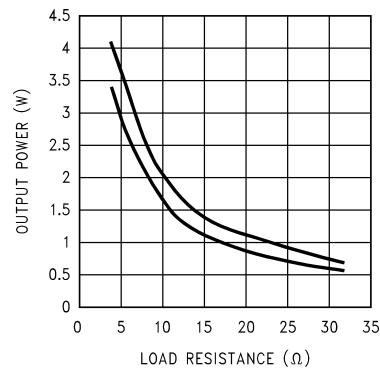
Output Power vs Load Resistance



20047094

$V_{DD} = 12V$, BTL operation, $f_{IN} = 1kHz$,
at (from top to bottom at 15 Ω):
THD+N = 10%, THD+N = 1%

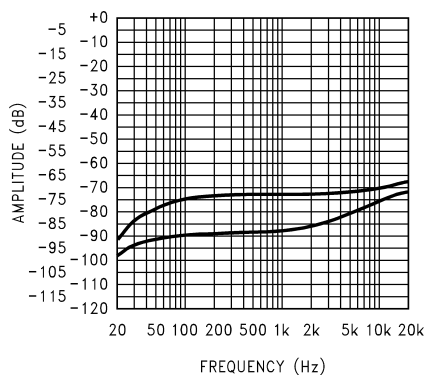
Output Power vs Load Resistance



20047091

$V_{DD} = 12V$, SE operation, $f_{IN} = 1kHz$,
both channels driven and loaded, at (from top to bottom
at 15 Ω):
THD+N = 10%, THD+N = 1%

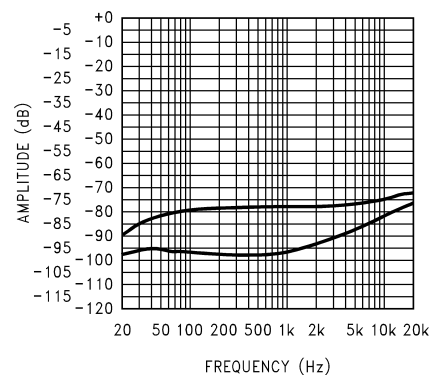
Channel-to-Channel Crosstalk vs Frequency



20047098

$V_{DD} = 12V$, $R_L = 4\Omega$, $P_{OUT} = 1W$, SE operation,
at (from top to bottom at 1kHz): V_{INB} driven,
 V_{OUTA} measured; V_{INA} driven, V_{OUTB} measured

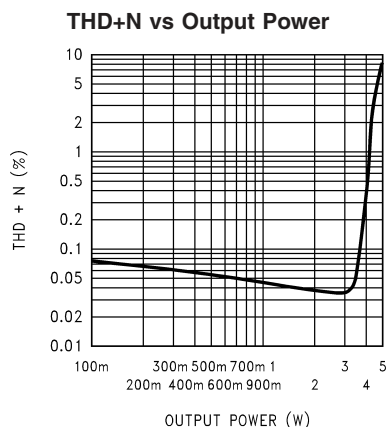
Channel-to-Channel Crosstalk vs Frequency



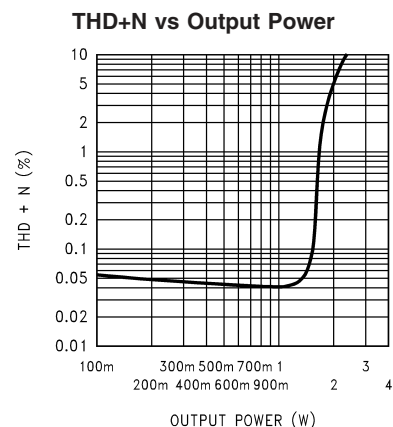
200470A3

$V_{DD} = 12V$, $R_L = 8\Omega$, $P_{OUT} = 1W$, SE operation,
at (from top to bottom at 1kHz): V_{INB} driven,
 V_{OUTA} measured; V_{INA} driven, V_{OUTB} measured

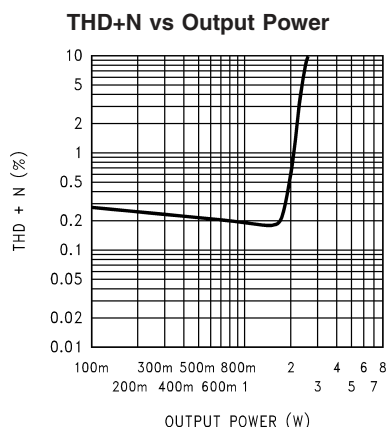
Typical Performance Characteristics (Continued)



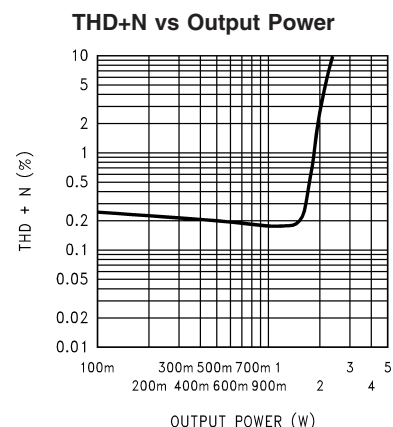
$V_{DD} = 9.6V$, $R_L = 8\Omega$,
BTL operation, $f_{IN} = 1kHz$



$V_{DD} = 9.6V$, $R_L = 4\Omega$,
SE operation, $f_{IN} = 1kHz$
both channels driven and loaded (average shown)

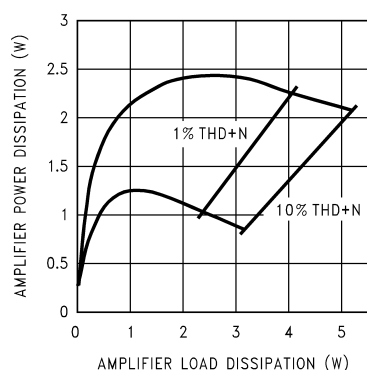


$V_{DD} = 9.6V$, $R_L = 8\Omega$, BTL operation,
 $BTLA_V = 20$, $f_{IN} = 1kHz$



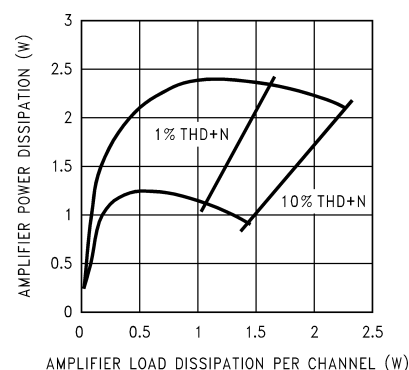
$V_{DD} = 9.6V$, $R_L = 4\Omega$, SE operation,
 $AV = 10$, $f_{IN} = 1kHz$
both channels driven and loaded (average shown)

Total Power Dissipation vs Load Dissipation



$V_{DD} = 9.6V$, BTL operation, $f_{IN} = 1kHz$
at (from top to bottom at 2W):
 $R_L = 8\Omega$, $R_L = 16\Omega$

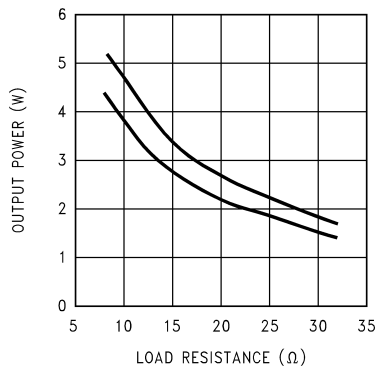
Total Power Dissipation vs Load Dissipation per Channel



$V_{DD} = 9.6V$, SE operation, $f_{IN} = 1kHz$,
at (from top to bottom at 1W):
 $R_L = 4\Omega$, $R_L = 8\Omega$

Typical Performance Characteristics (Continued)

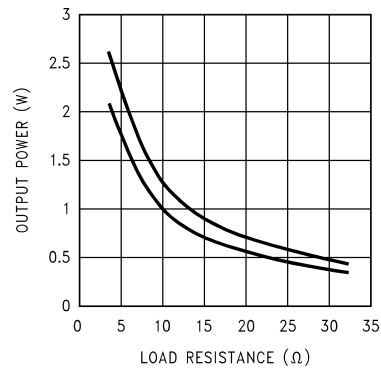
Output Power vs Load Resistance



20047095

$V_{DD} = 9.6V$, BTL operation, $f_{IN} = 1kHz$,
at (from top to bottom at 15Ω):
THD+N = 10%, THD+N = 1%

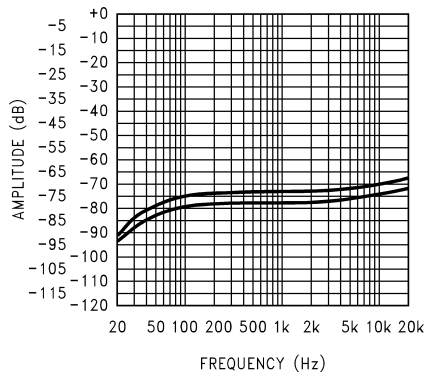
Output Power vs Load Resistance



20047092

$V_{DD} = 9.6V$, SE operation, $f_{IN} = 1kHz$,
both channels driven and loaded, at (from top to bottom
at 15Ω):
THD+N = 10%, THD+N = 1%

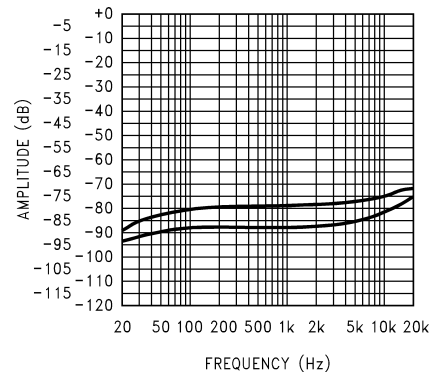
Channel-to Channel Crosstalk vs Frequency



20047096

$V_{DD} = 9.6V$, $R_L = 4\Omega$, $P_{OUT} = 1W$, SE operation,
at (from top to bottom at $1kHz$): V_{INB} driven, V_{OUTA}
measured; V_{INA} driven, V_{OUTB} measured

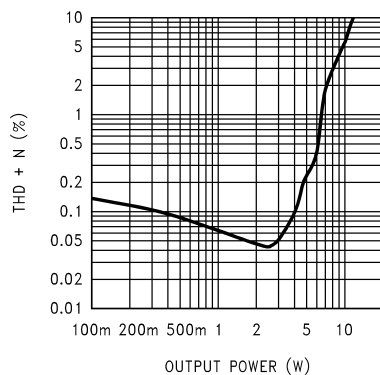
Channel-to Channel Crosstalk vs Frequency



200470A4

$V_{DD} = 9.6V$, $R_L = 8\Omega$, $P_{OUT} = 1W$, SE operation,
at (from top to bottom at $1kHz$): V_{INB} driven, V_{OUTA}
measured; V_{INA} driven, V_{OUTB} measured

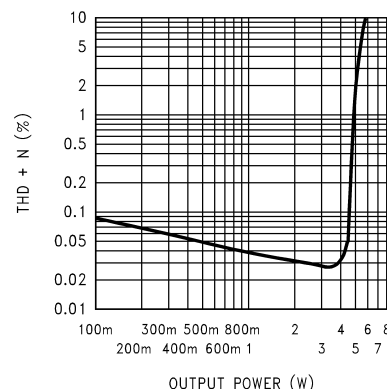
THD+N vs Output Power



200470C0

$V_{DD} = 15V$, $R_L = 8\Omega$,
BTL operation, $f_{IN} = 1kHz$

THD+N vs Output Power

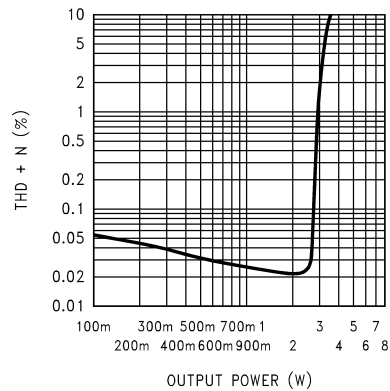


200470C2

$V_{DD} = 15V$, $R_L = 4\Omega$,
SE operation, $f_{IN} = 1kHz$
both channels driven and loaded (average shown)

Typical Performance Characteristics (Continued)

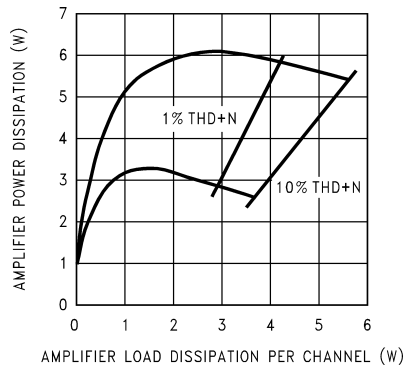
THD+N vs Output Power



200470E3

$V_{DD} = 15V$, $R_L = 8\Omega$,
SE operation, $f_{IN} = 1kHz$
both channels driven and loaded (average shown)

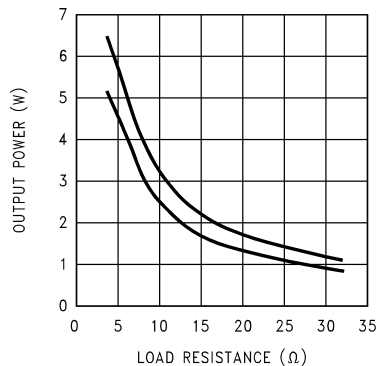
Total Power Dissipation vs Load Dissipation per Channel



20047080

$V_{DD} = 15V$, SE operation, $f_{IN} = 1kHz$,
at (from top to bottom at 2W): $R_L = 4\Omega$, $R_L = 8\Omega$

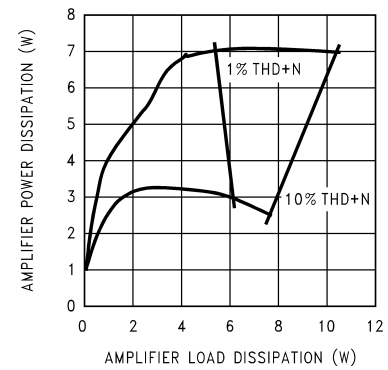
Output Power vs Load Resistance



20047090

$V_{DD} = 15V$, SE operation, $f_{IN} = 1kHz$,
both channels driven and loaded,
at (from top to bottom at 15Ω): THD+N = 10%, THD+N = 1%

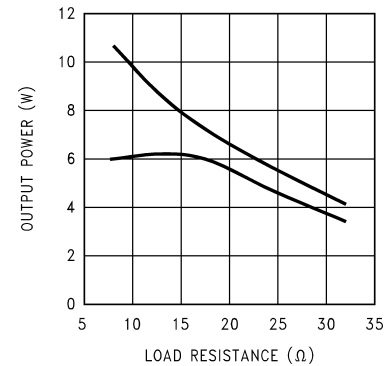
Total Power Dissipation vs Load Dissipation



20047083

$V_{DD} = 15V$, BTL operation, $f_{IN} = 1kHz$,
at (from top to bottom at 4W): $R_L = 8\Omega$, $R_L = 16\Omega$

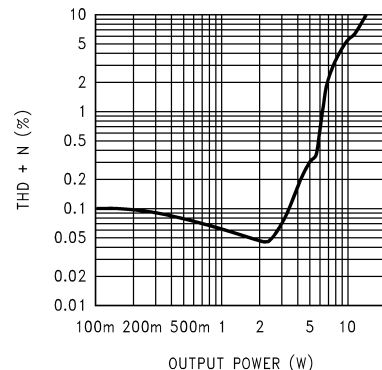
Output Power vs Load Resistance



20047093

$V_{DD} = 15V$, BTL operation, $f_{IN} = 1kHz$,
at (from top to bottom at 15Ω):
THD+N = 10%, THD+N = 1%

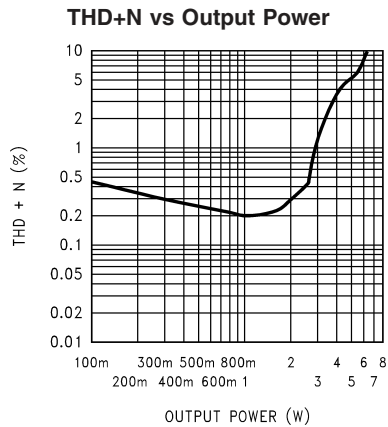
THD+N vs Output Power



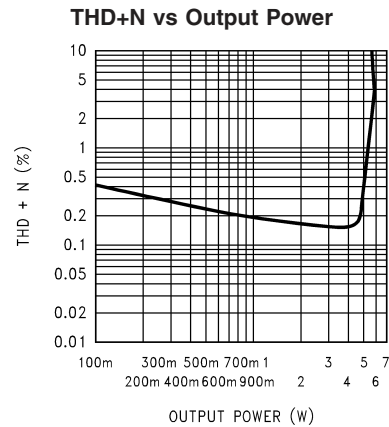
20047086

$V_{DD} = 16V$, $R_L = 8\Omega$,
BTL operation, $f_{IN} = 1kHz$

Typical Performance Characteristics (Continued)

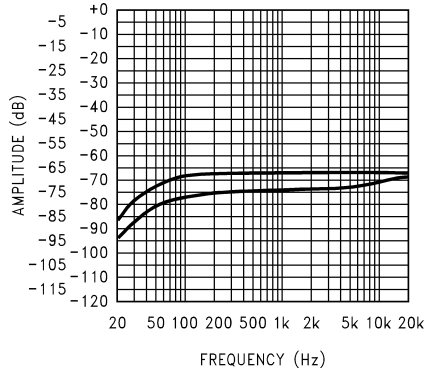


$V_{DD} = 16V$, $R_L = 8\Omega$,
BTL operation, $f_{IN} = 1kHz$, $BTLA_V = 20$



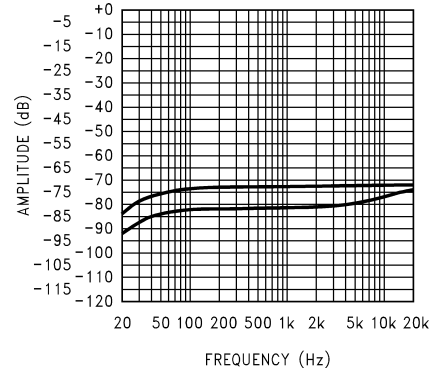
$V_{DD} = 16V$, $R_L = 4\Omega$, $A_V = 10$
SE operation, $f_{IN} = 1kHz$,
both channels driven and loaded (average shown)

Channel-to-Channel Crosstalk vs Frequency



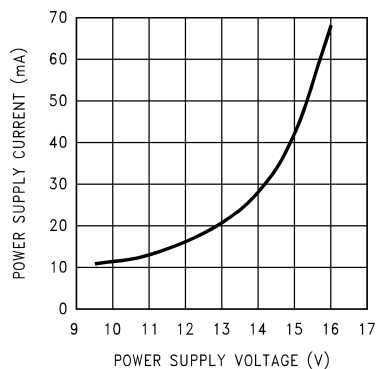
$V_{DD} = 16V$, $R_L = 4\Omega$, $P_{OUT} = 1W$, SE operation
at (from top to bottom at 1kHz): V_{INB} driven, V_{OUTA}
measured;
 V_{INA} driven, V_{OUTB} measured

Channel-to-Channel Crosstalk vs Frequency



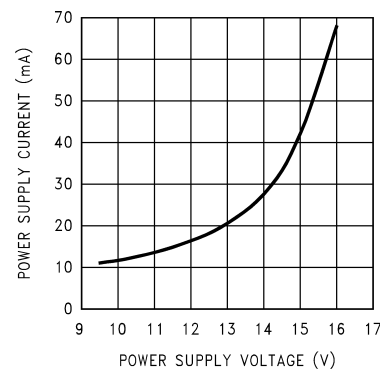
$V_{DD} = 16V$, $R_L = 8\Omega$, $P_{OUT} = 1W$, SE operation
at (from top to bottom at 1kHz): V_{INB} driven, V_{OUTA}
measured;
 V_{INA} driven, V_{OUTB} measured

Power Supply Current vs Power Supply Voltage



$R_L = 8\Omega$, BTL operation
 $V_{IN} = 0V$, $R_{SOURCE} = 50\Omega$

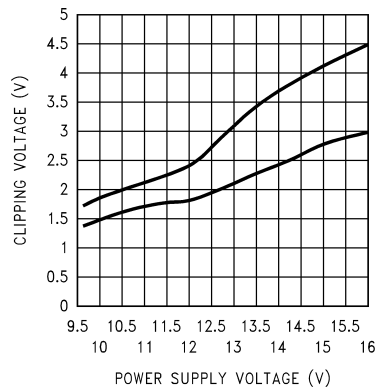
Power Supply Current vs Power Supply Voltage



$R_L = 4\Omega$, SE operation
 $V_{IN} = 0V$, $R_{SOURCE} = 50\Omega$

Typical Performance Characteristics (Continued)

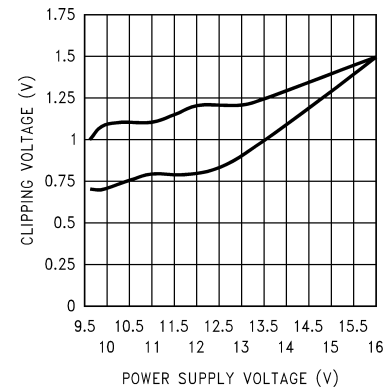
Clipping Voltage vs Power Supply Voltage



20047088

$R_L = 8\Omega$, BTL operation, $f_{IN} = 1\text{kHz}$
at (from top to bottom at 12V):
positive signal swing, negative signal swing

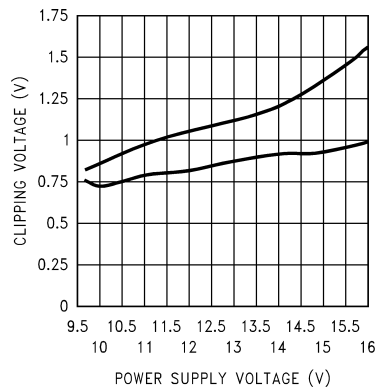
Clipping Voltage vs Power Supply Voltage



20047086

$R_L = 16\Omega$, BTL operation, $f_{IN} = 1\text{kHz}$
at (from to bottom at 12V):
positive signal swing, negative signal swing

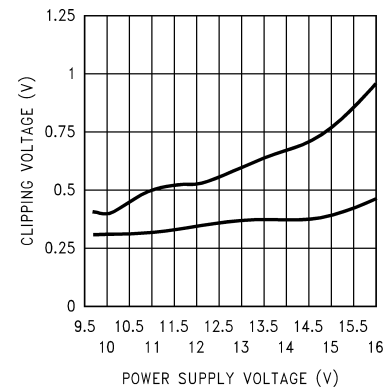
Clipping Voltage vs Power Supply Voltage



20047089

$R_L = 4\Omega$, SE operation, $f_{IN} = 1\text{kHz}$
both channels driven and loaded, at (from top to bottom
at 13V):
negative signal swing, positive signal swing

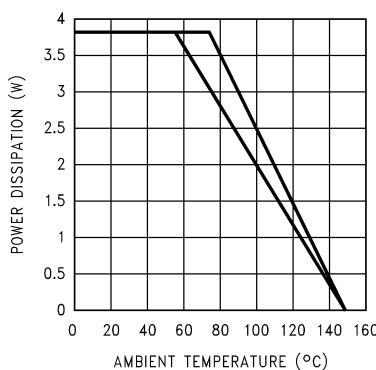
Clipping Voltage vs Power Supply Voltage



20047087

$R_L = 8\Omega$, SE operation, $f_{IN} = 1\text{kHz}$
both channels driven and loaded, at (from to bottom at
13V):
negative signal swing, positive signal swing

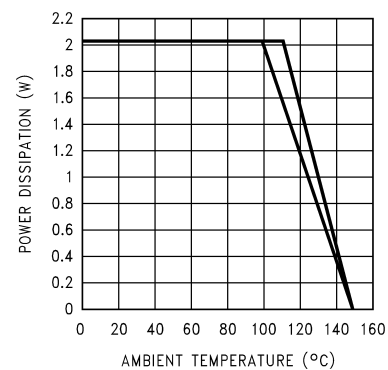
Power Dissipation vs Ambient Temperature



200470E6

$V_{DD} = 12\text{V}$, $R_L = 8\Omega$ (BTL), $f_{IN} = 1\text{kHz}$,
(from to bottom at 80°C): 16in² copper plane heatsink
area,
8in² copper plane heatsink area

Power Dissipation vs Ambient Temperature



200470E4

$V_{DD} = 12\text{V}$, $R_L = 8\Omega$ (SE), $f_{IN} = 1\text{kHz}$,
(from to bottom at 120°C): 16in² copper plane heatsink
area,
8in² copper plane heatsink area

Application Information

HIGH VOLTAGE BOOMER WITH INCREASED OUTPUT POWER

Unlike previous 5V Boomer® amplifiers, the LM4950 is designed to operate over a power supply voltages range of 9.6V to 16V. Operating on a 12V power supply, the LM4950 will deliver 7.5W into an 8Ω BTL load with no more than 10% THD+N.

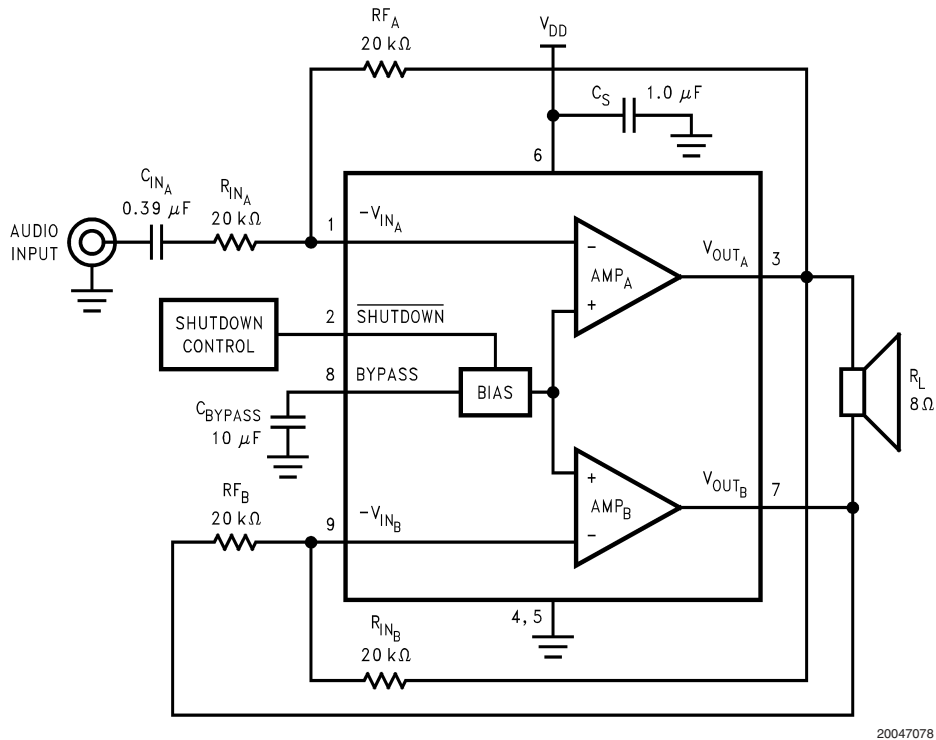


FIGURE 3. Typical LM4950 BTL Application Circuit

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 3, the LM4950 consists of two operational amplifiers that drive a speaker connected between their outputs. The value of external input and feedback resistors determine the gain of each amplifier. Resistors R_{IN_A} and R_{F_A} set the closed-loop gain of AMP_A , whereas two 20kΩ resistors set AMP_B 's gain to -1. The LM4950 drives a load, such as a speaker, connected between the two amplifier outputs, V_{OUT_A} and V_{OUT_B} . Figure 3 shows that AMP_A 's output serves as AMP_B 's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between AMP_A and AMP_B and driven differentially (commonly referred to as "bridge mode"). This results in a differential, or BTL, gain of

$$A_{VD} = 2(R_f / R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing

across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **AUDIO POWER AMPLIFIER DESIGN** section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing AMP_1 's and AMP_2 's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

Application Information (Continued)

$$P_{\text{DMAX-SE}} = (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{ Single Ended} \quad (2)$$

The LM4950's dissipation is twice the value given by Equation (2) when driving two SE loads. For a 12V supply and two 8Ω SE loads, the LM4950's dissipation is 1.82W.

The LM4950's dissipation when driving a BTL load is given by Equation (3). For a 12V supply and a single 8Ω BTL load, the dissipation is 3.65W.

$$P_{\text{DMAX-MONOBTL}} = 4(V_{\text{DD}})^2 / 2\pi^2 R_L: \text{ Bridge Mode} \quad (3)$$

The maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{\text{DMAX}}' = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (4)$$

The LM4950's $T_{\text{JMAX}} = 150^\circ\text{C}$. In the TS package, the LM4950's θ_{JA} is 20°C/W when the metal tab is soldered to a copper plane of at least 16in^2 . This plane can be split between the top and bottom layers of a two-sided PCB. Connect the two layers together under the tab with a 5x5 array of vias. For the TA package, use an external heatsink with a thermal impedance that is less than 20°C/W . At any given ambient temperature T_A , use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4950's maximum junction temperature.

$$T_A = T_{\text{JMAX}} - P_{\text{DMAX-MONOBTL}} \theta_{\text{JA}} \quad (5)$$

For a typical application with a 12V power supply and a BTL 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 77°C for the TS package.

$$T_{\text{JMAX}} = P_{\text{DMAX-MONOBTL}} \theta_{\text{JA}} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX} . If the result violates the LM4950's 150°C , reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (3) is greater than that of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. Further, ensure that speakers rated at a nominal 4Ω (SE operation) or 8Ω (BTL operation) do not fall below 3Ω or 6Ω, respectively. If these measures are insufficient, a heat sink can be added to reduce θ_{JA} . The heat sink can be created using

additional copper area around the package, with connections to the ground pins, supply pin and amplifier output pins. Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

POWER SUPPLY VOLTAGE LIMITS

Continuous proper operation is ensured by never exceeding the voltage applied to any pin, with respect to ground, as listed in the Absolute Maximum Ratings section.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a voltage regulator typically use a 10μF in parallel with a 0.1μF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0μF tantalum bypass capacitance connected between the LM4950's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4950's power supply pin and ground as short as possible. Connecting a 10μF capacitor, C_{BYPASS} , between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_{BYPASS} , depends on desired PSRR requirements, click and pop performance (as explained in the section, **SELECTING EXTERNAL COMPONENTS**), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The LM4950 features an active-low micro-power shutdown mode. When active, the LM4950's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 40μA typical shutdown current is achieved by applying a voltage to the SHUTDOWN pin that is as near to GND as possible. A voltage that is greater than GND may increase the shutdown current.

There are a few methods to control the micro-power shutdown. These include using a single-pole, single-throw switch (SPST), a microprocessor, or a microcontroller. When using a switch, connect a 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD} and a second 100kΩ resistor in parallel with the SPST switch connected between the SHUTDOWN pin and GND. The two resistors form a voltage divider that ensures that the voltage applied to the SHUTDOWN pin does not exceed $V_{\text{DD}}/2$. Select normal amplifier operation by opening the switch. Closing the switch applies GND to the SHUTDOWN pin, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the active-state voltage to the SHUTDOWN pin. Again, ensure that the microcontroller or microprocessor logic-high signal does not exceed the LM4950's $V_{\text{DD}}/2$ SHUTDOWN signal limit.

Application Information (Continued)

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Two quantities determine the value of the input coupling capacitor: the lowest audio frequency that requires amplification and desired output transient suppression.

As shown in Figure 3, the input resistor (R_{IN}) and the input capacitor (C_{IN}) produce a high pass filter cutoff frequency that is found using Equation (7).

$$f_c = 1/2\pi R_i C_i \quad (7)$$

As an example when using a speaker with a low frequency limit of 50Hz, C_i , using Equation (7) is 0.159 μ F. The 0.39 μ F C_{INA} shown in Figure 3 allows the LM4950 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_{BYPASS} , the capacitor connected to the BYPASS pin. Since C_{BYPASS} determines how fast the LM4950 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4950's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_{BYPASS} equal to 10 μ F along with a small value of C_{IN} (in the range of 0.1 μ F to 0.39 μ F), produces a click-less and pop-less shutdown function. As discussed above, choosing C_{IN} no larger than necessary for the desired bandwidth helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4950 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4950's internal amplifiers are configured as unity gain buffers and are disconnected from the AMP_A and AMP_B pins. An internal current source charges the capacitor connected between the BYPASS pin and GND in a

controlled manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage applied to the BYPASS pin.

The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of C_{BYPASS} alters the device's turn-on time. Here are some typical turn-on times for various values of C_{BYPASS} :

| C_B (μ F) | T_{ON} (ms) |
|------------------|---------------|
| 1.0 | 120 |
| 2.2 | 120 |
| 4.7 | 200 |
| 10 | 440 |

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

There is a relationship between the value of C_{IN} and C_{BYPASS} that ensures minimum output transient when power is applied or the shutdown mode is deactivated. Best performance is achieved by setting the time constant created by C_{IN} and $R_i + R_f$ to a value less than the turn-on time for a given value of C_{BYPASS} as shown in the table above.

DRIVING PIEZO-ELECTRIC SPEAKER TRANSDUCERS

The LM4950 is able to drive capacitive piezo-electric transducer loads that are less than equal to 200nF. Stable operation is assured by placing 33pF capacitors in parallel with the 20k Ω feedback resistors. The additional capacitors are shown in Figure 4.

When driving piezo-electric transducers, sound quality and acoustic power is entirely dependent upon a transducer's frequency response and efficiency. In this application, power dissipated by the LM4950 is very low, typically less than 250mW when driving a 200nF piezo-electric transducer ($V_{DD} = 12V$).

Application Information (Continued)

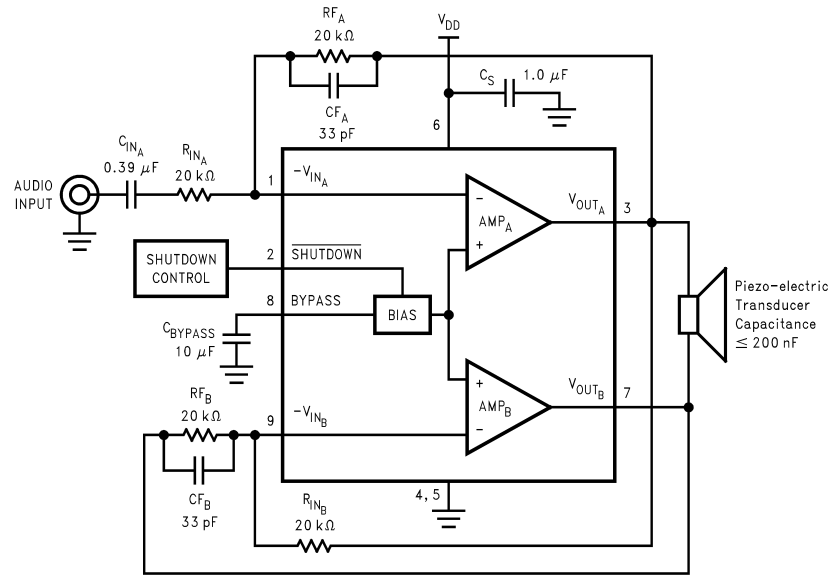


FIGURE 4. Piezo-electric Transducer Capacitance $\leq 200\text{nF}$

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 4W into an 8Ω BTL

The following are the desired operational parameters:

| | |
|-----------------|--------------------------------|
| Power Output | 4W _{RMS} |
| Load Impedance | 8Ω |
| Input Level | 0.3V _{RMS} (max) |
| Input Impedance | 20kΩ |
| Bandwidth | 50Hz–20kHz $\pm 0.25\text{dB}$ |

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the *Output Power vs Power Supply Voltage* curve in the **Typical Performance Characteristics** section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the *Clipping Dropout Voltage vs Power Supply Voltage* in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (8). The result is Equation (9).

$$V_{\text{opeak}} = \sqrt{2R_L P_O} \quad (8)$$

$$V_{DD} = V_{\text{OUTPEAK}} + V_{\text{ODTOP}} + V_{\text{ODBOT}} \quad (9)$$

The *Output Power vs. Power Supply Voltage* graph for an 8Ω load indicates a minimum supply voltage of 10.2V. The commonly used 12V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the LM4950 to produce peak output power in excess of 4W without clipping or other audible distortion. The choice of

supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the Power Dissipation section. After satisfying the LM4950's power dissipation requirements, the minimum differential gain needed to achieve 4W dissipation in an 8Ω BTL load is found using Equation (10).

$$A_V \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{\text{orms}} / V_{\text{inrms}} \quad (10)$$

Thus, a minimum gain of 18.9 allows the LM4950's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{V\text{-BTL}} = 19$. The amplifier's overall BTL gain is set using the input (R_{IN_A}) and feedback (R) resistors of the first amplifier in the series BTL configuration. Additionally, $A_{V\text{-BTL}}$ is twice the gain set by the first amplifier's R_{IN} and R_f . With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_f / R_{IN} = A_{V\text{-BTL}} / 2 \quad (11)$$

The value of R_f is 190kΩ (choose 191kΩ, the closest value). The nominal output power is 4W.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired $\pm 0.25\text{dB}$ pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the $\pm 0.25\text{dB}$ -desired limit. The results are an

$$f_L = 50\text{Hz} / 5 = 10\text{Hz} \quad (12)$$

Application Information (Continued)

and an

$$f_L = 20\text{kHz} \times 5 = 100\text{kHz} \quad (13)$$

As mentioned in the **SELECTING EXTERNAL COMPONENTS** section, R_{INA} and C_{INA} create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (14).

$$C_i = 1 / 2\pi R_{IN} f_L \quad (14)$$

The result is

$$1 / (2\pi \times 20\text{k}\Omega \times 10\text{Hz}) = 0.795\mu\text{F}$$

Use a 0.82 μF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD} , determines the

upper passband response limit. With $A_{VD} = 7$ and $f_H = 100\text{kHz}$, the closed-loop gain bandwidth product (GBWP) is 700kHz. This is less than the LM4950's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 5 through Figure 7 show the recommended two-layer PC board layout that is optimized for the TO263-packaged, SE-configured LM4950 and associated external components. Figure 8 through Figure 10 show the recommended two-layer PC board layout that is optimized for the TO263-packaged, BTL-configured LM4950 and associated external components. These circuits are designed for use with an external 12V supply and 4 Ω (min)(SE) or 8 Ω (min)(BTL) speakers.

These circuit boards are easy to use. Apply 12V and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker between the board's OUT_A and OUT_B outputs.

Demonstration Board Layout

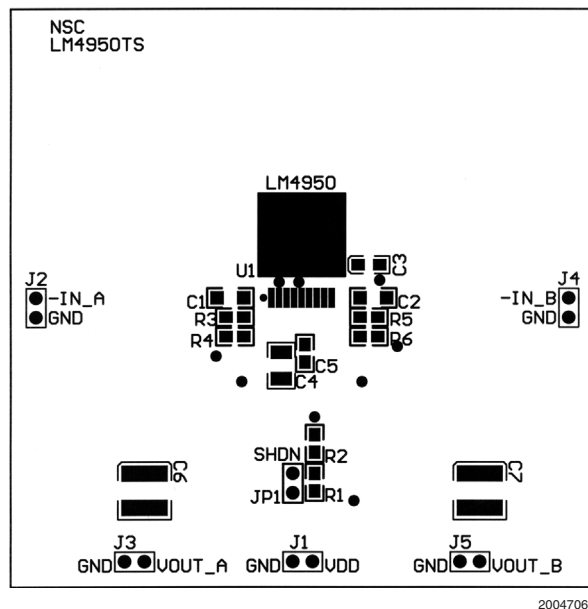
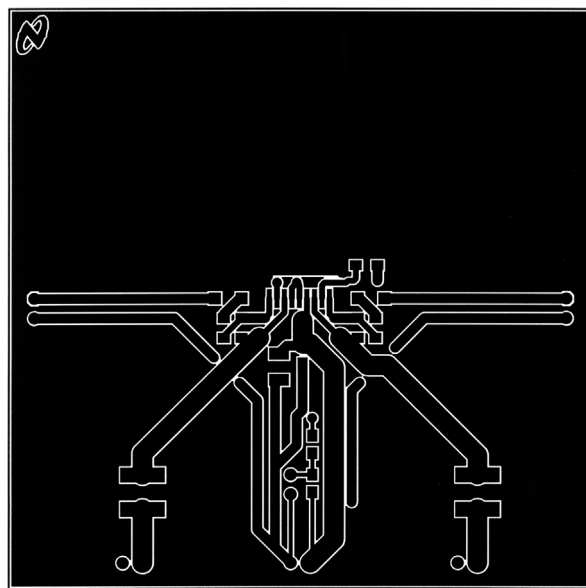


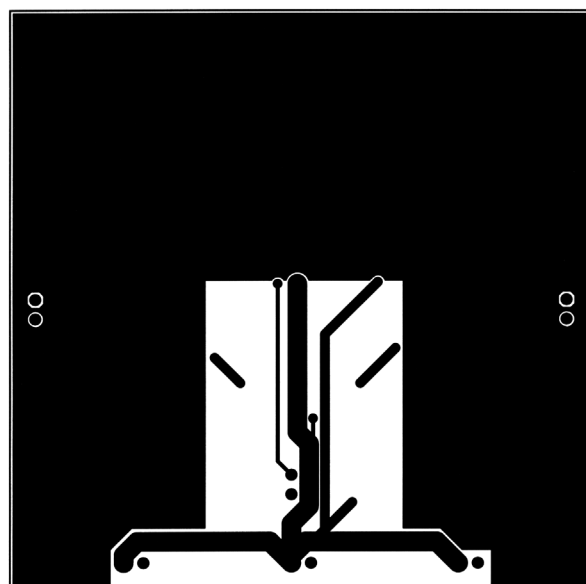
FIGURE 5. Recommended TS SE PCB Layout:
Top Silkscreen

Demonstration Board Layout (Continued)



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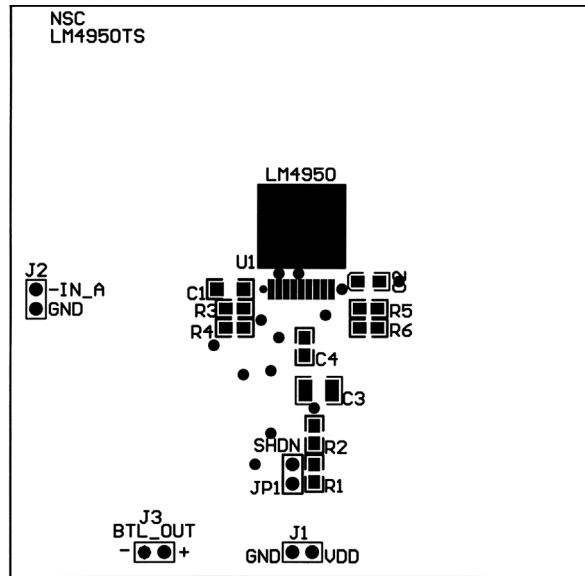
FIGURE 6. Recommended TS SE PCB Layout:
Top Layer



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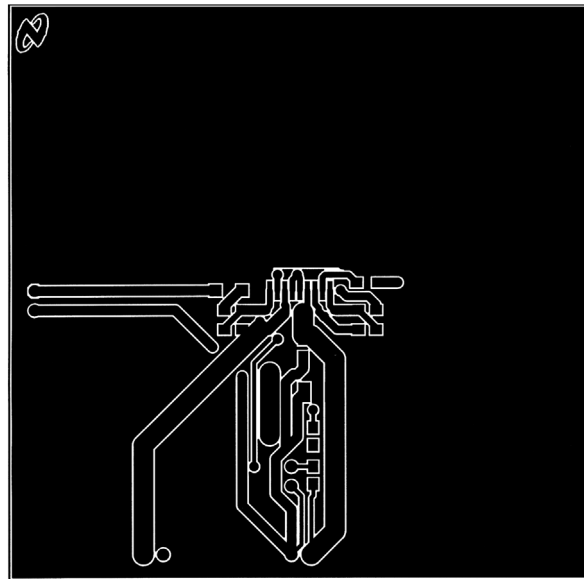
FIGURE 7. Recommended TS SE PCB Layout:
Bottom Layer

Demonstration Board Layout (Continued)



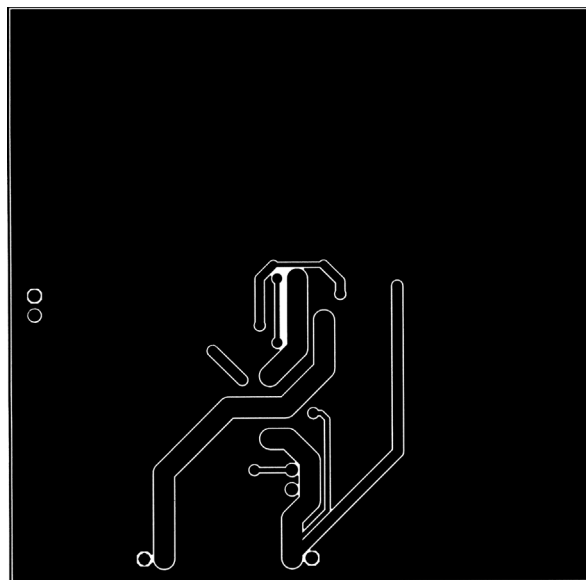
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FIGURE 8. Recommended TS BTL PCB Layout:
Top Silkscreen



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FIGURE 9. Recommended TS BTL PCB Layout:
Top Layer

Demonstration Board Layout (Continued)

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**FIGURE 10. Recommended TS BTL PCB Layout:
Bottom Layer**



TA09A (Rev C)

For Staggered Lead Non-Isolated Package
Order Number LM4950TA
NS Package Number TA09A

Notes

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