

FEATURES

- **1.8V to 5.5V Supply Voltage**
- **Single and Dual Transceivers**
- **High-Speed Operation**
 - 1Mbps for 250pF/3k Ω Load (LTC2802, LTC2804)
 - 250kbps for 1nF/3k Ω Load
 - 100kbps for 2.5nF/3k Ω TIA/EIA-232-F Load
- **Low-Power 1 μ A Shutdown and 15 μ A Receivers-Active Modes**
- No Damage or Latch-Up to ± 10 kV ESD on RS-232 Interface
- Logic Supply Pin for Easy Level-Shifting to UART or Microprocessor
- Low-Latency Output Enable Allows Line Sharing and Half-Duplex Operation
- True RS-232 Compliant Output Levels
- Small Footprint:
 - LTC2801/LTC2802 4mm $\times$ 3mm DFN Package
 - LTC2803/LTC2804 Narrow SSOP-16 and 5mm $\times$ 3mm DFN Packages

APPLICATIONS

- Battery-Powered Systems
- Computers and Consumer Electronics
- Diagnostic Ports

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DESCRIPTION

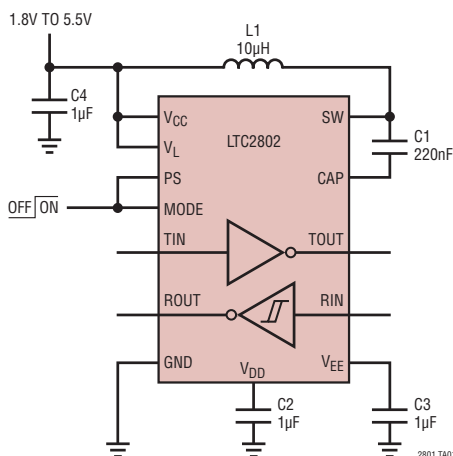
The LTC[®]2801/LTC2802/LTC2803/LTC2804 are single and dual RS-232 transceivers in narrow SSOP and chip-scale DFN packages. All operate over a supply range of 1.8V to 5.5V, which permits operation directly from two alkaline, NiCd or NiMH cells. An integrated DC-to-DC converter generates power supplies for driving RS-232 levels. A logic supply pin allows easy interfacing with different logic levels independent of the DC-DC supply.

These parts are compatible with the TIA/EIA-232-F standard. Driver outputs are protected from overload and can be shorted to ground or up to ± 15 V without damage. To extend battery life, receivers can be kept active, operating at reduced speed, with only 15 μ A current. In shutdown mode, current is further reduced to 1 μ A. Line sharing and half-duplex operation are also supported.

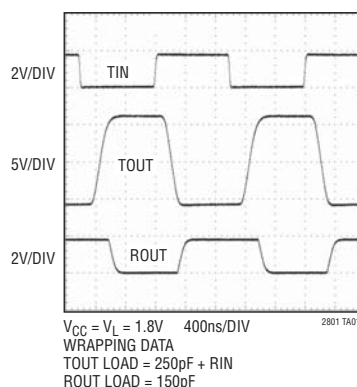
PRODUCT SELECTION GUIDE

PART NUMBER	DRIVERS	RECEIVERS	PACKAGE
LTC2801	1	1	12-Lead DFN
LTC2802	1	1	12-Lead DFN
LTC2803	2	2	16-Lead DFN
LTC2803-1	2	2	16-Lead Narrow SSOP
LTC2804	2	2	16-Lead DFN
LTC2804-1	2	2	16-Lead Narrow SSOP

TYPICAL APPLICATION



LTC2802 at 1.8V and 1Mbps



LTC2801/LTC2802/ LTC2803/LTC2804

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supplies

V_{CC} -0.3V to 7V

V_L -0.3V to 6.7V

Generated Supplies

V_{DD} V_{CC} -0.3V to 7.5V

V_{EE} 0.3V to -7.5V

$V_{DD} - V_{EE}$ 14V

SW -0.3V to $V_{DD} + 0.3V$

CAP +0.3V to $V_{EE} - 0.3V$

TIN, T1IN, T2IN, MODE -0.3V to 7V

PS, ON/OFF -0.3V to ($V_L + 0.3V$)

RIN, R1IN, R2IN -25V to 25V

TOUT, T1OUT, T2OUT -15V to 15V

ROUT, R1OUT, R2OUT -0.3V to ($V_L + 0.3V$)

Operating Temperature

LTC280XC 0°C to 70°C

LTC280XI -40°C to 85°C

Storage Temperature Range -65°C to 125°C

Lead Temperature (Soldering, 10 sec)

GN Package 300°C

PIN CONFIGURATION

1-Driver/1-Receiver	2-Driver/2-Receiver	2-Driver/2-Receiver
TOP VIEW DE PACKAGE 12-LEAD (4mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 43^{\circ}C/W$, $\theta_{JC} = 4.3^{\circ}C/W$ (4 Layer) EXPOSED PAD (PIN 13) IS V_{EE}, MUST BE SOLDERED TO PCB	TOP VIEW DHC PACKAGE 16-LEAD (5mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 44^{\circ}C/W$, $\theta_{JC} = 4.3^{\circ}C/W$ (4 Layer) EXPOSED PAD (PIN 17) IS V_{EE}, MUST BE SOLDERED TO PCB	TOP VIEW GN PACKAGE 16-LEAD (NARROW 0.150) PLASTIC SSOP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 110^{\circ}C/W$, $\theta_{JC} = 40^{\circ}C/W$ (4 Layer)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2801CDE#PBF	LTC2801CDE#TRPBF	2801	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2801IDE#PBF	LTC2801IDE#TRPBF	2801	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2802CDE#PBF	LTC2802CDE#TRPBF	2802	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2802IDE#PBF	LTC2802IDE#TRPBF	2802	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2803CDHC#PBF	LTC2803CDHC#TRPBF	2803	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC2803IDHC#PBF	LTC2803IDHC#TRPBF	2803	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2804CDHC#PBF	LTC2804CDHC#TRPBF	2804	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC2804IDHC#PBF	LTC2804IDHC#TRPBF	2804	16-Lead (5mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2803CGN-1#PBF	LTC2803CGN-1#TRPBF	28031	16-Lead (Narrow 0.150) Plastic SSOP	0°C to 70°C
LTC2803IGN-1#PBF	LTC2803IGN-1#TRPBF	280311	16-Lead (Narrow 0.150) Plastic SSOP	-40°C to 85°C
LTC2804CGN-1#PBF	LTC2804CGN-1#TRPBF	28041	16-Lead (Narrow 0.150) Plastic SSOP	0°C to 70°C
LTC2804IGN-1#PBF	LTC2804IGN-1#TRPBF	280411	16-Lead (Narrow 0.150) Plastic SSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{CC} = 1.8\text{V}$ to 5.5V , $V_L = 1.8\text{V}$ to 5.5V , Normal Mode. Typical values are given for $V_{CC} = V_L = 3.3\text{V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supplies								
I _{CC}	V _{CC} Supply Current	Outputs Unloaded Normal Mode (Note 3) Receivers Active Mode Shutdown Mode			2.3 1 1		10 10	mA μA μA
I _L	V _L Supply Current	Outputs Unloaded Normal Mode (LTC2801, LTC2802) Normal Mode (LTC2803, LTC2804) Receivers Active Mode Shutdown Mode			0.08 0.15 15 1		0.15 0.30 30 10	mA mA μA μA
Driver								
V _{OLD}	Output Voltage	R _L = 3kΩ	Low		−5	−5.7		V
V _{OHD}	Output Voltage	R _L = 3kΩ	High		5	6.2		V
V _{HYS}	Logic Input Hysteresis					0.6		V
I _{OSD}	Output Short Circuit Current	V _L = V _{CC} = 5.5V; V _{TOUT} = 0V			±35		±70	mA
I _{POLD}	Power-Off Output Leakage Current	V _L = V _{CC} = V _{DD} = V _{EE} = 0V; V _{TOUT} = ±2V			±0.1		±10	μA
I _{OLD}	Output Leakage Current	Shutdown or Receivers Active or Drivers Disabled Modes, −15V ≤ V _{TOUT} ≤ 15V			±0.1		±10	μA
Receiver								
V _{IR}	Input Thresholds	Receivers Active Mode			0.8	1.5	2.4	V
V _{ILR}	Input Thresholds	Normal Mode, Input Low			0.8	1.3		V
V _{IHR}	Input Thresholds	Normal Mode, Input High				1.7	2.5	V
V _{HYSR}	Input Hysteresis	Normal Mode			0.1	0.4	1.0	V
V _{OLR}	Output Voltage	Output Low, I _{ROUT} = 1mA (Sinking)				0.2	0.4	V
V _{OHR}	Output Voltage	Output High, I _{ROUT} = −1mA (Sourcing)		V _L − 0.4		V _L − 0.2		V
R _{IN}	Input Resistance	−15V ≤ V _{RIN} ≤ 15V			3	5	7	kΩ
I _{OSR}	Output Short Circuit Current	V _L = 5.5V; 0V ≤ V _{ROUT} ≤ V _L				±25	±50	mA
Logic								
	Logic Input Voltage Threshold				0.4		0.67 • V _L	V
I _{IN}	Logic Input Current						±1	μA
Power Supply Generator								
V _{DD}	Regulated V _{DD} Output Voltage	Driver R _L = 3kΩ (Note 3) LTC2801, LTC2802: V _{TIN} = V _L LTC2803, LTC2804: V _{T1IN} = V _L , V _{T2IN} = 0V				7		V
V _{EE}	Regulated V _{EE} Output Voltage	Driver R _L = 3kΩ (Note 3) LTC2801, LTC2802: V _{TIN} = V _L LTC2803, LTC2804: V _{T1IN} = V _L , V _{T2IN} = 0V				−6.3		V

LTC2801/LTC2802/ LTC2803/LTC2804

SWITCHING CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{CC} = 1.8\text{V}$ to 5.5V , $V_L = 1.8\text{V}$ to 5.5V , Normal Mode. Typical values are given for $V_{CC} = V_L = 3.3\text{V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Maximum Data Rate	LTC2801, LTC2803 (Note 3)				
		$R_L = 3\text{k}\Omega$, $C_L = 2.5\text{nF}$	●	100		kbps
		$R_L = 3\text{k}\Omega$, $C_L = 1\text{nF}$	●	250		kbps
		LTC2802, LTC2804 (Note 3)				
		$R_L = 3\text{k}\Omega$, $C_L = 2.5\text{nF}$	●	100		kbps
		$R_L = 3\text{k}\Omega$, $C_L = 1\text{nF}$	●	250		kbps
		$R_L = 3\text{k}\Omega$, $C_L = 250\text{pF}$	●	1000		kbps

Driver

SR(D)	Driver Slew Rate	LTC2801, LTC2803 (Figure 1)				
		$V_{CC} = V_L = 1.8\text{V}$, $R_L = 3\text{k}\Omega$, $C_L = 2.5\text{nF}$	●	4		V/ μs
		$V_{CC} = V_L = 5.5\text{V}$, $R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$	●		30	V/ μs
		LTC2802, LTC2804 (Figure 1)				
		$V_{CC} = V_L = 1.8\text{V}$, $R_L = 3\text{k}\Omega$, $C_L = 2.5\text{nF}$	●	4		V/ μs
		$V_{CC} = V_L = 5.5\text{V}$, $R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$	●		150	V/ μs
t_{PHLD} , t_{PLHD}	Driver Propagation Delay	$R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$ (Figure 2)				
		LTC2801, LTC2803	●	1	2	μs
		LTC2802, LTC2804	●	0.2	0.5	μs
t_{SKEWD}	Driver Skew	$R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$ (Figure 2)				
		LTC2801, LTC2803		100		ns
		LTC2802, LTC2804		50		ns
t_{PZHD} , t_{PZLD}	Driver Output Enable Time	$PS = V_L$, $MODE = \uparrow$, $R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$ (Figure 4)	●	0.6	2	μs
t_{PHZD} , t_{PLZD}	Driver Output Disable Time	$PS = V_L$, $MODE = \downarrow$, $R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$ (Figure 4)	●	0.3	2	μs

Receiver

t_{PHLR} , t_{PLHR}	Receiver Propagation Delay	$C_L = 150\text{pF}$ (Figure 3)	●	0.2	0.4	μs
t_{SKEWR}	Receiver Skew	$C_L = 150\text{pF}$ (Figure 3)		50		ns
t_{RR} , t_{FR}	Receiver Rise or Fall Time	$C_L = 150\text{pF}$ (Figure 3)	●	60	200	ns
t_{PZHR} , t_{PZLR}	Shutdown to Receiver Output Enable	$PS = MODE = \uparrow$ or $ON/\overline{OFF} = \uparrow$, $R_L = 1\text{k}\Omega$, $C_L = 150\text{pF}$ (Figure 5)	●	5	15	μs
t_{PHZR} , t_{PLZR}	Receiver Output Disable upon Shutdown	$PS = MODE = \downarrow$ or $ON/\overline{OFF} = \downarrow$, $R_L = 1\text{k}\Omega$, $C_L = 150\text{pF}$ (Figure 5)	●	0.15	0.3	μs

Power Supply Generator

	V_{DD}/V_{EE} Supply Rise Time	(Notes 3 and 4)	●	0.2	2	ms
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Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: Guaranteed by other measured parameters and not tested directly.

Note 4: Time from $PS \uparrow$ or $ON/\overline{OFF} \uparrow$ until $V_{DD} \geq 5\text{V}$ and $V_{EE} \leq -5\text{V}$.

TEST CIRCUITS

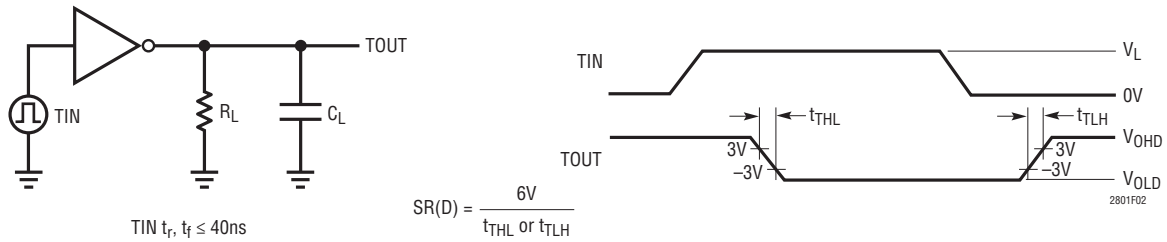


Figure 1. Driver Slew Rate Measurement

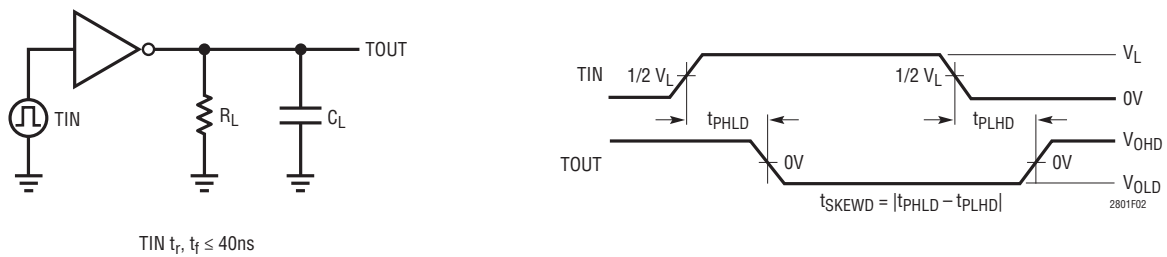


Figure 2. Driver Timing Measurement

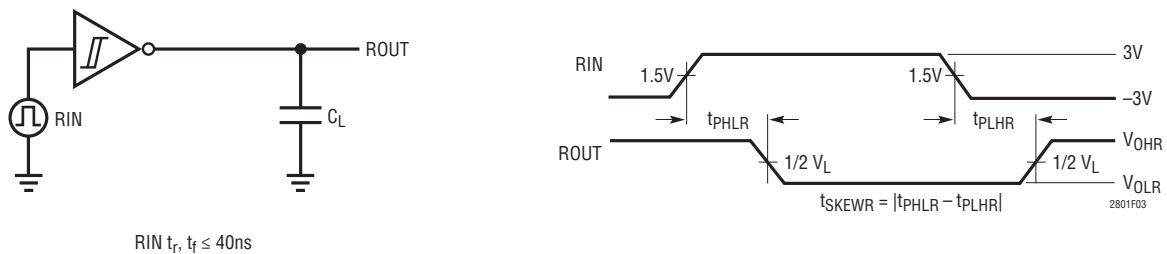


Figure 3. Receiver Timing Measurement

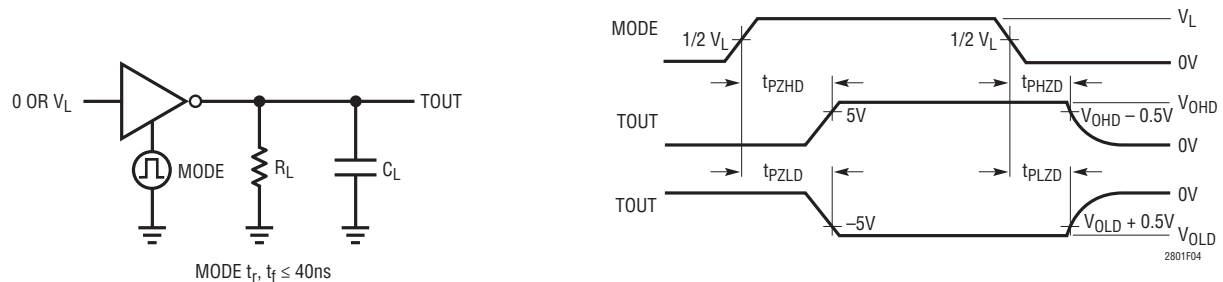


Figure 4. Driver Enable/Disable Times

LTC2801/LTC2802/ LTC2803/LTC2804

TEST CIRCUITS

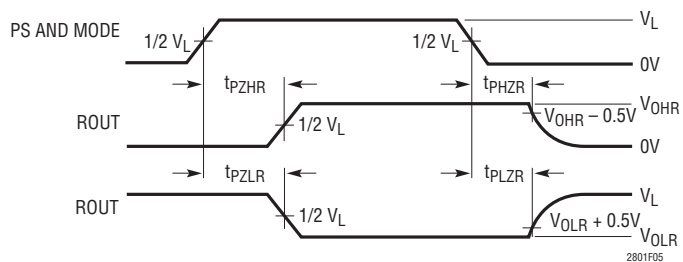
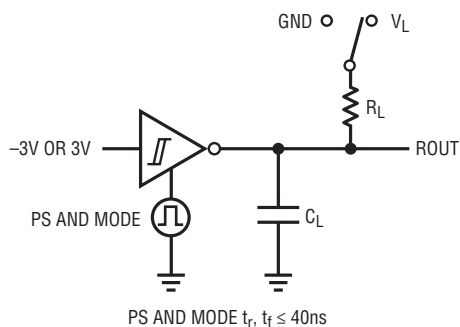
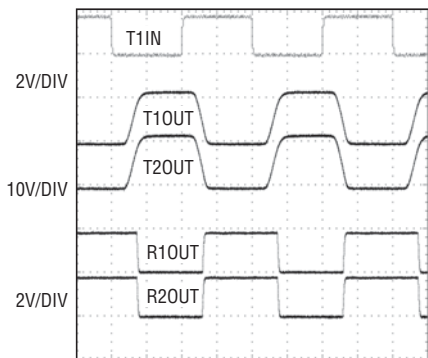


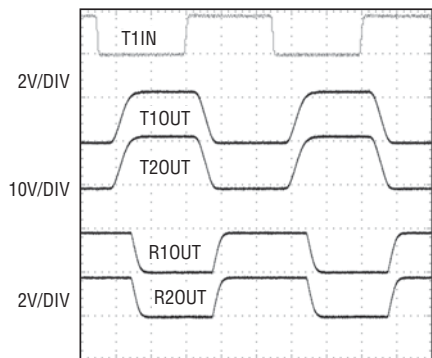
Figure 5. Receiver Enable/Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted.

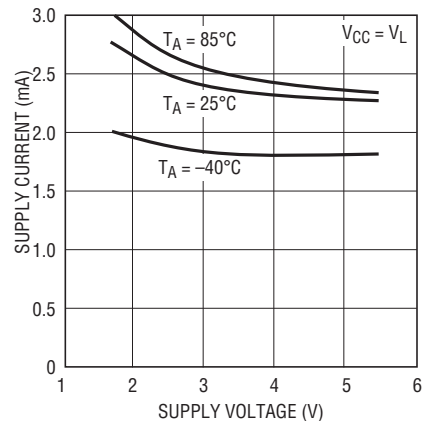
LTC2803 at 1.8V and 250kbps



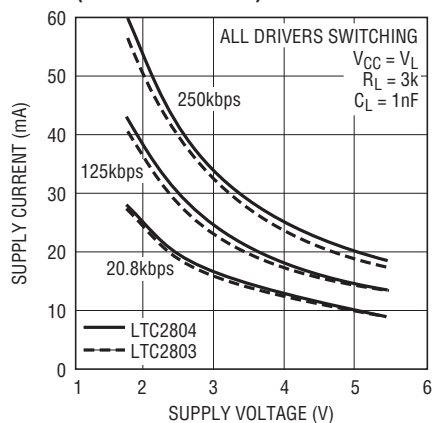
LTC2804 at 1.8V and 1Mbps



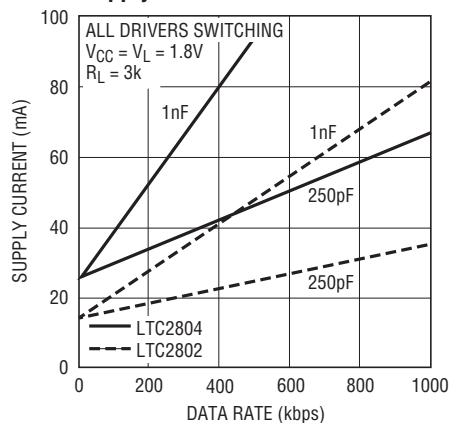
Drivers Disabled Mode Supply Current vs Supply Voltage



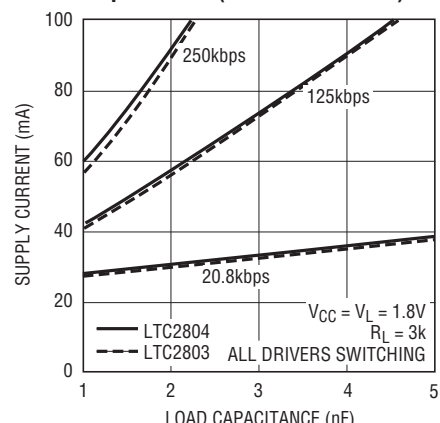
Supply Current vs Supply Voltage (Dual Transceiver)



Supply Current vs Data Rate

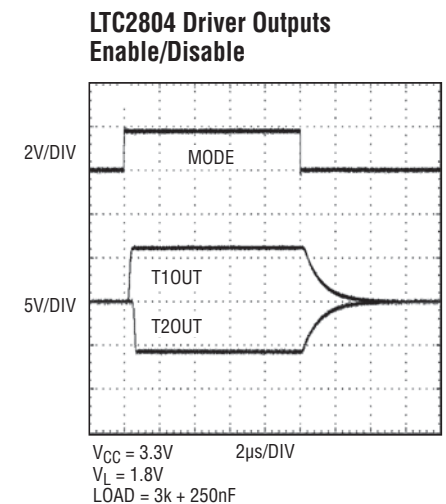
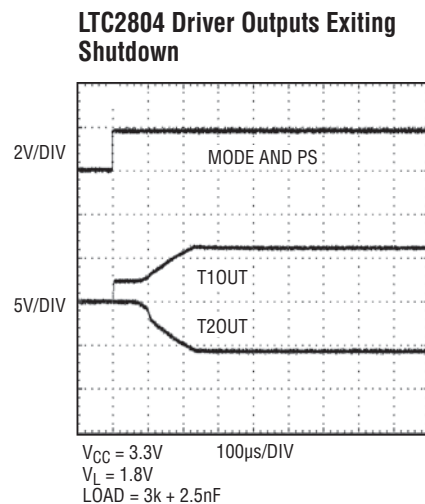
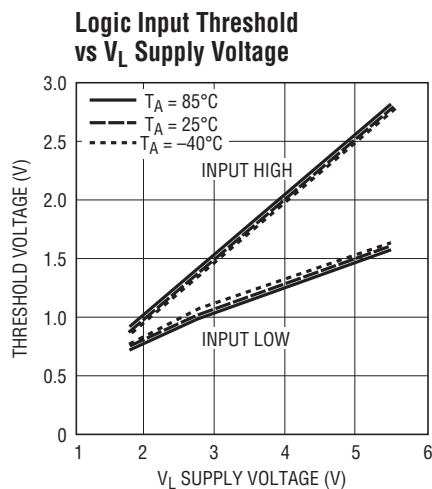
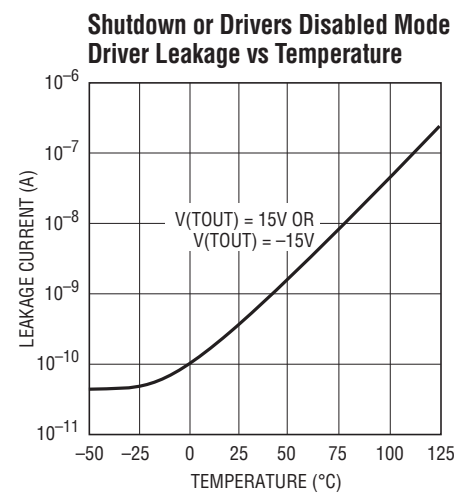
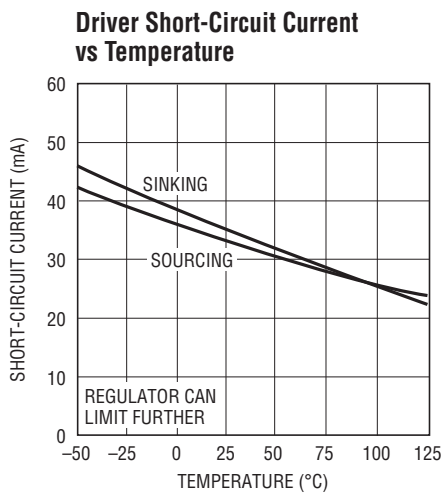
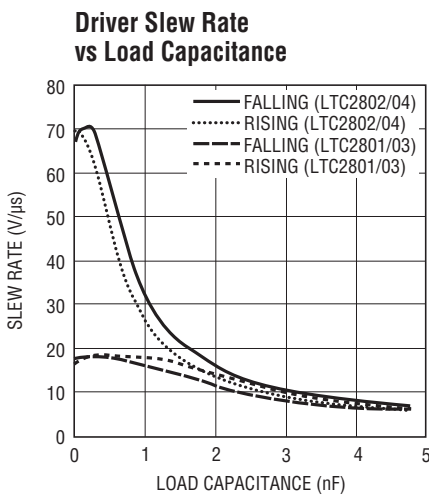
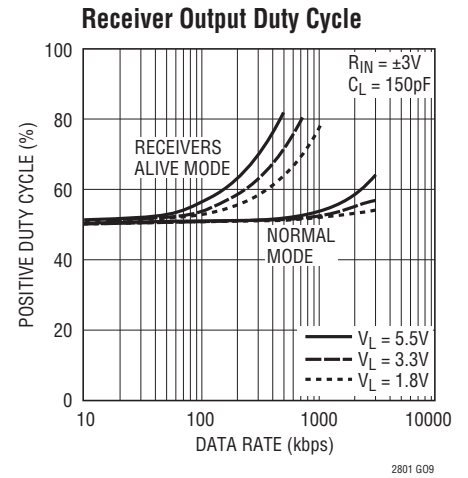
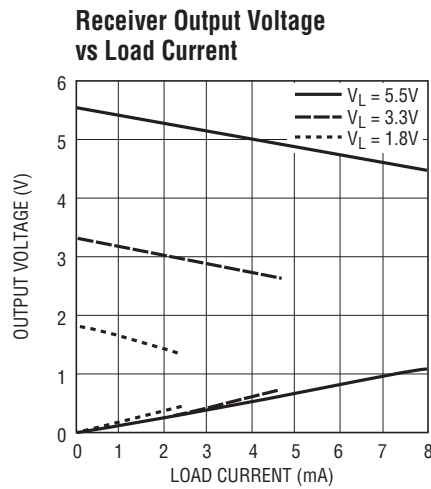
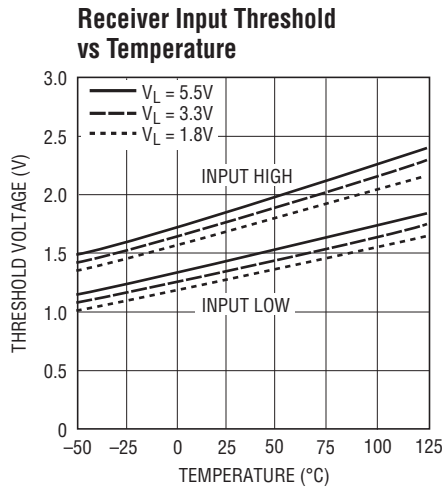


Supply Current vs Load Capacitance (Dual Transceiver)



TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = V_L = 3.3\text{V}$ unless otherwise noted.



LTC2801/LTC2802/ LTC2803/LTC2804

PIN FUNCTIONS

PIN NAME	PIN NUMBER			COMMENTS
	2801 2802	2803 2804	2803-1 2804-1	
V _{CC}	3	5	5	Input Supply (1.8V-5.5V). Bypass to GND with a 1μF capacitor.
V _{DD}	4	6	6	Generated Positive Supply Voltage for RS-232 Driver (7V). Connect a 1μF capacitor between V _{DD} and GND.
V _{EE}	13*	17*	9	Generated Negative Supply Voltage for RS-232 Driver (–6.3V). Connect a 1μF capacitor between V _{EE} and GND.
SW	5	7	7	Switch Pin. Connect a 10μH inductor between SW and V _{CC} .
GND	6	8	8	Ground.
CAP	7	9	10	Charge Pump Capacitor for Generated Negative Supply Voltage. Connect a 220nF capacitor between CAP and SW.
V _L	10	12	12	Logic Supply (1.8V-5.5V) for the receiver outputs, driver inputs, and control inputs. This pin should be bypassed to GND with a 220nF capacitor if it's not tied to V _{CC} .
TIN (T1IN, T2IN)	11	14, 13	14, 13	Driver Input(s), referenced to V _L .
TOUT (T1OUT, T2OUT)	2	3, 4	3, 4	RS-232 Driver Output(s).
RIN (R1IN, R2IN)	1	1, 2	1, 2	RS-232 Receiver Input(s). Includes internal 5kΩ termination resistor(s).
ROUT (R1OUT, R2OUT)	12	16, 15	16, 15	Receiver Output(s), referenced to V _L . Output is short-circuit protected to GND/V _{CC} /V _L , and is high impedance in Shutdown mode, allowing data line sharing.
PS	8	10	—	Power Supply control pin, referenced to V _L . Enables the integrated DC-DC converter.
MODE	9	11	—	Mode control pin, referenced to V _L . See Table 1 for functionality.
ON/OFF	—	—	11	Transceiver enable pin, referenced to V _L . A logic low puts the device in Shutdown mode and places both driver and receiver outputs in a high impedance state.

*Backside thermal pad

MODE CONTROL

Table 1. LTC2801-LTC2804

MODE NAME	PS	MODE	RECEIVER OUTPUT(S)	DC-DC	DRIVER OUTPUT(S)	I _{VCC} *	I _{VL} *
SHUTDOWN	L	L	HI-Z	OFF	HI-Z	1μA	1μA
RECEIVERS ACTIVE	L	H	ON	OFF	HI-Z	1μA	15μA
DRIVERS DISABLED	H	L	ON	ON	HI-Z	2.1mA	80μA OR 150μA
NORMAL	H	H	ON	ON	ON	2.3mA	80μA OR 150μA

Table 2. LTC2803-1, LTC2804-1

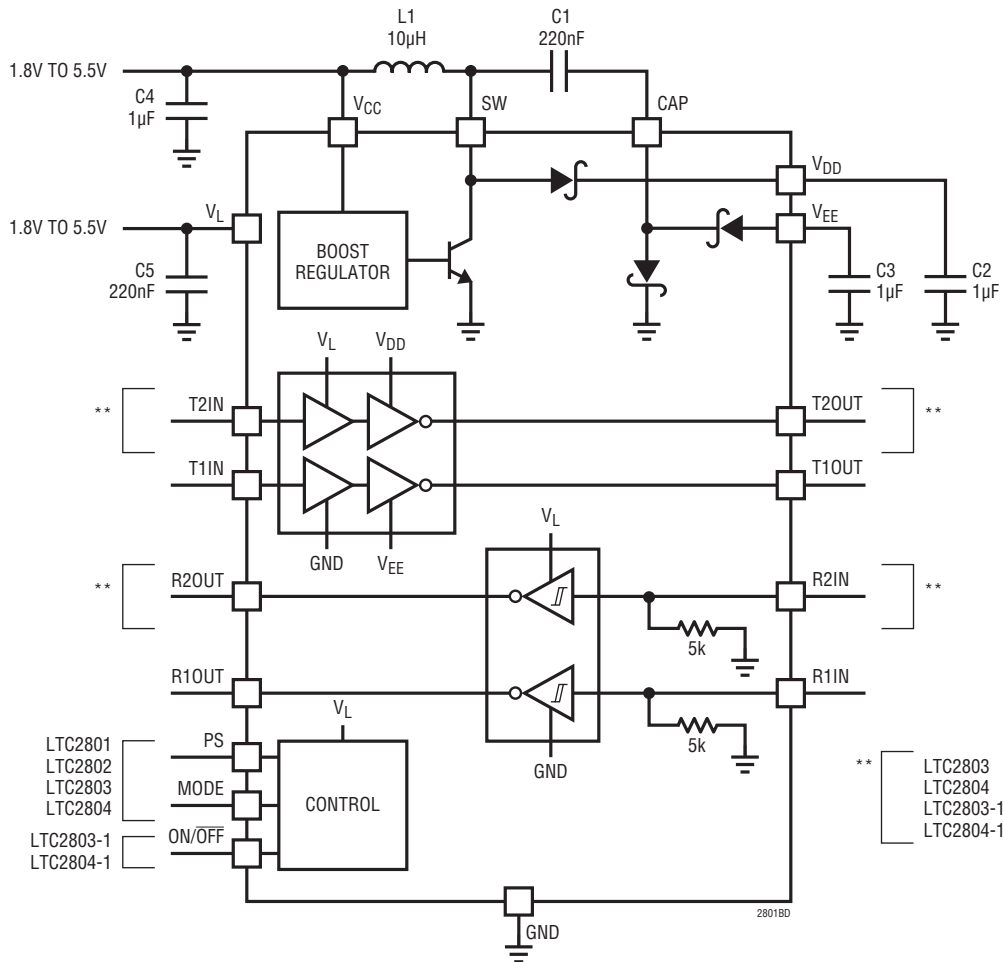
MODE NAME	ON/OFF	RECEIVER OUTPUTS	DC-DC	DRIVER OUTPUTS	I _{VCC} *	I _{VL} *
SHUTDOWN	L	HI-Z	OFF	HI-Z	1μA	1μA
NORMAL	H	ON	ON	ON	2.3mA	150μA

*Typical currents for static drivers. Normal mode currents are for unloaded outputs.

FEATURE SUMMARY

FEATURE	2801	2802	2803	2803-1	2804	2804-1
DRIVERS and RECEIVERS	1 + 1	1 + 1	2 + 2	2 + 2	2 + 2	2 + 2
PACKAGE	DE	DE	DHC	GN	DHC	GN
1.8V - 5.5V OPERATION	•	•	•	•	•	•
1.8V - 5.5V LOGIC SUPPLY (V_L)	•	•	•	•	•	•
SHUTDOWN ($1\mu A$)	•	•	•	•	•	•
RECEIVER(S) ACTIVE ($15\mu A$)	•	•	•	•	•	•
DRIVER DISABLE	•	•	•	•	•	•
100kb/s for $R_L = 3k\Omega$, $C_L = 2.5nF$	•	•	•	•	•	•
250kb/s for $R_L = 3k\Omega$, $C_L = 1nF$	•	•	•	•	•	•
1Mb/s for $R_L = 3k\Omega$, $C_L = 250pF$	•	•	•	•	•	•

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTC2801 family of RS-232 transceivers operates on a V_{CC} supply of 1.8V to 5.5V, utilizing a switching regulator to generate the necessary higher voltage rails for the drivers. The transceivers interface with logic operating on any supply from 1.8V to 5.5V, independent of the V_{CC} voltage. Depending on the device, one or two control pins are available to invoke Shutdown, Receiver Active and Driver Disable features.

DC-DC Converter

The on-chip DC-DC converter operates from the V_{CC} input, generating a 7V V_{DD} supply and a charge pumped $-6.3V$ V_{EE} supply, as shown in Figure 6. V_{DD} and V_{EE} power the output stage of the drivers and are regulated to levels that guarantee greater than $\pm 5V$ output swing. The DC-DC converter requires a 10 μH inductor (L1) and a bypass capacitor (C4) of at least 1 μF . The recommended size for the charge pump capacitor (C1) is 220nF and for the storage capacitors (C2 and C3) is 1 μF . Larger storage capacitors up to 4.7 μF may be used if C1 is kept at 20% to 50% their size and C4 is also scaled. Locate C1-C4 close to their associated pins.

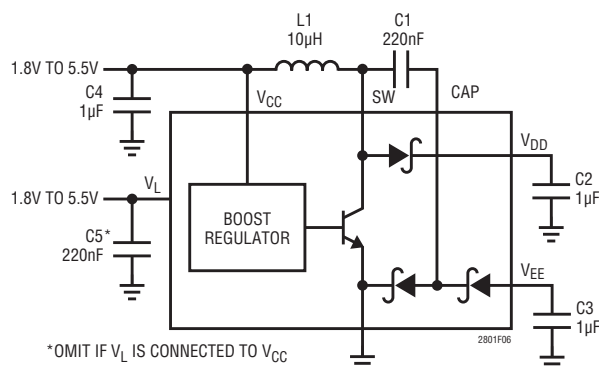


Figure 6. DC/DC Converter and Recommended Bypassing

V_L Logic Supply

A separate logic supply pin V_L allows the LTC2801 family to interface with any logic signal from 1.8V to 5.5V, as shown in Figure 7. Simply connect the desired logic supply to V_L . There is no interdependency between V_{CC} and V_L ; they may simultaneously operate at any voltage from 1.8V to 5.5V and sequence in any order. If V_L is powered separately from V_{CC} , bypass V_L with a 220nF capacitor (C5).

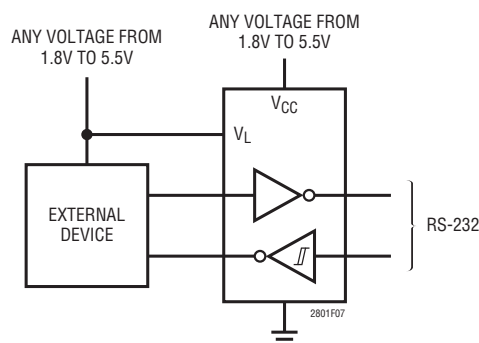


Figure 7. V_{CC} and V_L Are Independent

Power-Saving Modes

When the DC-DC converter and drivers are turned off (PS or ON/OFF = logic low), V_{CC} supply current is reduced to 1 μA . Tables 1 and 2 summarize the modes for each device.

In Shutdown mode, V_L supply current is reduced to 1 μA , and both receiver and driver outputs assume a high impedance state.

In Receivers Active mode, the quiescent V_L supply current is reduced to 15 μA and the driver outputs assume a high impedance state. The receivers operate at a reduced rate (typically 100 kbps) with hysteresis turned off.

Half-Duplex Operation

When the DC-DC converter is kept on (PS = logic high), MODE serves as a low-latency driver enable for half-duplex operation. Each driver is enabled and disabled in less than 2 μs , while each receiver remains continuously active. This mode of operation is illustrated in Figures 15-17.

Battery Operation

To maximize battery life, connect V_{CC} (and L1) directly to the unregulated battery voltage and V_L to the regulated supply, as shown in Figure 22. This configuration typically minimizes conversion loss while providing compatibility with system logic levels.

Inductor Selection

A 10 μH inductor with a saturation current (I_{SAT}) rating of at least 200mA and low DCR (copper wire resistance) is recommended. Some small inductors meeting these requirements are listed in Table 3.

APPLICATIONS INFORMATION

Table 3. Recommended Inductors

PART NUMBER	I _{SAT} (mA)	MAX DCR (Ω)	SIZE (mm)	MANUFACTURER
LQH2MCN100K02L	225	1.2	2 × 1.6 × 0.95	Murata www.murata.com
LBC2016T100K	245	0.85	2 × 1.6 × 1.6	Taiyo Yuden www.t-yuden.com
FSLB2520-100K	220	1.1	2.5 × 2 × 1.6	Toko www.tokoam.com

Capacitor Selection

The small size of ceramic capacitors makes them ideal for the LTC2801 family. X5R and X7R (preferred) types are recommended because their ESR is low and they retain their capacitance over relatively wide voltage and temperature ranges. Use a voltage rating of at least 10V.

Table 4. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	URL
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Kemet	www.kemet.com

Inrush Current and Supply Overshoot Precaution

In certain applications, such as battery-operated and wall-adaptor devices, fast supply slew rates are generated when power is connected. If V_{CC}'s voltage is greater than 4.5V and its rise time is faster than 10μs, the pins V_{DD} and SW can exceed their ABS MAX values during start-up. When supply voltage is applied to V_{CC}, the voltage difference between V_{CC} and V_{DD} generates inrush current

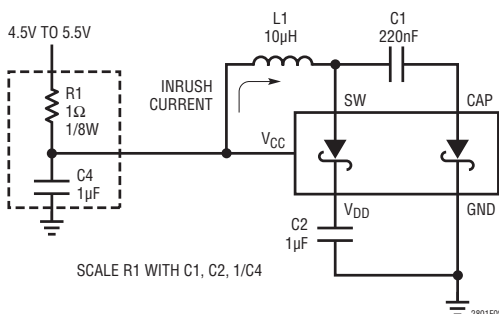


Figure 8. Supply Overshoot Protection for Input Supplies of 4.5V or Higher

flowing through inductor L1 and capacitors C1, C2. The peak inrush current must not exceed 2A. To avoid this condition, add a 1Ω resistor as shown in Figure 8. This precaution is not relevant for supply voltages below 4.5V or rise times longer than 10μs.

Board Layout

The board layout should minimize the length and area of the SW and CAP traces. Suggested compact layouts for the LTC2801 family are shown in Figure 9 (a) and (b).

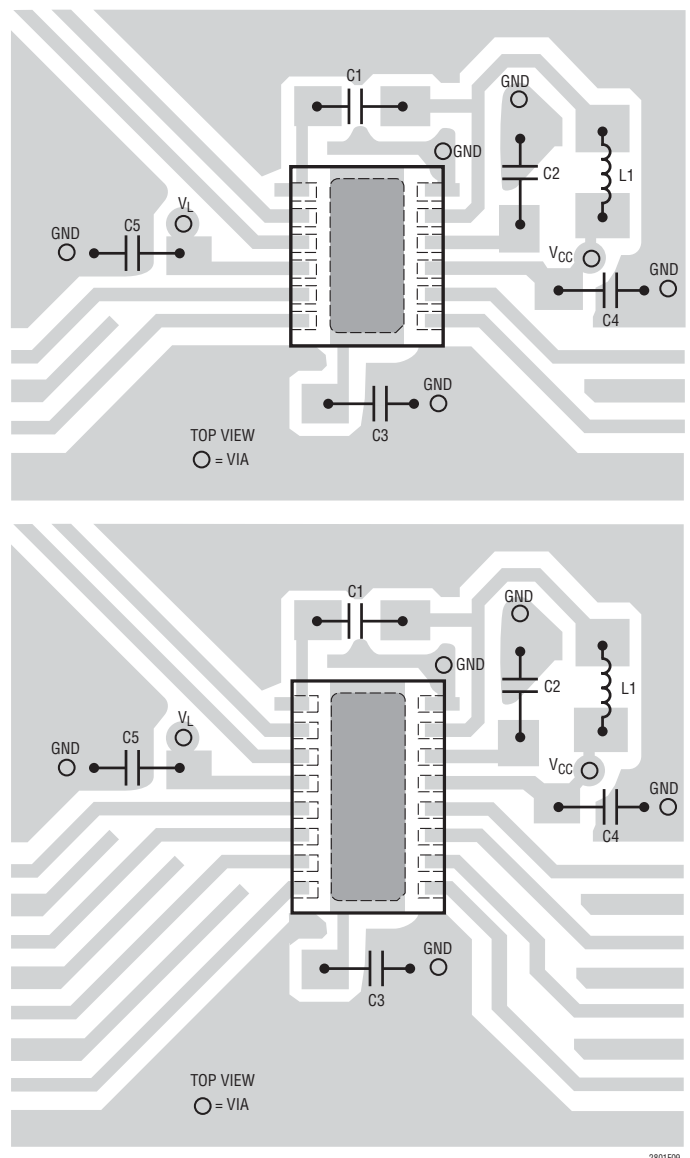


Figure 9. Recommended Board Layouts for (a) Single and (b) Dual Transceiver Parts

2801234fc

TYPICAL APPLICATIONS

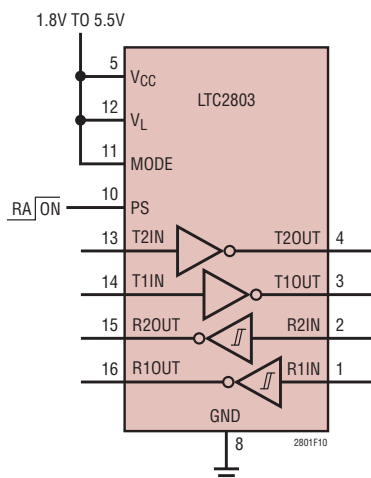


Figure 10. Power-Saving Receivers-Active Mode

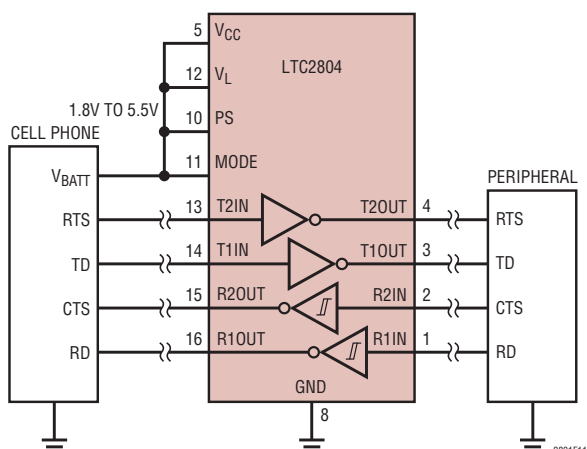


Figure 11. Cellphone Peripheral Interface

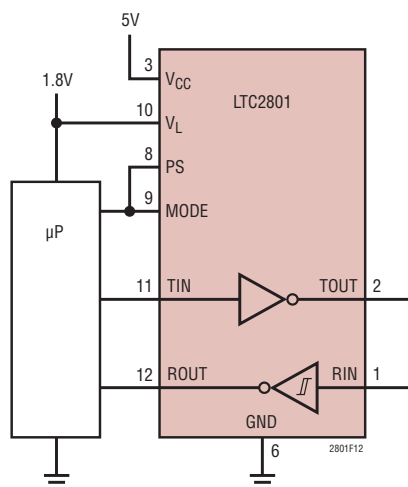


Figure 12. 1.8V Microprocessor Interface

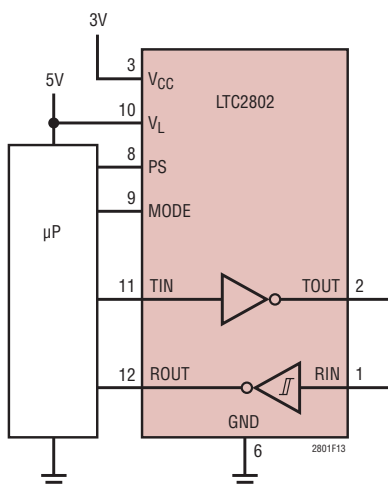


Figure 13. 5V Microprocessor Interface

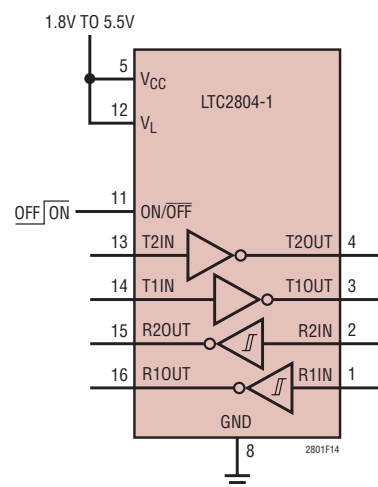


Figure 14. Power-Saving Shutdown Mode

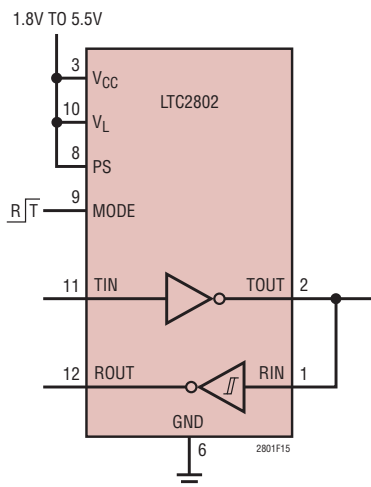


Figure 15. Half-Duplex on Single Line, Separate ROUT, TIN

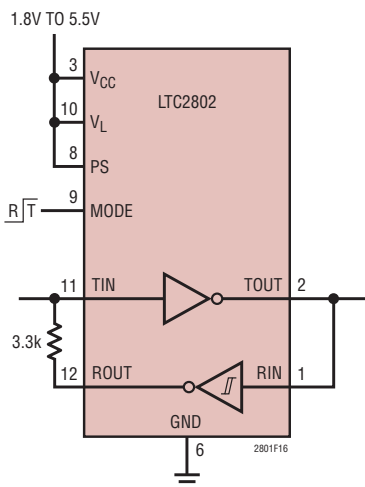


Figure 16. Half-Duplex on Single Line

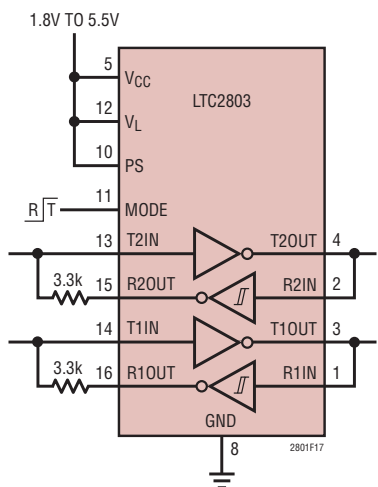
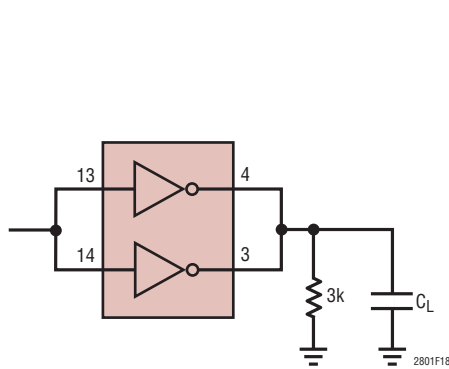


Figure 17. Half-Duplex Dual Transceiver

TYPICAL APPLICATIONS



DATA RATE (kbps)	C_L (nF)	LTC2803	LTC2804
100	5	X	X
250	2	X	X
1000	0.5	X	X

Figure 18. Driving Larger Loads

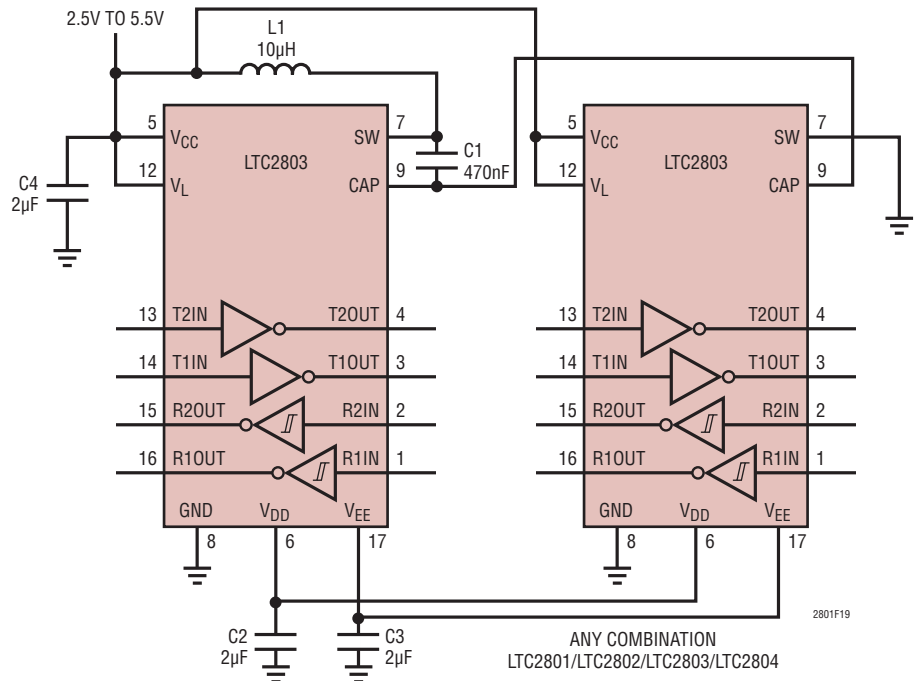
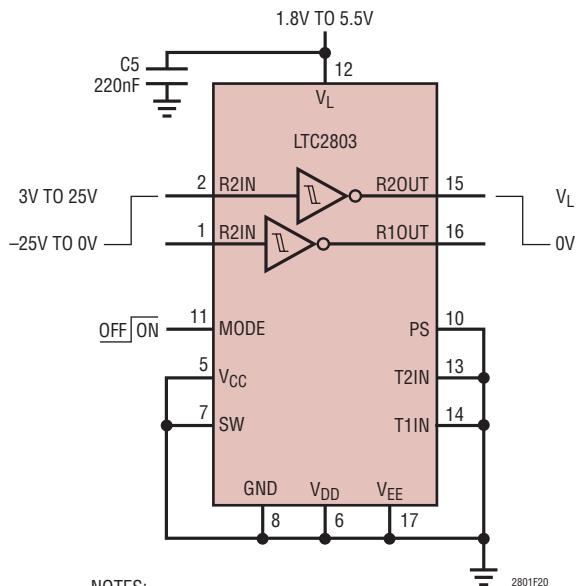


Figure 19. Quad Transceiver ($2.5V < V_{CC} < 5.5V$)



- NOTES:
1. NO L1 OR C2-C4 NEEDED.
 2. RECEIVERS ACTIVE MODE SHOWN HAS NO DC HYSTERESIS.
 3. SEE DUTY CYCLE GRAPH IN TYPICAL PERFORMANCE SECTION.

Figure 20. 100kbps Dual Inverting Level Translator
($I_L = 15\mu A$ Static)

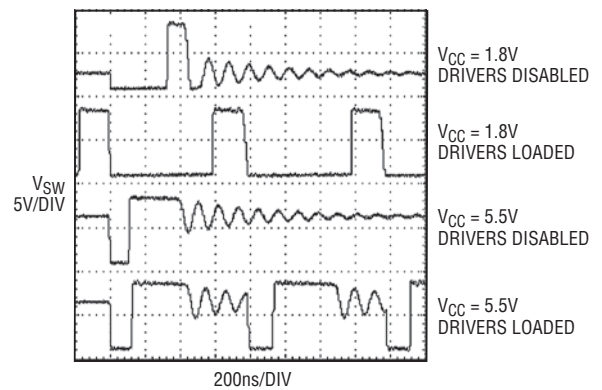
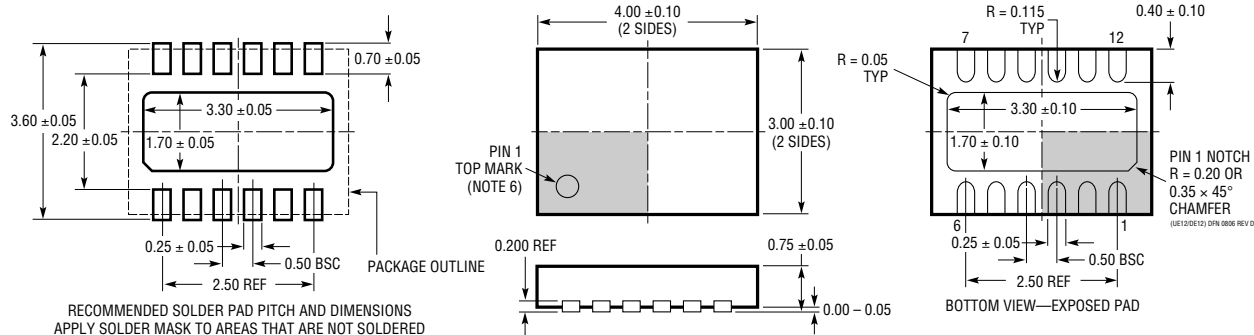


Figure 21. Typical SW Pin Waveforms

TYPICAL APPLICATIONS

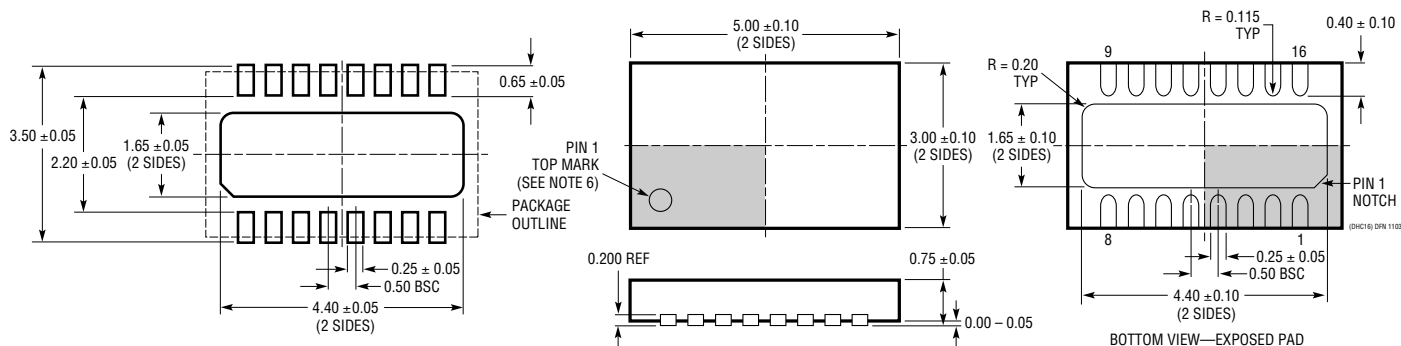
DE/UE Package 12-Lead Plastic DFN (4mm × 3mm) (Reference LTC DWG # 05-08-1695 Rev D)



NOTE:

1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

DHC Package 16-Lead Plastic DFN (5mm × 3mm) (Reference LTC DWG # 05-08-1706)

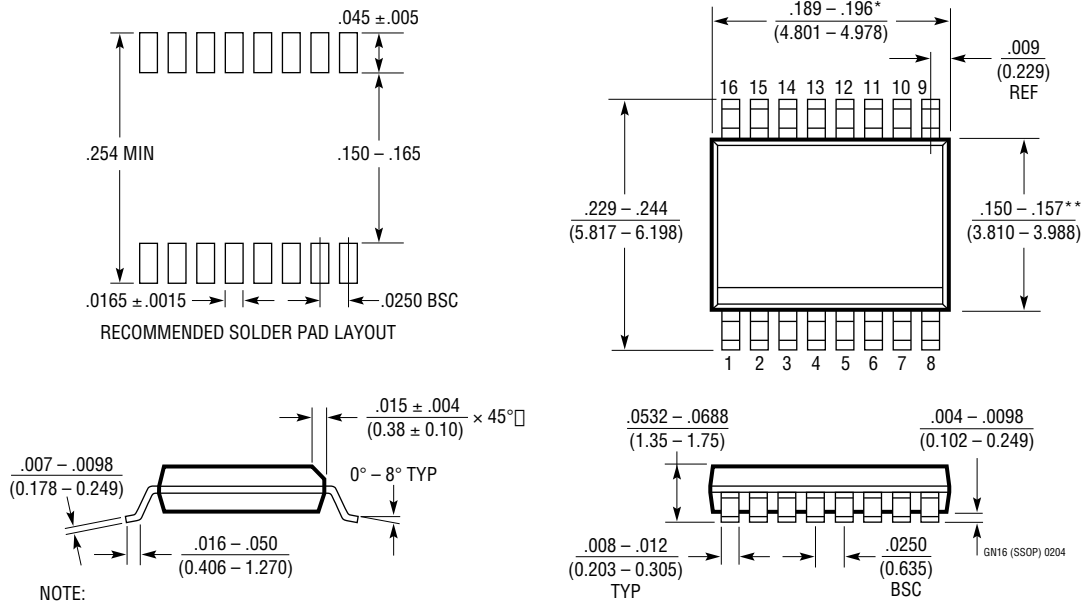


NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES

2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

3. DRAWING NOT TO SCALE

DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006^ (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010^* (0.254mm) PER SIDE

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1780/LT1781	2-Driver/2-Receiver RS232 Transceiver	Single 5V Supply with 0.1μF Capacitors, 15kV ESD
LTC1337	3-Driver/5-Receiver RS232 Transceiver	Ultralow Power for DTE Applications
LTC1338	5-Driver/3-Receiver RS232 Transceiver	Ultralow Power for DCE Applications
LT1039/LT1039-16	3-Driver/3-Receiver RS232 Transceiver	30kΩ Input Impedance for Multi-Drop Applications
LTC1348	3-Driver/5-Receiver RS232 Transceiver	True RS232 Levels on 3.3V Supply