TOSHIBA

TOSHIBA Original CMOS 32-Bit Microcontroller

TLCS-900/H1 Series

TMP92C820

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = (INT0 to INT3, INTKEY, INTRTC, INTALM0 to INTALM4), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

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CMOS 32-bit Microcontrollers
TMP92C820FG/JTMP92C820

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1. Outline and Device Characteristics

TMP92C820 is high-speed advanced 32-bit micro-controller developed for controlling equipment which processes mass data.

TMP92C820 is a micro-controller which has a high-performance CPU (900/H1 CPU) and various built-in I/Os. TMP92C820FG is housed in a 144-pin flat package. JTMP92C820 is a 144-pad chip product.

Device characteristics are as follows:

(1) CPU: 32-bit CPU (900/H1 CPU)

- Compatible with TLCS-900, 900/L, 900/L1, 900/H's instruction code

- 16 Mbytes of linear address space

- General-purpose register and register banks

- Micro DMA: 8 channels (250 ns/4 bytes at fc = 20 MHz, best case)

(2) Minimum instruction execution time: 50 ns (at 20 MHz)

(3) Internal memory

- Internal RAM: 8 Kbytes (can use for code section)

- Internal ROM: None

(4) External memory expansion

- Expandable up to 136 Mbytes (Shared with program/data area)

- Can simultaneously support 8-/16-/32-bit width external data bus
    .... Dynamic data bus sizing

- Separate bus system

(5) Memory controller

- Chip select outputs: 4 channels

(6) 8-bit timers: 4 channels

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

(7) 16-bit timer/event counter: 1 channel

(8) General-purpose serial interface: 3 channels
- UART/synchronous mode
- IrDA

(9) Serial bus interface: 1 channel
- I²C bus mode
- Clock synchronous select mode

(10) LCD controller
- Shift register/built-in RAM LCD driver
- Supported 16, 8 and 4 Gray-levels and black and white
- Hardware blinking cursor

(11) SDRAM controller
- Supported 16-M, 64-M and 128-Mbit SDRAM with 16-/32-bit data bus

(12) Timer for real-time clock (RTC)
- Based on TC8521A
- Separate the power supply

(13) Key-on wakeup (Interrupt key input)

(14) 10-bit AD converter: 5 channels

(15) Watchdog timer

(16) Melody/alarm generator
- Melody: Output of clock 4 to 5461 Hz
- Alarm: Output of the 8 kinds of alarm pattern
- Output of the 5 kinds of interval interrupt

(17) MMU
- Expandable up to 136 Mbytes (4 local areas/8 bank methods)

(18) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 31 internal interrupts: Seven selectable priority levels
- 5 external interrupts: Seven selectable priority levels (4-edge selectable)

(19) Input/output ports: 61 pins (@ external 32-bit data bus memory)

(20) Standby function
- Three HALT modes: IDLE2 (Programmable), IDLE1, STOP

(21) Triple-clock controller
- Clock gear function: Select a high-frequency clock fc to fc/16
- RTC (fs = 32.768 kHz)

(22) Operating voltage
- DVCC = 3.0 to 3.6 V
- RTCVCC = 2.0 to 3.6 V

(23) Package
- 144-pin QFP (P-LQFP144-1616-0.40C)
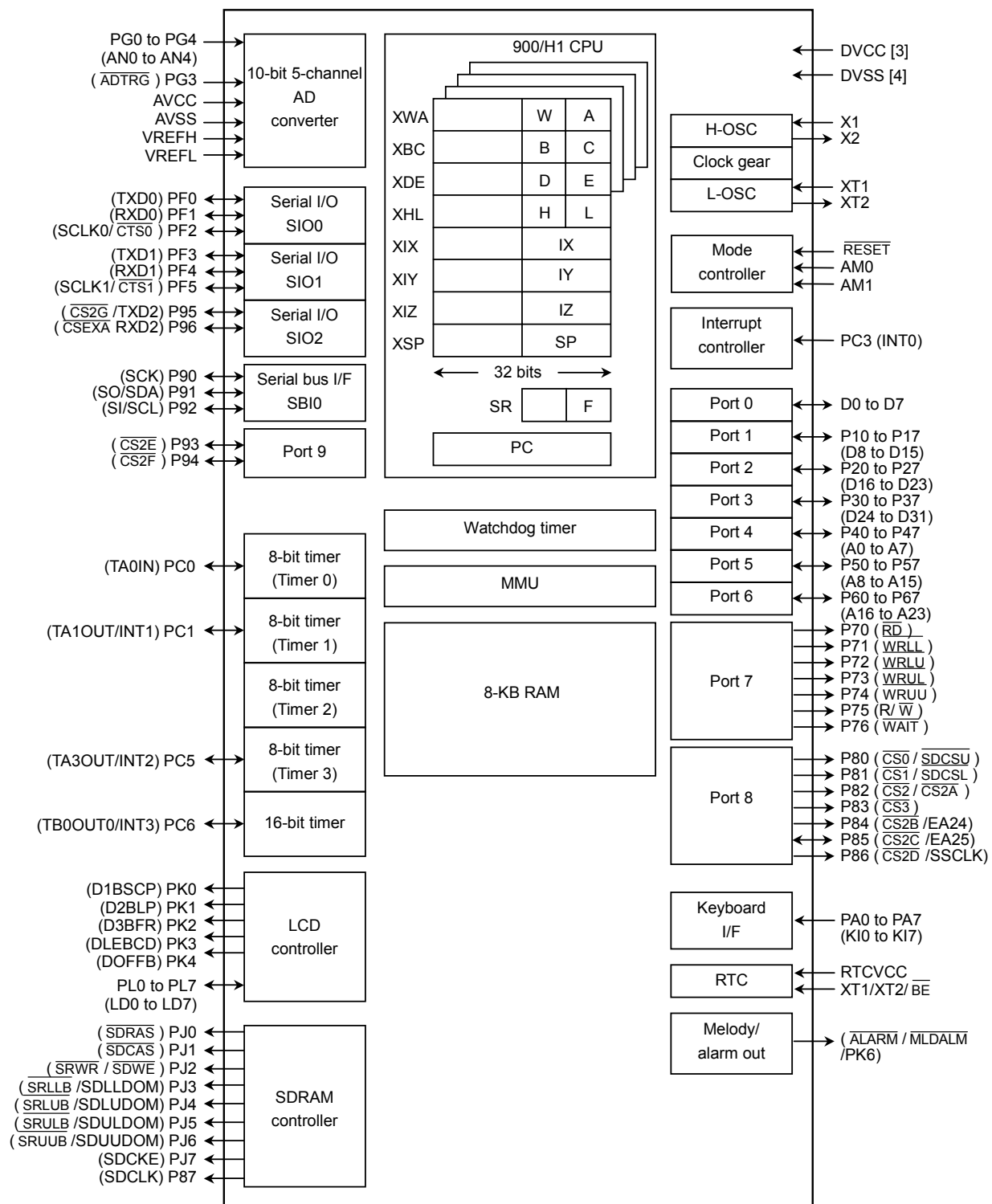- Chip form supply also available. For details, contact your local Toshiba sales representative

Figure 1.1.1 TMP92C820 Block Diagram