

# STS1DN45K3

# Dual N-channel 450 V, 3.2 Ω, 0.5 A SuperMESH3<sup>TM</sup> Power MOSFET in SO-8

Preliminary data

### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>w</sub>
STS1DN45K3	450 V	< 3.8 Ω	0.5 A	1.7 W

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance

### **Application**

■ Switching applications

### **Description**

SuperMESH3™ is a new Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

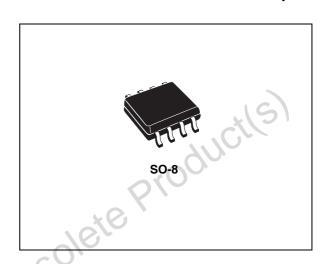


Figure 1. Internal schematic diagram

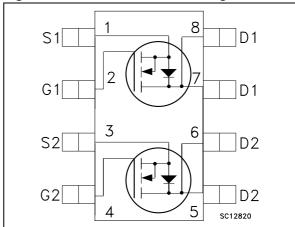


Table 1. Device summary

Order codes	Marking	Packages	Packaging	
STS1DN45K3	STS1DN45K3 1II45		Tape and reel	

Contents STS1DN45K3

### **Contents**

1	Electrical ratings 3
2	Electrical characteristics 4
3	Test circuits 6
4	Package mechanical data
5	Revision history
	Obsolete ,
	productis
0050	Electrical characteristics

**47/** 

STS1DN45K3 **Electrical ratings** 

#### **Electrical ratings** 1

Table 2. **Absolute maximum ratings** 

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage (V <sub>GS</sub> = 0)	450	V
V <sub>GS</sub>	Gate-source voltage	± 30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	0.5	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	0.32	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	2	Α
D	Total dissipation at T <sub>C</sub> = 25 °C (dual operation)	1.7	W
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C (single operation)	1.3	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by $\mathbf{T}_{\mathbf{j}}$ max)	0.5	Α
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j = 25^{\circ}C$ , $I_D = I_{AR}$ , $V_{DD} = 50 \text{ V}$ )	TBD	mJ
dv/dt (2)	Peak diode recovery voltage slope	TBD	V/ns
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C
T <sub>j</sub>	Max. operating junction temperature	150	°C

Pulse width limited by safe operating area

Table 3. Thermal data

Sy	mbol	Parameter	Value	Unit
P	(1)	Thermal resistance junction-amb max (single operation)	62.5	°C/W
\tag{\tau_thj}	R <sub>thj-amb</sub> <sup>(1)</sup>	Thermal resistance junction-amb max (dual operation)	78	°C/W
0050 1. V	When mo	ounted on FR4 board (steady state)		

<sup>2.</sup>  $I_{SD} \leq 0.5 \text{ A, di/dt} \leq \text{TBD A/}\mu\text{s, V}_{Peak} < V_{(BR)DSS}$ 

**Electrical characteristics** STS1DN45K3

#### **Electrical characteristics** 2

(T<sub>C</sub> = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	450			٧
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V		(	±10	μΑ
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50 \mu A$	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A	70	3.2	3.8	Ω
Table 5.	Dynamic	colete				
Symbol	Parameter	Test conditions	Min.	Tvp.	Max.	Unit

Table 5. **Dynamic** 

	Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
	C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	150 30 6	-	pF pF pF
Obsole	C <sub>o(tr)</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>DS</sub> = 0 to 360 V, V <sub>GS</sub> = 0	-	TBD	1	pF
	C <sub>o(er)</sub> <sup>(2)</sup>	Equivalent capacitance energy related	v <sub>DS</sub> = 0 to 360 v, v <sub>GS</sub> = 0	-	TBD	1	pF
	$R_{G}$	Intrinsic gate resistance	f = 1 MHz open drain	-	TBD	-	Ω
	Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 360 V, $I_D$ = 0.5 A, $V_{GS}$ = 10 V (see <i>Figure 3</i> )	-	6 TBD TBD	-	nC nC nC

<sup>1.</sup> Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ 

<sup>2.</sup> Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ 

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
$t_{d(on)}$ $t_{r}$ $t_{d(off)}$ $t_{f}$	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 225 \text{ V}, I_{D} = 0.5 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see <i>Figure 4</i> )	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current Source-drain current (pulsed)		-	. \C	0.5 2	A A
V <sub>SD</sub> (2)	Forward on voltage	$I_{SD} = 0.5 \text{ A}, V_{GS} = 0$	- 6		1.6	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 0.5 \text{ A, di/dt} = 100 \text{ A/µs}$ $V_{DD} = 100 \text{ V (see } Figure 7)$	()	TBD TBD TBD		ns nC A
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 0.5 \text{ A, di/dt} = 100 \text{ A/µs}$ $V_{DD} = 100 \text{ V, T}_j = 150 \text{ °C}$ (see <i>Figure 7</i> )	1	TBD TBD TBD		ns nC A

<sup>1.</sup> Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol Parameter	Test conditions	Min.	Тур.	Max.	Unit
BV <sub>GSO</sub> Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

<sup>2.</sup> Pulsed: pulse duration =  $300 \mu s$ , duty cycle 1.5%

Test circuits STS1DN45K3

## 3 Test circuits

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

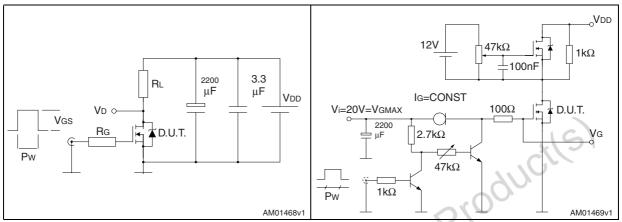


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

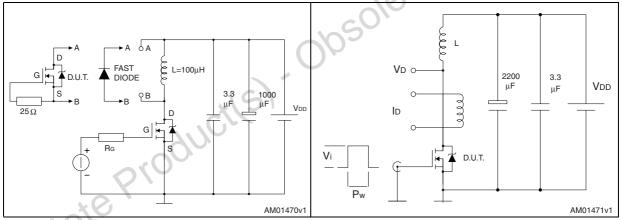
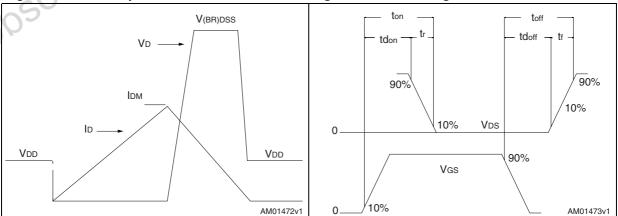


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



577

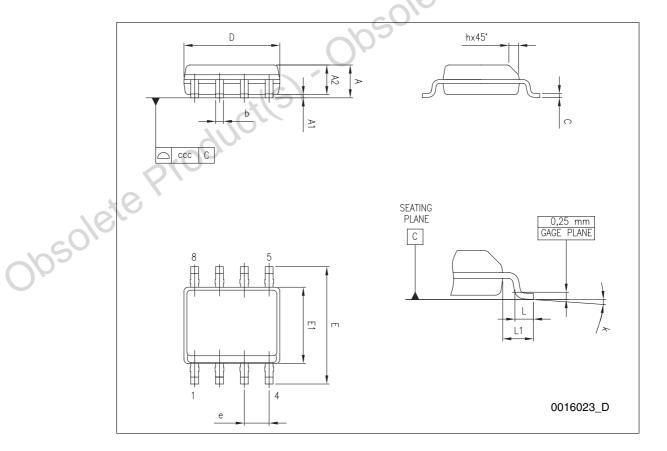
# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Obsolete Product(s). Obsolete Product(s)

### SO-8 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
С	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
е		1.27	1,10
h	0.25		0.50
L	0.40	- *(	1.27
L1		1.04	
k	0°		8°
ccc		×C	0.10



STS1DN45K3 Revision history

# 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Apr-2010	1	First release



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