ID ROM for CRT display

BR24C21 / BR24C21F / BR24C21FJ / BR24C21FV

The BR24C21 series are 1kbits serial EEPROMs and support DDC1™ and DDC2™ interfaces for PLUG&PLAY displays.

●Features

1) 128 x 8 bits serial EEPROM
2) Operating voltage range (2.5V~5.5V)
3) Completely implements DDC1™ / DDC2™ interface for monitor identification
   Transmit-Only Mode
   Recovery Mode
   Bi-directional Mode
4) Page write function : 8 bytes
5) Low current consumption
   Active (at 5V) : 1.5mA (Typ.)
   Standby (at 5V) : 10μA (Typ.)
6) DATA security
   Write enable feature
   Inhibit to WRITE at low Vcc
7) Compact packages
8) High reliability fine pattern CMOS technology
9) Rewriting possible up to 100,000 times
10) Data can be stored for ten years without corruption
11) Noise filters at SCL, SDA and VCLK pins

●Absolute maximum ratings (Ta=25°C)

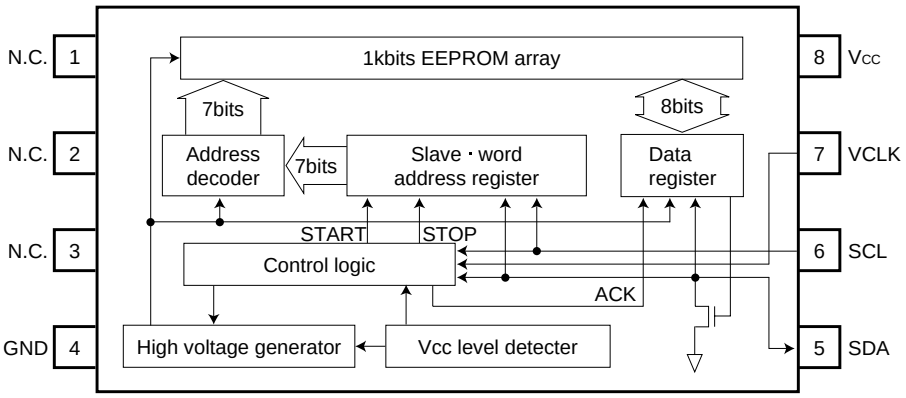
Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	−0.3~+6.5	V
Power disssipation	Pd	800(DIP8) ∗1	mW
		450(SOP8) ∗2	
		450(SOP-J8) ∗2	
		350(SSOP-B8) ∗3	
Storage temperature range	Tstg	−65~+125	°C
Operating temperature range	Topr	−40~+85	°C
Terminal voltage	−	−0.3~V_{CC}+0.3	V

∗1 Degradation is done at 8.0mW/°C for operation above 25°C.
∗2 Degradation is done at 4.5mW/°C for operation above 25°C.
∗3 Degradation is done at 3.5mW/°C for operation above 25°C.

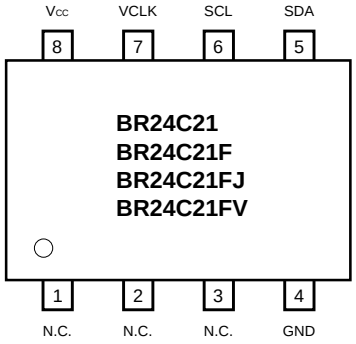
●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	2.5~5.5	V
Input voltage	V_{IN}	0~V_{CC}	V

●Block diagram



●Pin assignment



●Pin descriptions

Pin No.	Pin name	I / O	Function
1	N.C.	–	No connection
2	N.C.	–	No connection
3	N.C.	–	No connection
4	GND	–	Ground (0V)
5	SDA	I / O	Slave and word address, serial data input, serial data output *
6	SCL	I	Serial clock input for Bi-directional Mode
7	VCLK	I	Clock input (Transmit-Only Mode) Write enable (Bi-directional Mode)
8	Vcc	–	Power supply

* An open drain output requires a pull-up resistor.

●**Electrical characteristics** (Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.5~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"HIGH" input volatge1	V_{IH1}	0.7V_{CC}	–	–	V	SCL, SDA
"LOW" input volatge1	V_{IL1}	–	–	0.3V_{CC}	V	SCL, SDA
"HIGH" input volatge2	V_{IH2}	2.0	–	–	V	VCLK
"LOW" input volatge2	V_{IL2}	–	–	0.8	V	VCLK, V_{CC}≥4.0V
"LOW" input volatge3	V_{IL3}	–	–	0.2V_{CC}	V	VCLK, V_{CC}<4.0V
"LOW" output volatge	V_{OL}	–	–	0.4	V	SDA, I_{OL}=3.0mA
Input leakage current	I_{LI}	–1	–	1	µA	SCL, VCLK, V_{IN}=0V~V_{CC}
Output leakage current	I_{LO}	–1	–	1	µA	SDA, V_{OUT}=0V~V_{CC}
Operating current	I_{CC}	–	–	3.0	mA	V_{CC}=5.5V, f_{SCL}=400kHz
Standby current	I_{SB}	–	10	100	µA	V_{CC}=5.5V, SDA=SCL=V_{CC}, VCLK=GND *1

*1 Transmit-Only Mode…After the power is on, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV are in Standby state without providing the clock on the VCLK pin. After the VCLK pin is provided the clock, the device is switched from Standby to Transmit-Only Mode, and the operating current runs.
Bi-directional Mode…The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV are in Standby state after each command is porformed.

●**Operating timing characteristics** (Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.5~5.5V)

Parameter	Symbol	Fast-mode Vcc=2.5~5.5V			Standard-mode Vcc=2.5~5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL frequency	f_{SCL}	–	–	400	–	–	100	kHz
Data clock "HIGH" time	t_{HIGH}	0.6	–	–	4.0	–	–	µs
Data clock "LOW" time	t_{LOW}	1.3	–	–	4.7	–	–	µs
SDA/SCL rise time	t_R	–	–	0.3	–	–	1.0	µs
SDA/SCL fall time	t_F	–	–	0.3	–	–	0.3	µs
Start condition hold time	t_{HD} : STA	0.6	–	–	4.0	–	–	µs
Start condition setup time	t_{SU} : STA	0.6	–	–	4.7	–	–	µs
Input data hold time	t_{HD} : DAT	0	–	–	0	–	–	ns
Input data setup time	t_{SU} : DAT	100	–	–	250	–	–	ns
Output data delay time (SCL)	t_{PD}	–	–	0.9	–	–	3.5	µs
Stop condition setup time	t_{SU} : STO	0.6	–	–	4.0	–	–	µs
Bus open time before start or transfer	t_{BUF}	1.3	–	–	4.7	–	–	µs
Internal write cycle time	t_{WR}	–	–	10	–	–	10	ms
Noise erase valid time (SCL and SDA)	t_I	–	–	0.1	–	–	0.1	µs
<Transmit-Only Mode>								
Output data delay time (VCLK)	t_{VPD}	–	–	1.0	–	–	2.0	µs
VCLK "HIGH" time	t_{VHIGH}	0.6	–	–	4.0	–	–	µs
VCLK "LOW" time	t_{VLOW}	1.3	–	–	4.7	–	–	µs
VCLK setup time	t_{VSU}	0	–	–	0	–	–	µs
VCLK hold time	t_{VHD}	0.6	–	–	4.0	–	–	µs
Mode transition time	t_{VHZ}	–	–	0.5	–	–	1.0	µs
Transmit-Only powerup time	t_{VPU}	0	–	–	0	–	–	µs
Noise erase valid time (VCLK)	t_{VI}	–	–	0.1	–	–	0.1	µs

●Timing charts

SYNCHRONOUS DATA TIMING

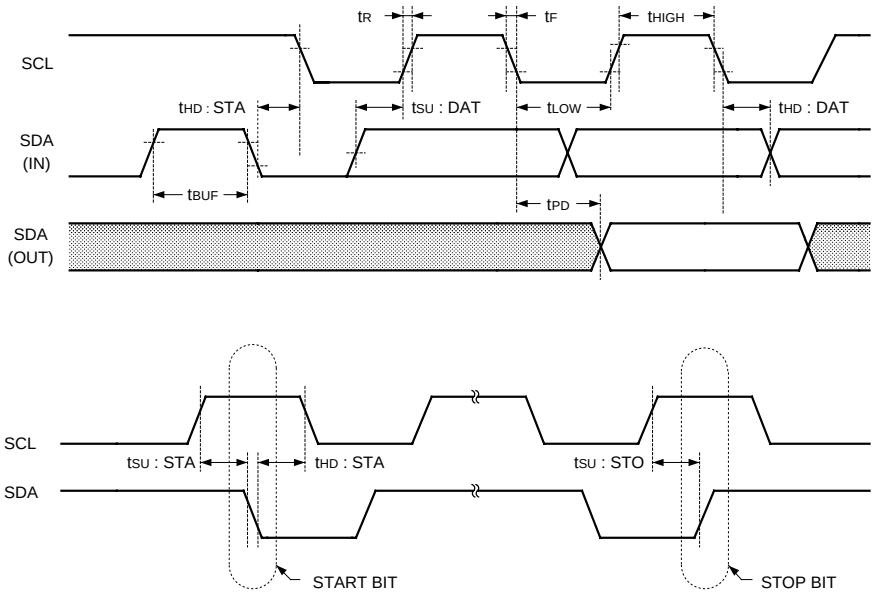


Fig.7

- SDA data is latched into the chip at the rising edge of the SCL clock.
- Output data toggles at the falling edge of the SCL clock.

WRITE CYCLE TIMING

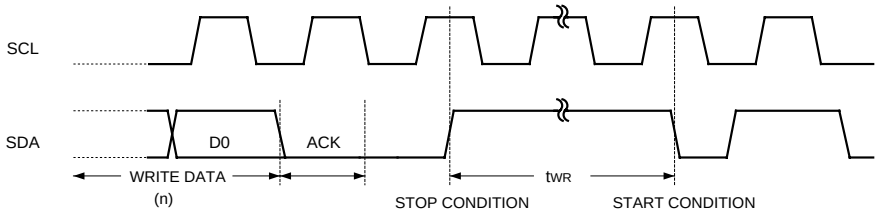


Fig.8

WRITE ENABLE TIMING

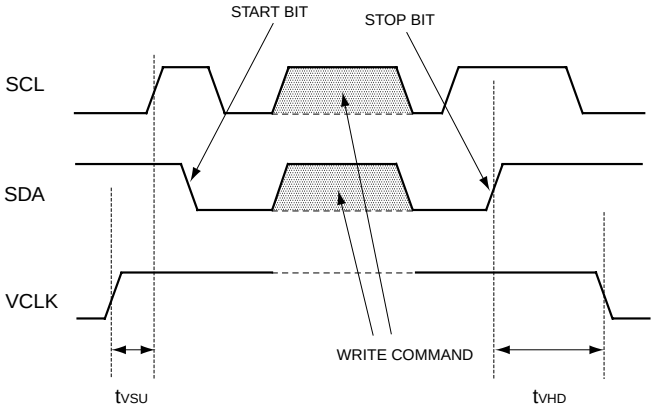


Fig.9

●Circuit operation

The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV operate in two modes, Transmit-Only Mode and Bi-directional Mode. The devices operate in Transmit-Only Mode when they will power up. In this mode, the devices transmit data on the SDA pin with the VCLK clock. This mode is continued by providing a valid high to low transition on the SCL pin.
The devices can be switched into Bi-directional Mode by providing a valid high to low transition on the SCL pin. They begin to count the VCLK clock at once. If the VCLK counter reaches 128 clock without the command for Bi-directional Mode, the device revert to Transmit-Only Mode. (Recovery function) If the devices are received the command for Bi-directional Mode and respond with an Acknowledge before the VCLK counter reaches 128 clock, it is impossible to revert to Transmit-Only Mode. (The way to switch Bi-directional Mode to Transmit-Only Mode is that the power down again.)

* When the power is on, the SCL pin set to V_{CC} (High level).

(1) Transmit-Only Mode

- After the power is on, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV are in Transmit-Only Mode. In this mode, the data can be output by providing the clock on the VCLK pin.
- When the power is on, the SCL pin set to V_{CC} (High level).
- The state of SDA is high-impedance during input of the first 9 clocks, and a data is output starting with the 10th rising clock edge on VCLK. After the power is on, the output data is as follow

  00h address data → 01h address data → 02h address data → …

  The address is incremented by one with every 9 clock of VCLK. All address is output in this mode. When the counter reaches the last address, the next output data is 00h address data.
- In the mode, the NULL bit (High data) is output between the address data and the next address data.
- The read operation in Transmit-Only Mode can be started after the power stabilized.

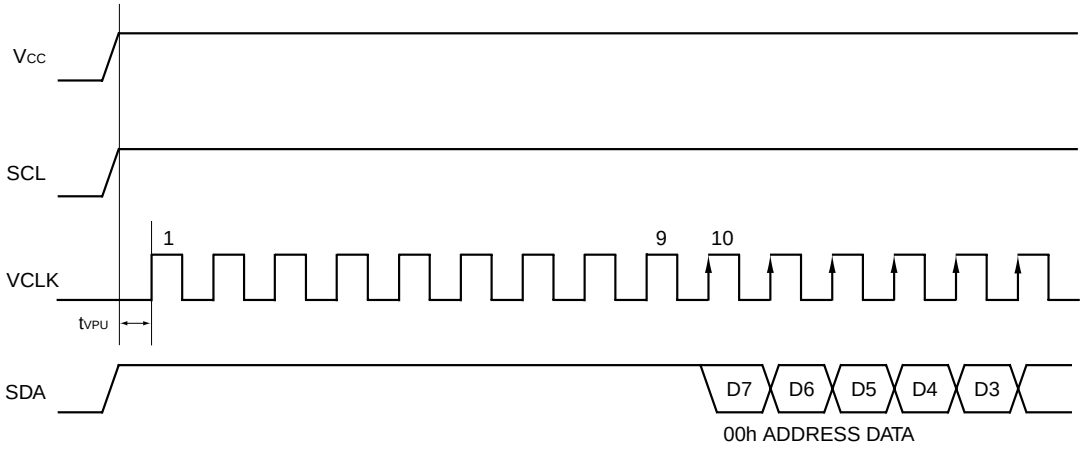


Fig.10 TRANSMIT-ONLY MODE

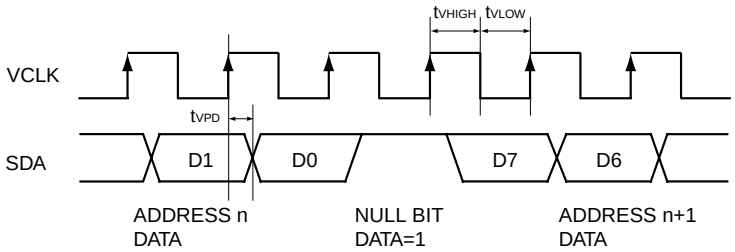


Fig.11 NULL BIT

(2) Bi-directional Mode

1) Bi-directional Mode and Recovery function

- The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV can be switched from Transmit-Only Mode to Bi-directional Mode by providing a valid high to low transition on the SCL pin, and the state of SDA is high-impedance.
- After a valid high to low transition on the SCL pin, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV begin to count the VCLK clock. If the VCLK counter reaches 128 clock without the command for Bi-directional Mode, the device revert to Transmit-Only Mode. (Recovery function) The VCLK counter is reset by providing a valid high to low transition on the SCL pin. After reversion to Transmit-Only Mode, the devices begin to output a data with the 129th rising clock edge on VCLK. The output data is 00h address data at the time.
- If the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV are switched from Transmit-Only Mode and received the command for Bi-directional Mode and responds with an Acknowledge, it is impossible to revert to Transmit-Only Mode. (The only way to revert to Transmit-Only Mode is that the power down again.) Unless the input device code is "1010", the device responds no Acknowledge. If the VCLK counter reaches 128 clock afterward, it is possible to revert to Transmit-Only Mode for Recovery function. If the master generates a stop condition during the slave address input, it is possible to revert to Transmit-Only Mode.
- When the devices are switched from Transmit-Only Mode to Bi-directional Mode, the period of t_{VHZ} need to be held.

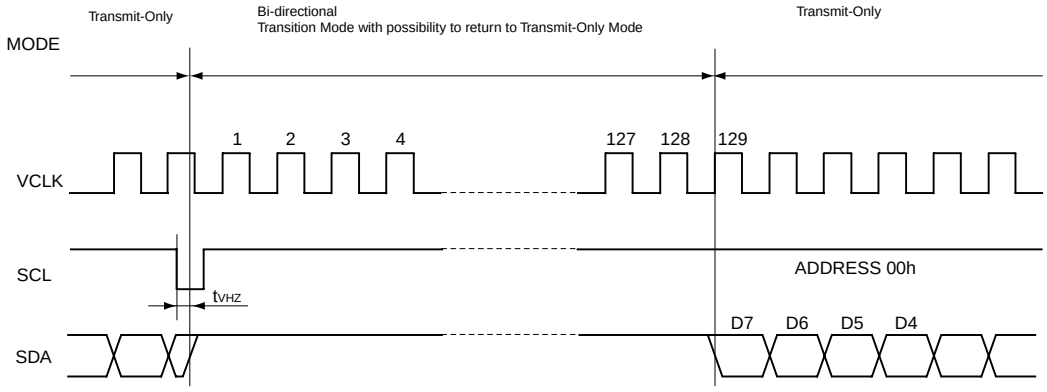


Fig.12 RECOVERY MODE

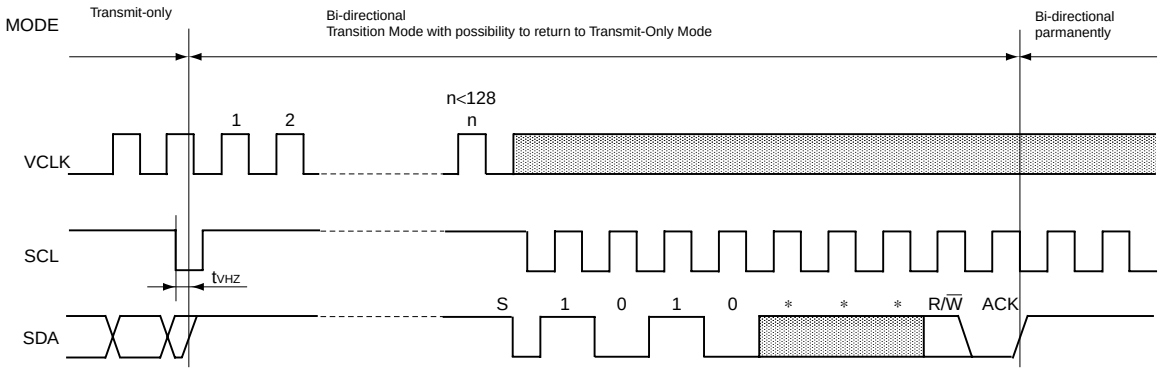


Fig.13 MODE CHANGE

2) Bi-directional Mode

START CONDITION

- All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH.
- The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

- All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.
- The stop condition initiates internal write cycle to write the data into memory array after write sequence.
- The stop condition is also used to place the device into the standby power mode after read sequence.
- A stop condition can only be issued after the transmitting device has released the bus.

DEVICE ADDRESSING

- Following a START condition, the master output the device address of the slave to be accessed. The most significant four bits of the slave address are the “device type indentifier”, For the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV this is fixed as “1010”.
- The next three bits of the slave address are don’t care.
- The last bit of the stream determines the operation to be performed. When set to “1”, a read operation is selected ; when set to “0”, a write operation is selected.

  R / $\overline{W}$ set to “0” ··· WRITE

  (This bit also sets to “0” for random read operation)

  R / $\overline{W}$ set to “1” ··· READ

1010	*	*	*	R / $\overline{W}$

* Don't care

WRITE PROTECT FUNCTION

- WRITE ENABLE (VCLK)

When using the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV in the Bi-directional Mode, the VCLK pin can be used as a write enable pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device. Setting VCLK low allow the word address setting in random read.

ACKNOWLEDGE

- Acknowledge is a software convention used to indicate successful data transfers. The master or the slave will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that the eight bits of data has been received.
- The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV will respond with an Acknowledge after recognition of a START condition and its slave address. If both the device and a write operation have been selected, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV will respond with an Acknowledge, after the receipt of each subsequent 8-bit word.
- In the READ mode, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV will transmit eight bits of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected, and no STOP condition is generated by the master, the BR24C21, BR24C21F, BR24C21FJ, BR24C21FV will continue to transmit the data.
- If an Acknowledge is not detected, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV will terminate further data transmissions and await a STOP condition before returning to the standby mode.

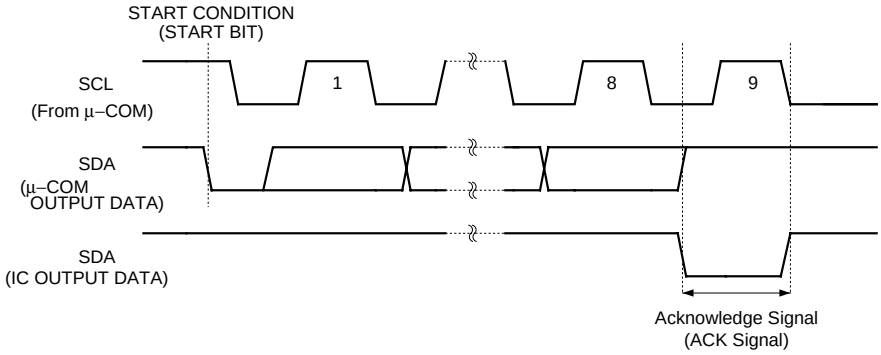


Fig.14 ACKNOWLEDGE RESPONSE FROM RECEIVER

3) Bi-directional Mode Command

BYTE WRITE

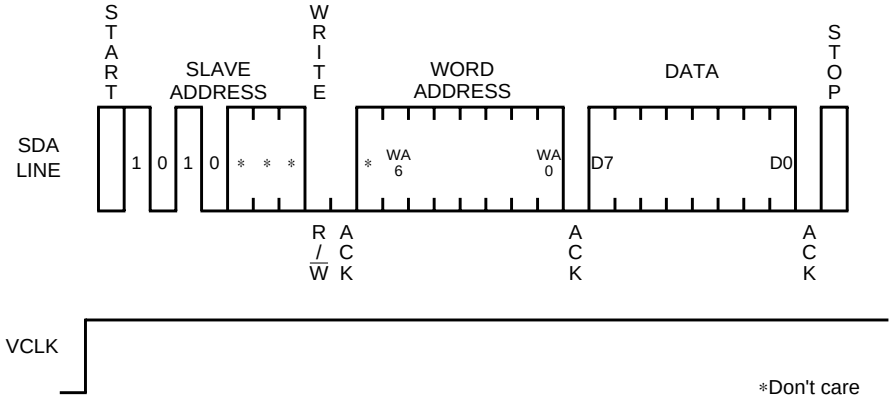


Fig.15 BYTE WRITE CYCLE TIMING

- When the master generates a STOP condition, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV begin the internal write cycle to the nonvolatile array.

PAGE WRITE

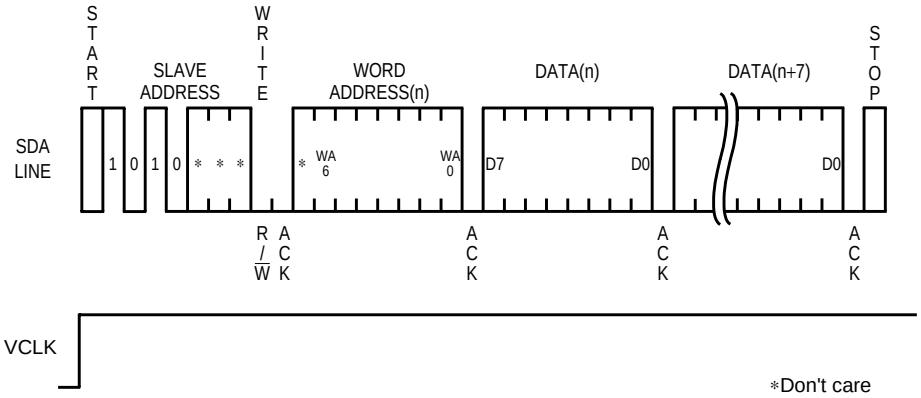


Fig.16 PAGE WRITE CYCLE TIMING

- If the master transmits the next data instead of generating a stop condition in byte write cycle, the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV transfer from byte write cycle to page write cycle. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The high order five bits of the word address remains constant.
  If the master transmits more than eight words, prior to generating the STOP condition, the address counter will "roll over", and the previous transmitted data will be overwritten.

CURRENT READ

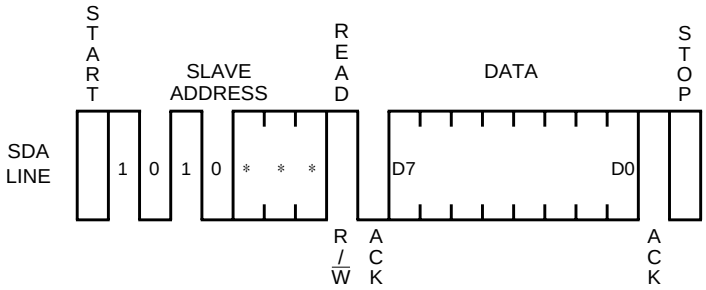


Fig.17 CURRENT READ CYCLE TIMING

- The BR24C21, BR24C21F, BR24C21FJ and BR24C21FV contain an internal address counter which maintains the address of the last word accessed, incremented by one. If the last accessed address is address n in a read operation, the next read operation will access data from address n+1 and increment the current address counter. If the last accessed address is address n in a write operation, the next read operation will access data from address n. If the master does not transfer the acknowledge but does generate a stop condition, the current address read operation only provides a single byte of data. At this point, the device discontinues transmission.

RANDOM READ

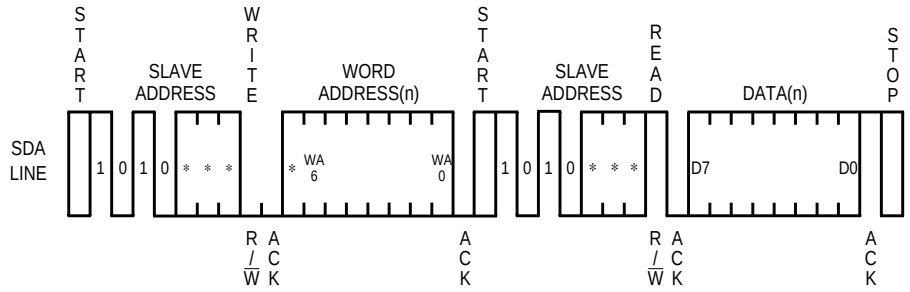


Fig.18 RANDOM READ CYCLE TIMING

- Random read operation allows the master to access any memory location. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with R / $\overline{W}$ set to “0”) followed by the address of the word to be read. This procedure sets the internal address counter of the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV to the desired address. After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by the slave address field with R / W the set to “1”. The device will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. If the master does not acknowledge the transmission but does generate the stop condition, at this point BR24C21, BR24C21F, BR24C21FJ and BR24C21FV discontinue transmission.

SEQUENTIAL READ

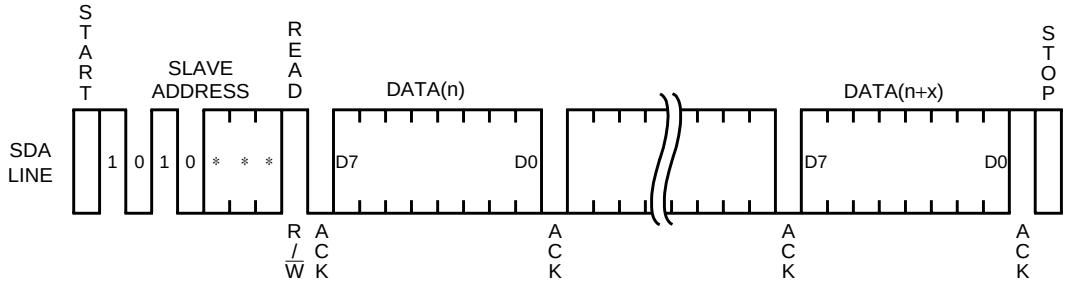
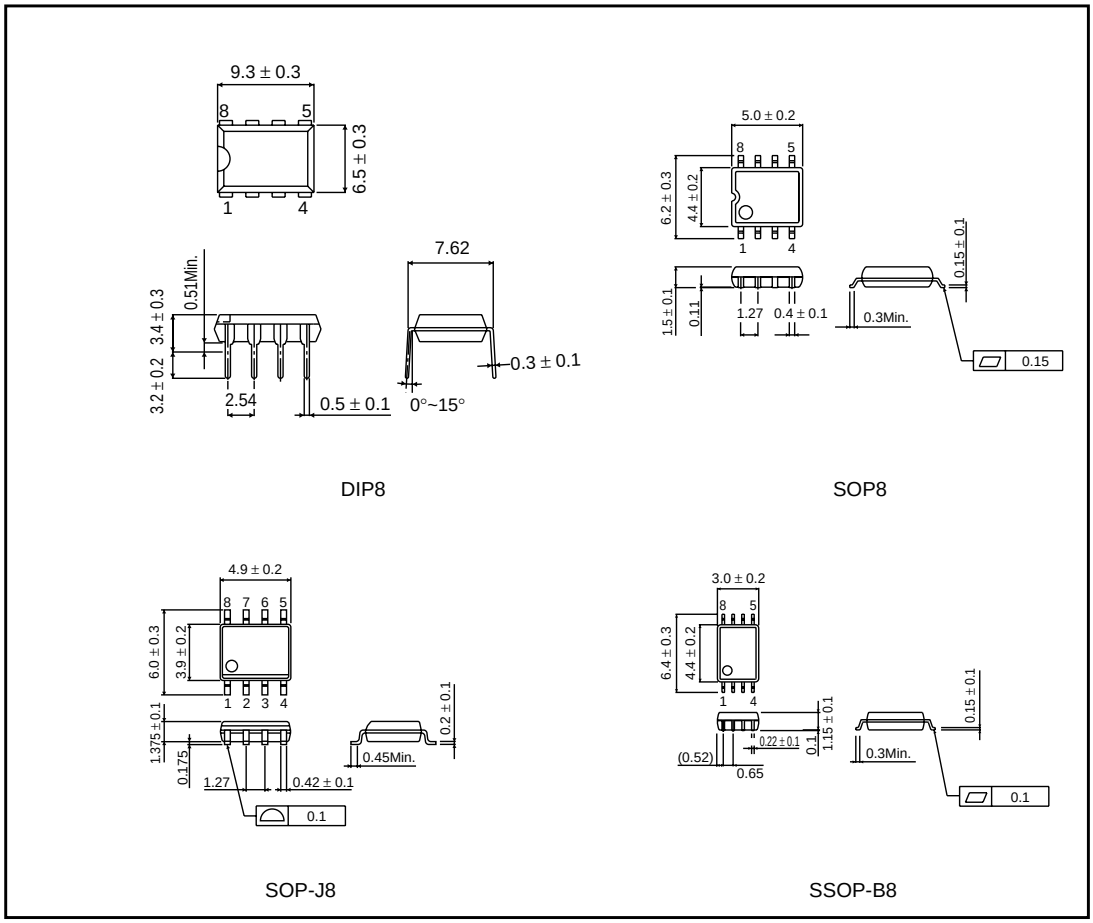


Fig.19 SEQUENTIAL READ CYCLE TIMING
(Current Read)

- During the sequential read operation, the internal address counter of the BR24C21, BR24C21F, BR24C21FJ and BR24C21FV automatically increments with each acknowledge received ensuring the data from address n will be followed with the data from n+1. For read operations, all bits of the address counter are incremented allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will “roll over” to the bottom of the array and continue to transmit the data.
- The sequential read operation can be performed with both current read and random read.

●**External dimension** (Units : mm)



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