



DRV5023 Digital-Switch Hall Effect Sensor

1 Features

- Digital Unipolar-Switch Hall Sensor
- Superior Temperature Stability
 - Sensitivity $\pm 10\%$ Over Temperature
- High Sensitivity Options:
 - $+6.9 / +2.3$ mT (AJ)
 - $+13.8 / +4.6$ mT (BI)
- Supports a Wide Voltage Range
 - 2.5 to 38 V
 - Operation from Unregulated Supply
- Wide Operating Temperature Range
 - $T_A = -40$ to 125°C (Q see [Figure 22](#))
- Open Drain Output
 - Up to 30-mA Current Sink
- Fast Power-On: 35 μs
- Small Package and Footprint
 - Surface Mount 3-Pin SOT-23 (DBZ)
 - $2.92\text{ mm} \times 2.37\text{ mm}$
 - Through-Hole 3-Pin SIP (LPG)
 - $4.00\text{ mm} \times 3.15\text{ mm}$
- **Protection Features**
 - Reverse Supply Protection (up to -22 V)
 - Supports up to 40-V Load Dump
 - Output Short-Circuit Protection
 - Output Current Limitation

2 Applications

- Docking Detection
- Door Open and Close Detection
- Proximity Sensing
- Valve Positioning
- Pulse Counting

3 Description

The DRV5023 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

When the applied magnetic flux density exceeds the B_{OP} threshold, the DRV5023 open drain output goes low. The output stays low until the field decreases to less than B_{RP} , and then the output goes to high impedance. The output current sink capability is 30 mA. A wide operating voltage range from 2.5 V to 38 V with reverse polarity protection up to -22 V makes the device suitable for a wide range of industrial applications.

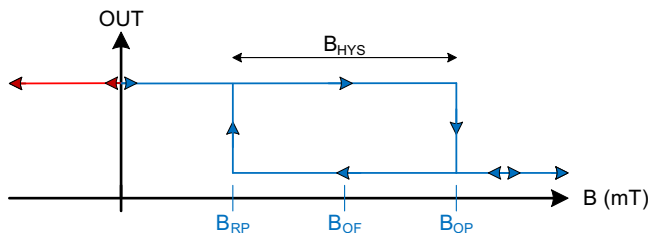
Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information⁽¹⁾

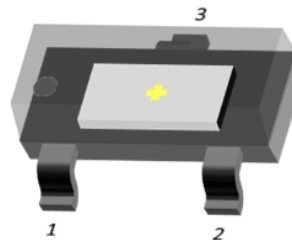
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5023	SOT-23 (3)	$2.92\text{ mm} \times 2.37\text{ mm}$
	SIP (3)	$4.00\text{ mm} \times 3.15\text{ mm}$

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Output State



SOT-23



SIP

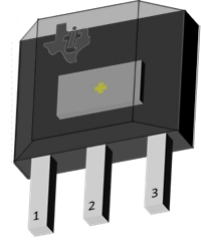


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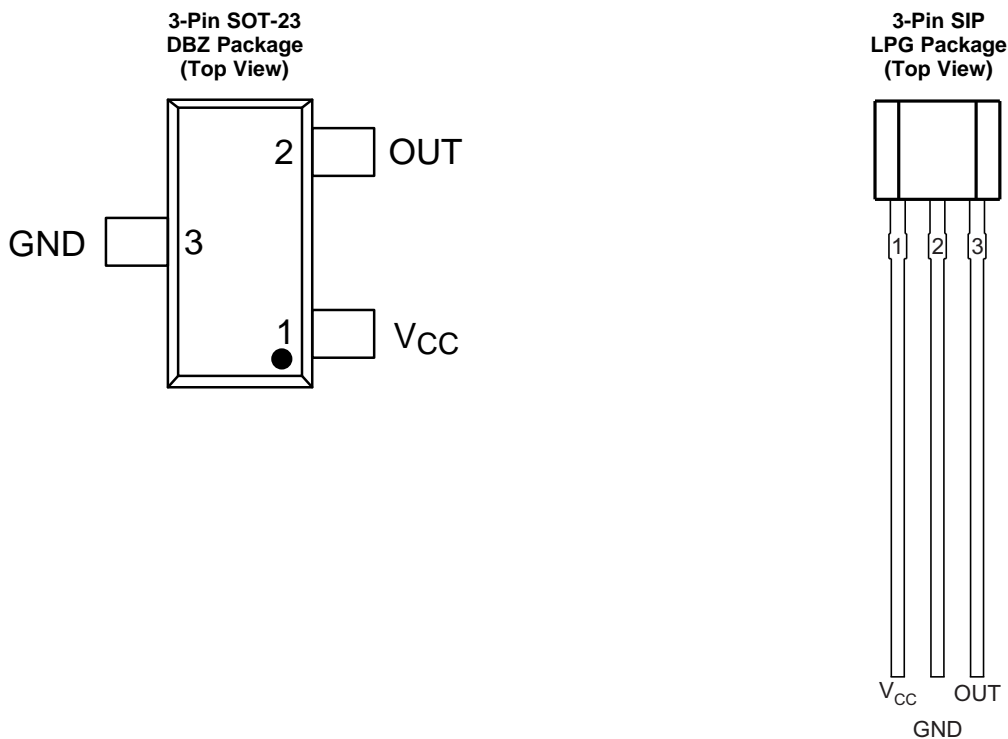
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5 Revision History

DATE	REVISION	NOTES
May 2014	*	Initial release.

6 Pin Configuration and Functions

For additional configuration information, see [Device Markings](#) and [Mechanical, Packaging, and Orderable Information](#).



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NUMBER			
	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V _{CC}	1	1	Power	2.5 to 38 V power supply. Bypass this terminal to the GND terminal with a 0.01-μF (minimum) ceramic capacitor rated for V _{CC} .

PRODUCT PREVIEW

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage	V _{CC}	–22 ⁽²⁾	40	V
	Voltage ramp rate (V _{CC}), V _{CC} < 5 V	Unlimited		V/μs
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V	0	2	
Output pin voltage	OUT	–0.5	40	V
Output pin reverse current during reverse supply condition	OUT	0	100	mA
Operating junction temperature	T _J	–40	175 ⁽³⁾	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Ensured by design. Only tested to –20 V.
- (3) Tested in production to T_A = 125°C.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	−2.5	2.5	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	−500	500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	2.5	38	V
V _O	Output pin voltage (OUT)	0	38	V
I _{SINK}	Output pin current sink (OUT) ⁽¹⁾	0	30	mA
T _A	Operating ambient temperature	–40	125	°C

- (1) Power dissipation and thermal limits must be observed.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DBZ (3 PINS)	LPG (3 PINS)	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	333.2	180	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.9	98.6	
R _{θJB}	Junction-to-board thermal resistance	66.9	154.9	
ψ _{JT}	Junction-to-top characterization parameter	4.9	40	
ψ _{JB}	Junction-to-board characterization parameter	65.2	154.9	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V _{CC}	V _{CC} operating voltage		2.5		38	V
I _{CC}	Operating supply current	V _{CC} = 2.5 to 38 V, T _A = 25°C		2.7		mA
		V _{CC} = 2.5 to 38 V, T _A = 125°C		3	3.5	
t _{on}	Power-on time			35	50	μs
OPEN DRAIN OUTPUT (OUT)						
r _{DS(on)}	FET on-resistance	V _{CC} = 3.3 V, I _O = 10 mA, T _A = 25°C		16		Ω
		V _{CC} = 3.3 V, I _O = 10 mA, T _A = 125°C		25	50	
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μA
PROTECTION CIRCUITS						
V _{CCR}	Reverse supply voltage		–22			V
I _{OCP}	Overcurrent protection level	Output current is clamped to this level	20	30	40	mA

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t _d	Output delay time	B = B _{RP} – 10 mT to B _{OP} + 10 mT in 1 μs		13	25	μs
t _r	Output rise time (10% to 90%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V			0.5	μs
t _f	Output fall time (90% to 10%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V			0.2	μs

7.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f_{BW}	Bandwidth		20			kHz
DRV5023AJ: +6.9 / +2.3 mT						
B _{OP}	Operate point (see Figure 12)	T _A = −40°C to 125°C	+3	+6.9	+12	mT
B _{RP}	Release point (see Figure 12)		+1	+2.3	+4	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} − B _{RP})		3	4.6	7	mT
B _O	Magnetic Offset, B _O = (B _{OP} + B _{RP}) / 2		+3.1	+4.6	+6.1	mT
DRV5023BI: +13.8 / +4.6 mT						
B _{OP}	Operate point (see Figure 12)	T _A = −40°C to 125°C	+6	+13.8	+24	mT
B _{RP}	Release point (see Figure 12)		+2	+4.6	+8	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} − B _{RP})		6	9.2	14	mT
B _O	Magnetic Offset, B _O = (B _{OP} + B _{RP}) / 2		+6.6	+8.1	+9.6	mT

(1) 1 mT = 10 Gauss

7.8 Typical Characteristics

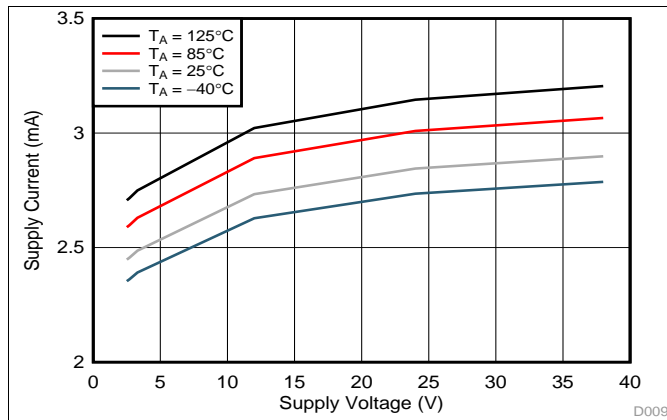


Figure 1. I_{CC} vs V_{CC}

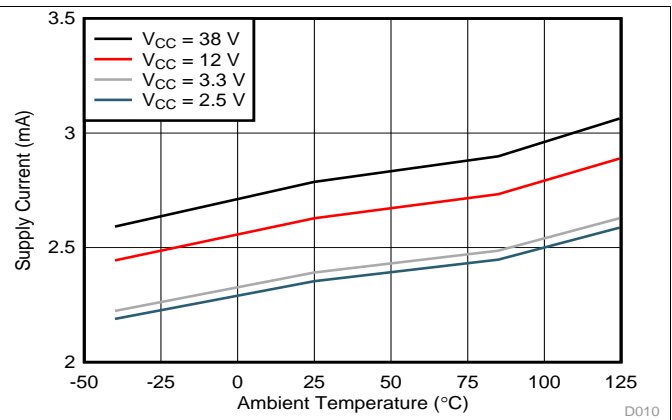


Figure 2. I_{CC} vs Temperature

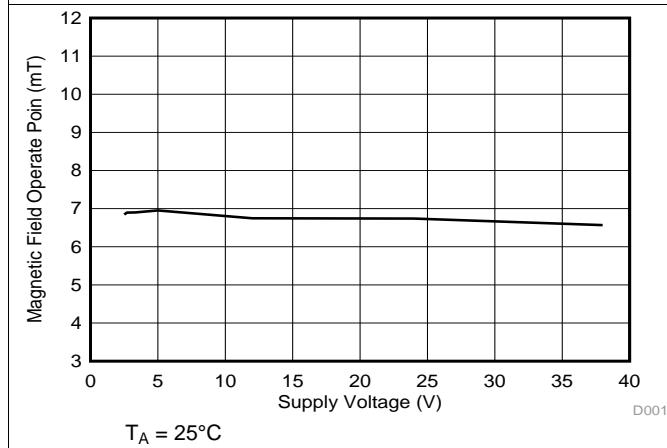


Figure 3. DRV5023AJ
 B_{OP} vs V_{CC}

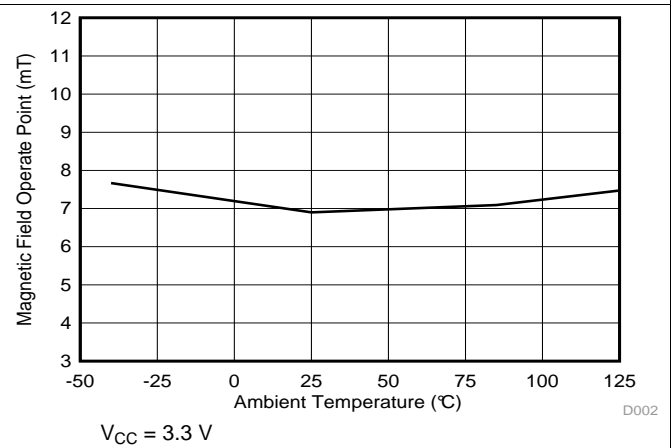


Figure 4. DRV5023AJ
 B_{OP} vs Temperature

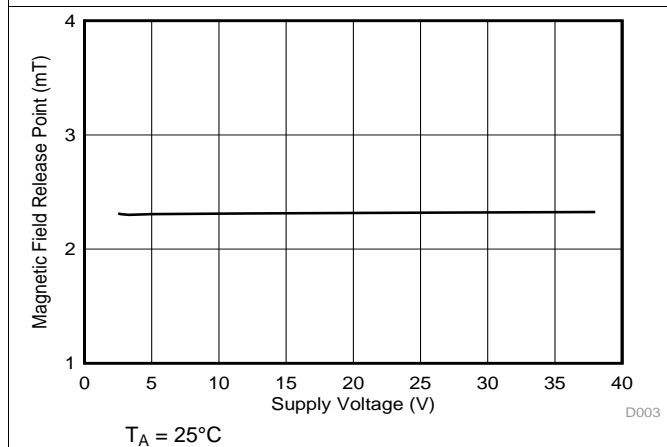


Figure 5. DRV5023AJ
 B_{RP} vs V_{CC}

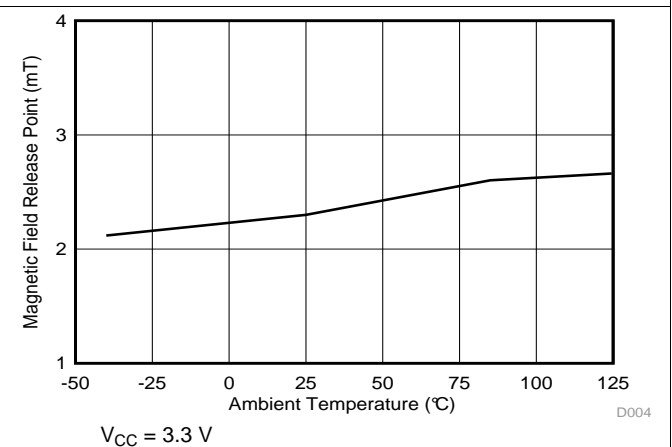


Figure 6. DRV5023AJ
 B_{RP} vs Temperature

Typical Characteristics (continued)

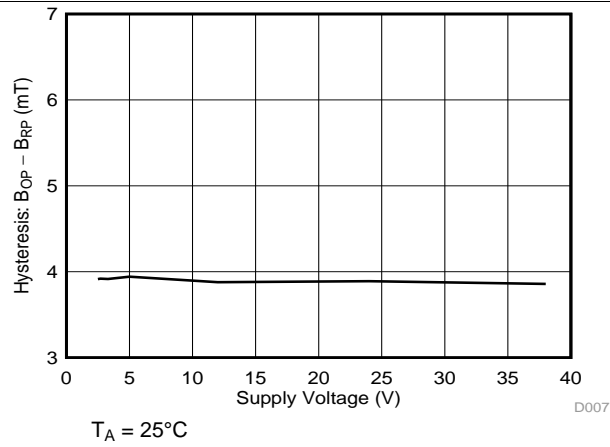


Figure 7. Hysteresis vs V_{CC}

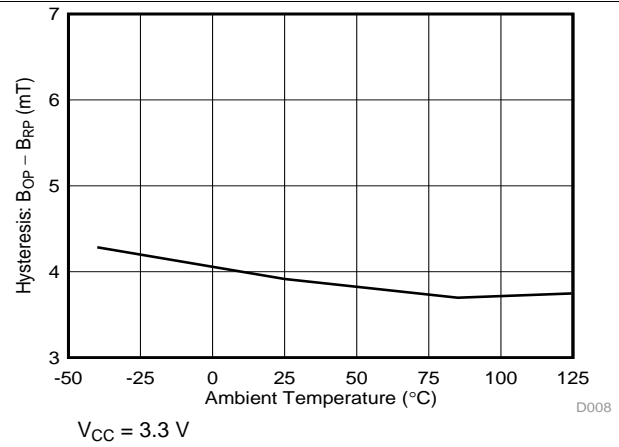


Figure 8. Hysteresis vs Temperature

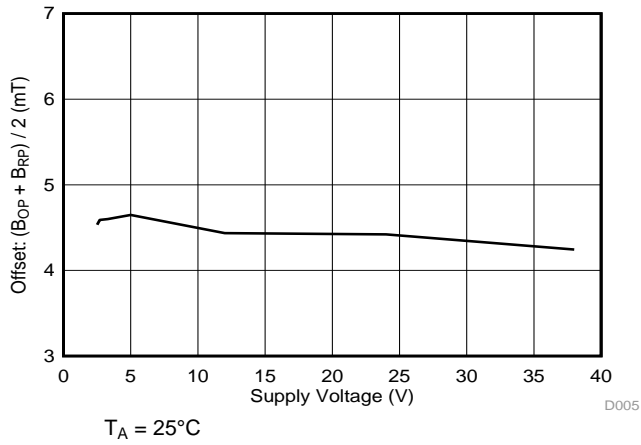


Figure 9. DRV5023AJ
Offset vs V_{CC}

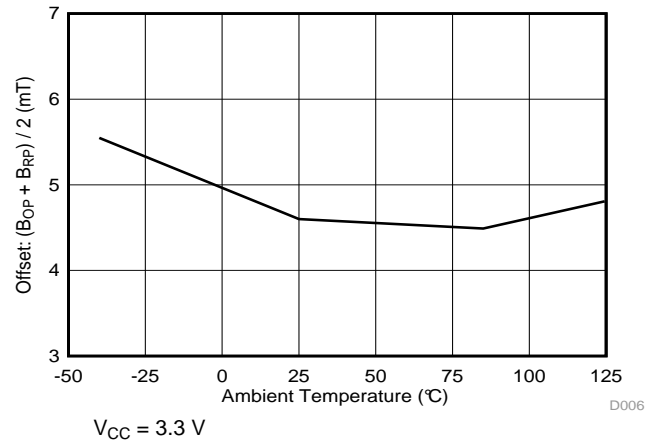


Figure 10. DRV5023AJ
Offset vs Temperature

PRODUCT PREVIEW

8 Detailed Description

8.1 Overview

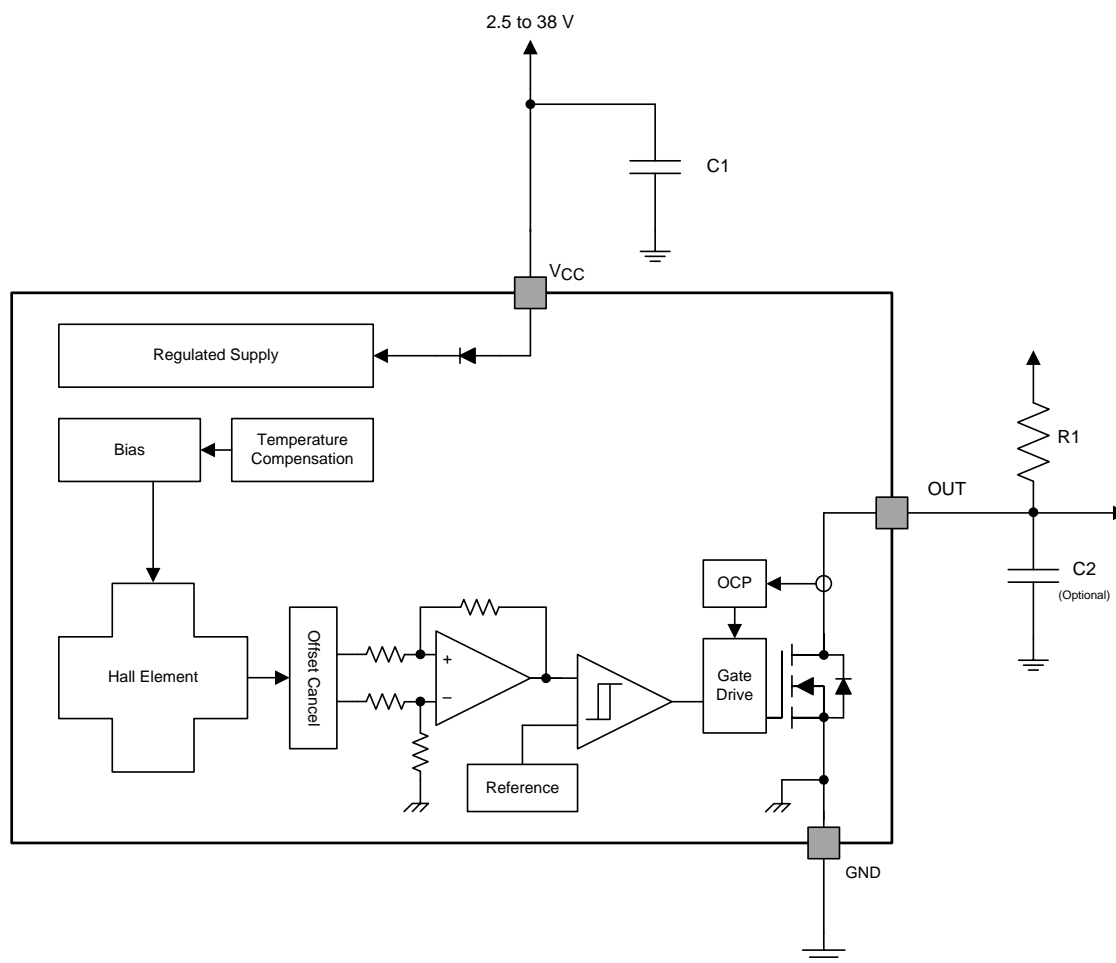
The DRV5023 device is a chopper-stabilized Hall sensor with an digital latched output for magnetic sensing applications. The DRV5023 device can be powered with a supply voltage between 2.5 and 38 V, and will survive –22 V reverse-battery conditions. The DRV5023 device does not operate when –22 to 2.4 V is applied to the VCC pin (with respect to GND pin). In addition, the device can withstand supply voltages up to 40 V for transient durations.

The field polarity is defined as follows: a **south pole** near the marked side of the package is a positive magnetic field. A **north pole** near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A strong **south pole** near the marked side of the package causes the output to pull low (operate point, BOP), and a weak **south pole** causes the output to release (release point, BRP). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Field Direction Definition

A positive magnetic field is defined as a **south pole** near the marked side of the package as shown in [Figure 11](#).

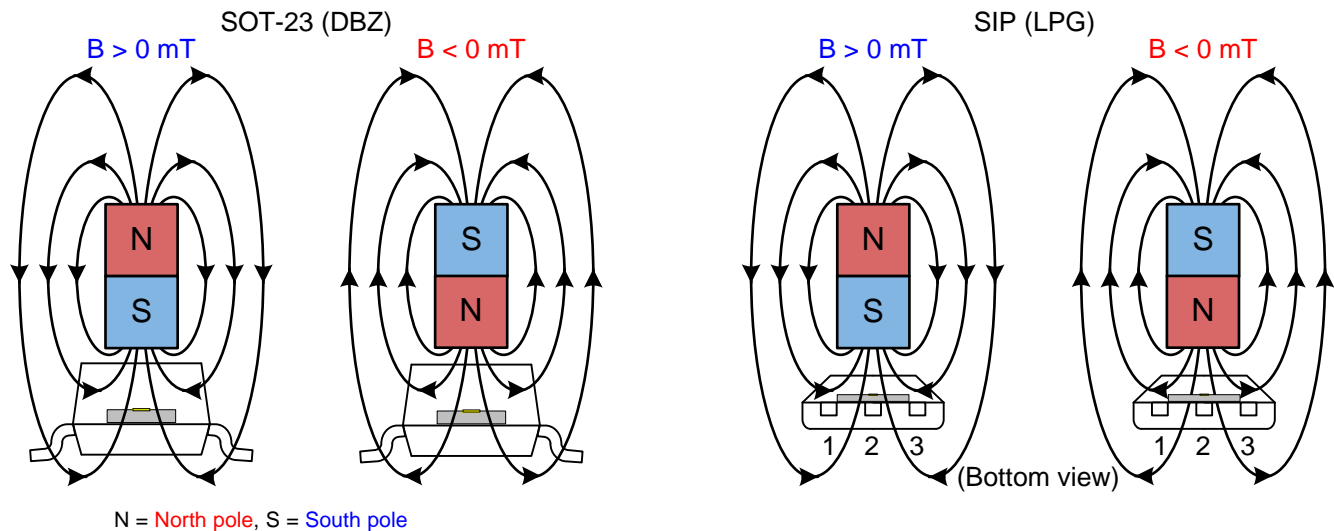


Figure 11. Field Direction Definition

8.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP} , then the output is pulled low. If the field strength is less than B_{RP} , then the output is released.

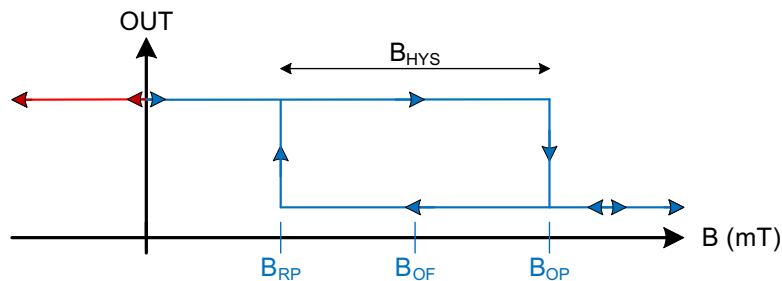


Figure 12. Output State

Feature Description (continued)

8.3.3 Power-On Time

After applying V_{CC} to the DRV5023 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5023 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field $B > B_{OP}$ and $B < B_{RP}$.

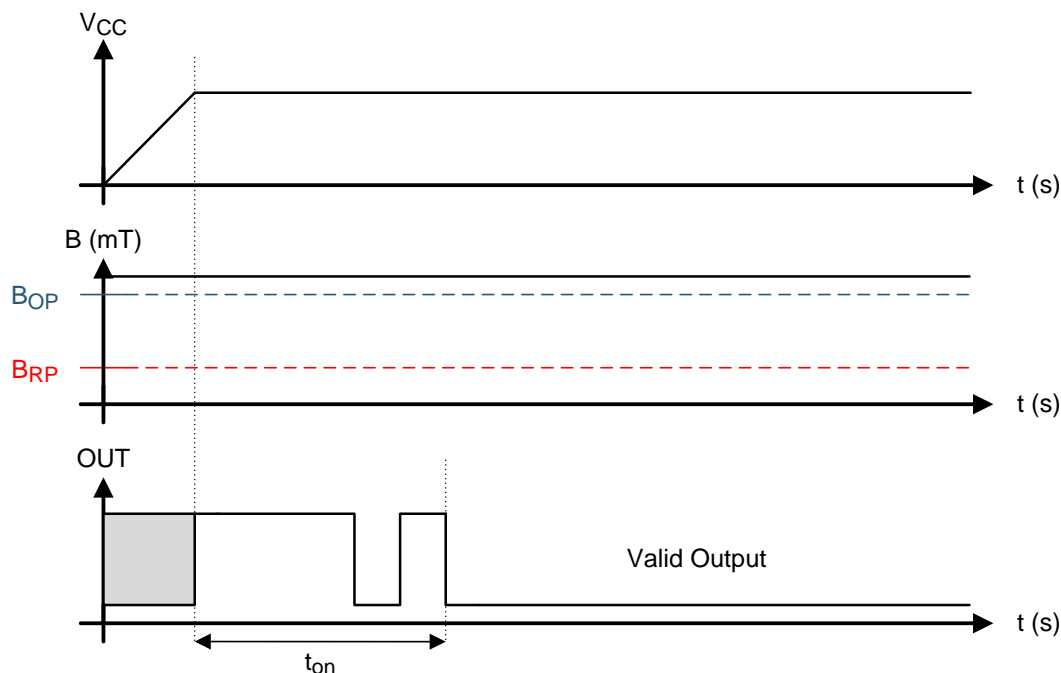


Figure 13. Case 1: Power On When $B > B_{OP}$

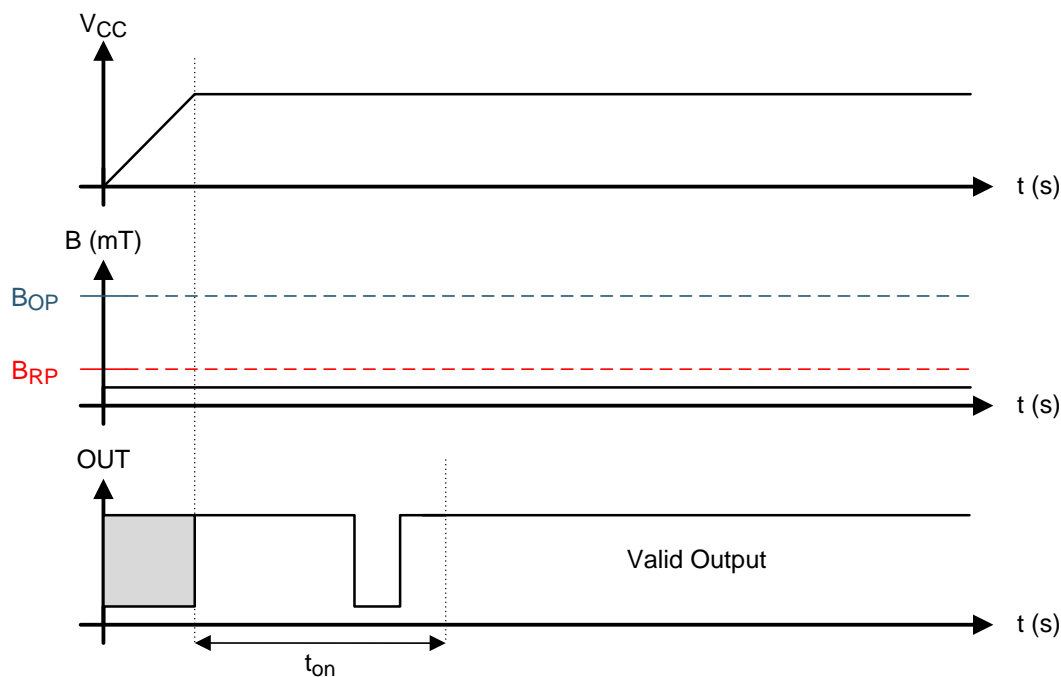


Figure 14. Case 2: Power On When $B < B_{RP}$

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

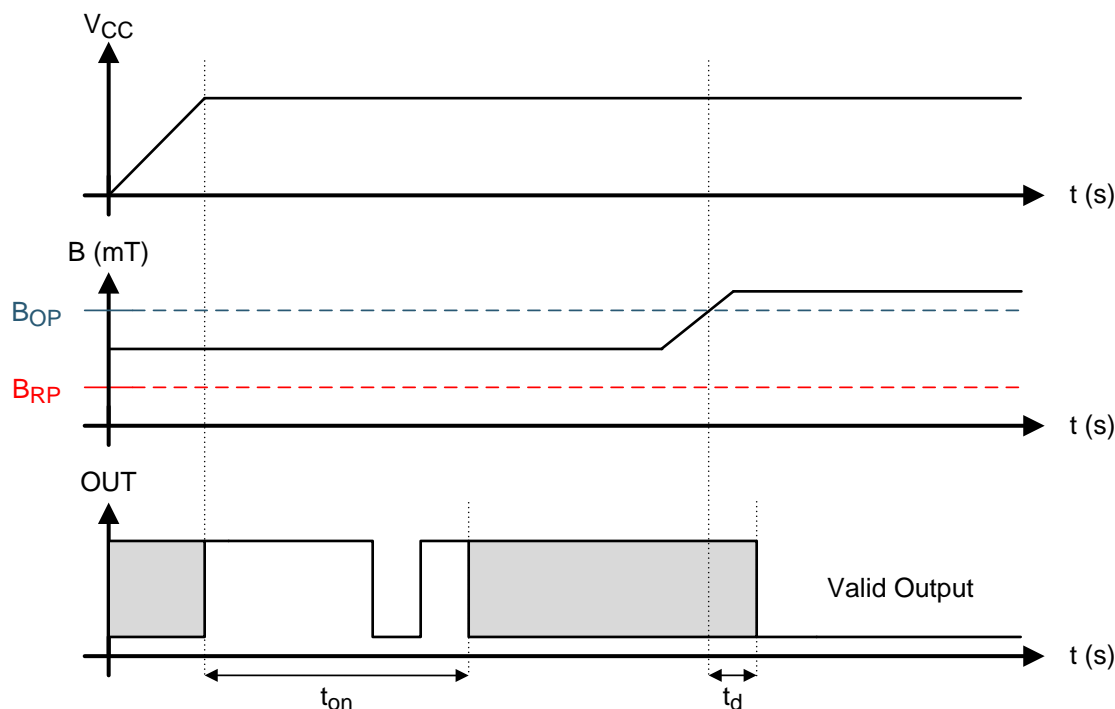


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

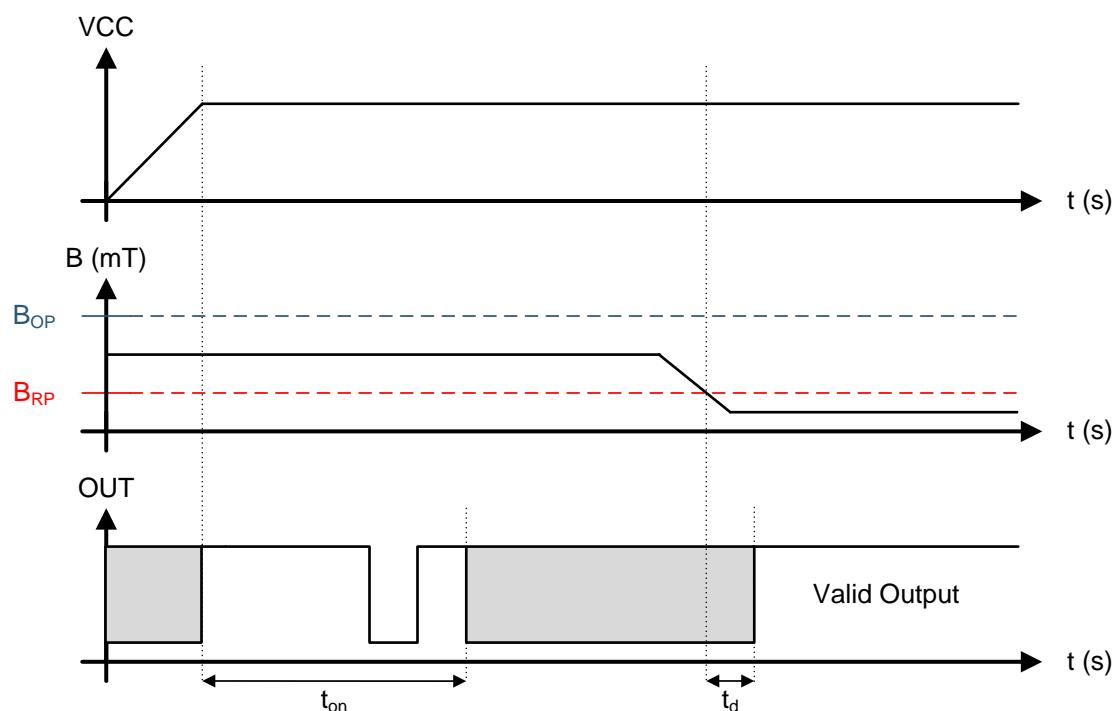


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

Feature Description (continued)

8.3.4 Output Stage

The DRV5023 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using [Equation 1](#).

$$\frac{V_{\text{ref max}}}{30 \text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100 \mu\text{A}} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC} . The allowable voltage range of this pin is specified in the [Absolute Maximum Ratings](#).

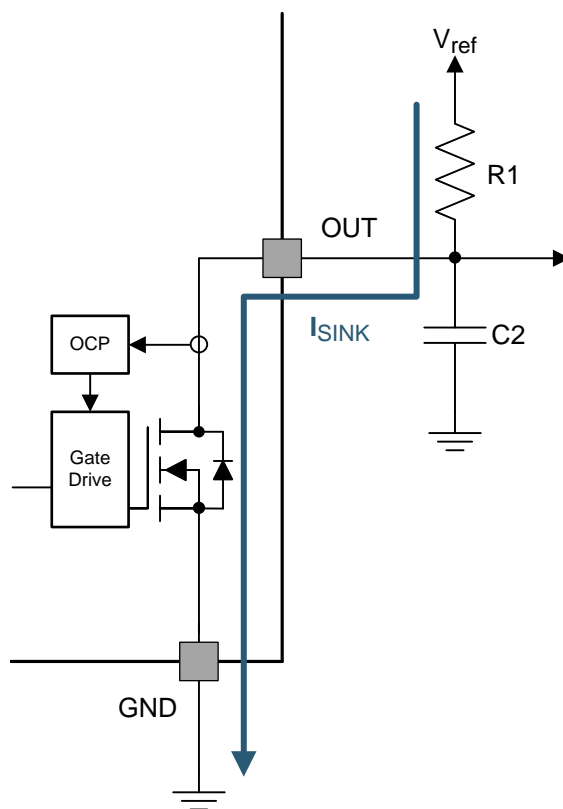


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in [Equation 2](#).

$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

8.3.5 Protection Circuits

The DRV5023 device is fully protected against overcurrent and reverse-supply conditions.

8.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

8.3.5.2 Load Dump Protection

The DRV5023 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand $V_{CC} = 40$ V. No current-limiting series resistor is required for this protection.

8.3.5.3 Reverse Supply Protection

The DRV5023 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the [Absolute Maximum Ratings](#).

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load Dump	$38\text{ V} < V_{CC} < 40\text{ V}$	Operating	Device will operate for a transient duration	$V_{CC} \leq 38\text{ V}$
Reverse Supply	$-22\text{ V} < V_{CC} < 0\text{ V}$	Disabled	Device will survive this condition	$V_{CC} \geq 2.5\text{ V}$

8.4 Device Functional Modes

The DRV5023 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

9 Application and Implementation

9.1 Application Information

The DRV5023 device is used in magnetic-field sensing applications.

9.2 Typical Application

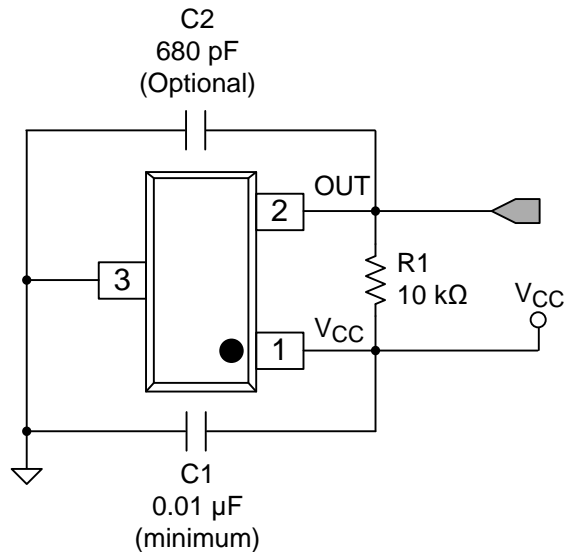


Figure 18. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

9.2.2 Detailed Design Procedure

Table 2. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-μF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

(1) REF is not a pin on the DRV5023 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC} .

9.2.2.1 Configuration Example

In a 3.3-V system, $3.2\text{ V} \leq V_{\text{ref}} \leq 3.4\text{ V}$. Use [Equation 3](#) to calculate the allowable range for R1.

$$\frac{V_{\text{ref max}}}{30\text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100\text{ }\mu\text{A}} \quad (3)$$

For this design example, use [Equation 4](#) to calculate the allowable range of R1.

$$\frac{3.4\text{ V}}{30\text{ mA}} \leq R1 \leq \frac{3.2\text{ V}}{30\text{ mA}} \quad (4)$$

Therefore:

$$113\text{ }\Omega \leq R1 \leq 32\text{ k}\Omega \quad (5)$$

After finding the allowable range of R1 ([Equation 5](#)), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use [Equation 6](#) to calculate the value of C2.

$$2 \times f_{\text{BW}}\text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (6)$$

For this design example, use [Equation 7](#) to calculate the value of C2.

$$2 \times 10\text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \quad (7)$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

9.2.3 Application Curves

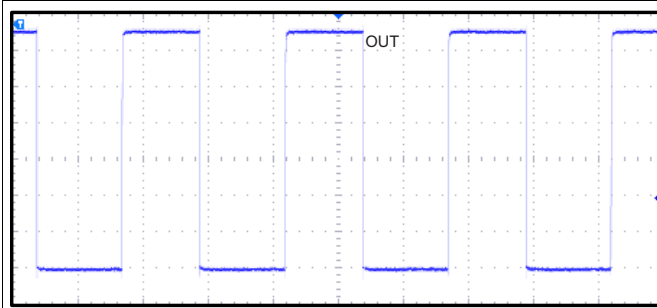


Figure 19. 10-kHz Switching Magnetic Field

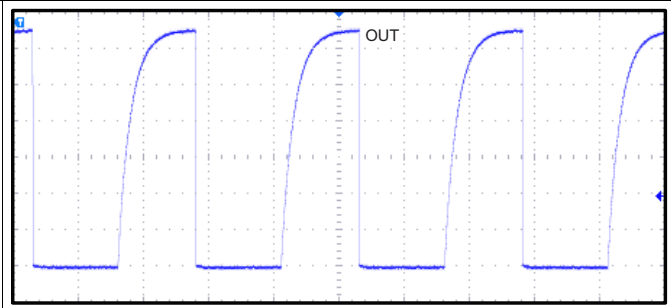


Figure 20. 10-kHz Switching Magnetic Field

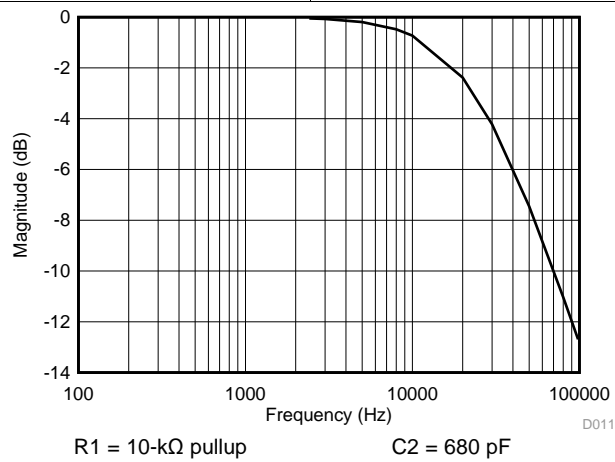


Figure 21. Low-Pass Filtering

10 Power Supply Recommendations

The DRV5023 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-μF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5023 device as possible.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 22 shows a legend for reading the complete device name for and DRV5023 device.

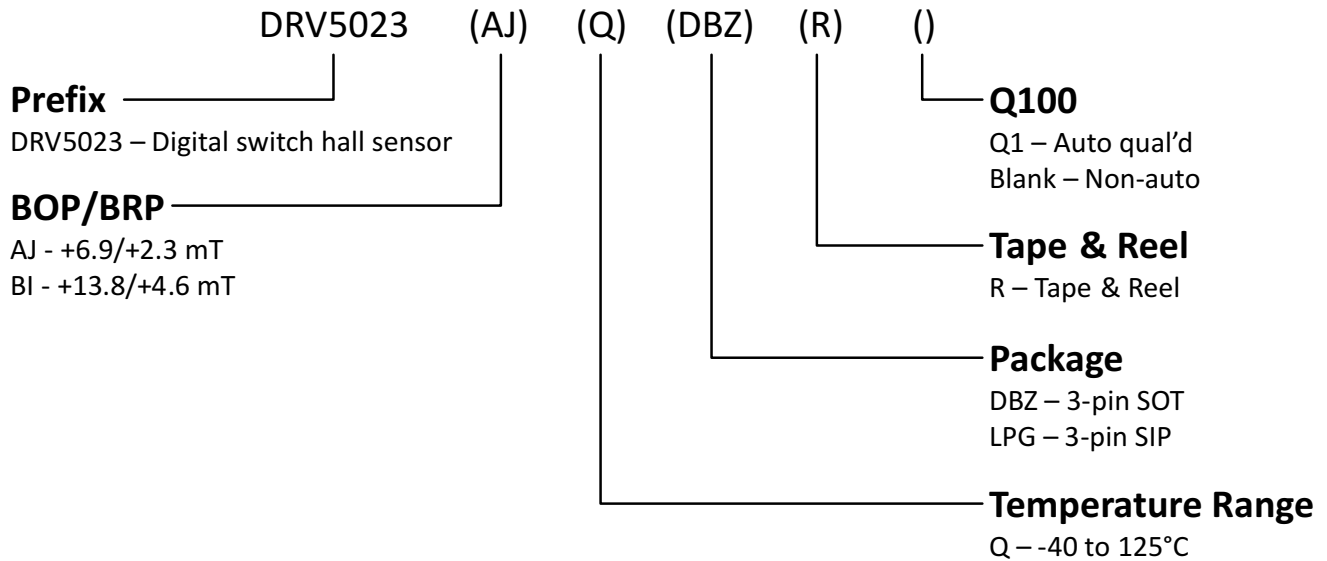


Figure 22. Device Nomenclature

11.1.2 Device Markings

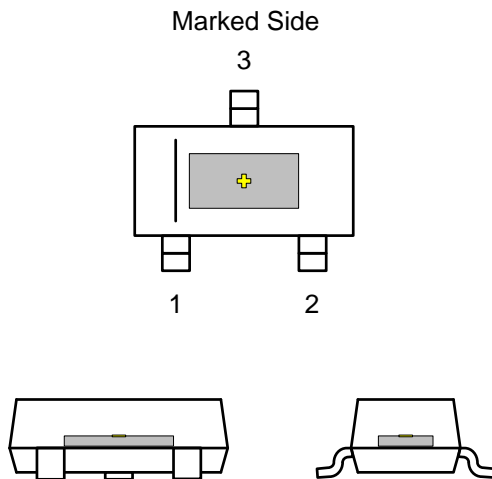


Figure 23. SOT-23 (DBZ) Package

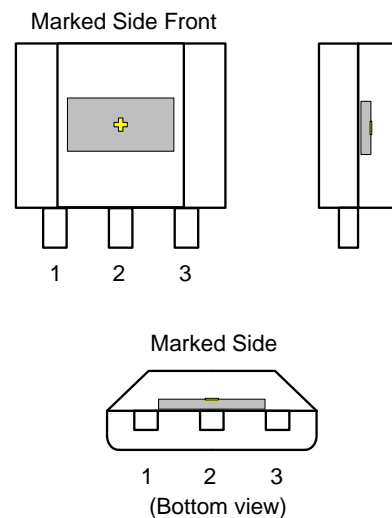


Figure 24. SIP (LPG) Package

✚ indicates the Hall Effect Sensor (not to scale). Located in the center of the package.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5023AJQDBZR	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		
DRV5023AJQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
DRV5023BIQDBZR	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		
DRV5023BIQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV5023AJQDBZT	PREVIEW	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125		
PDRV5023AJQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV5023BIQDBZT	PREVIEW	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125		
PDRV5023BIQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

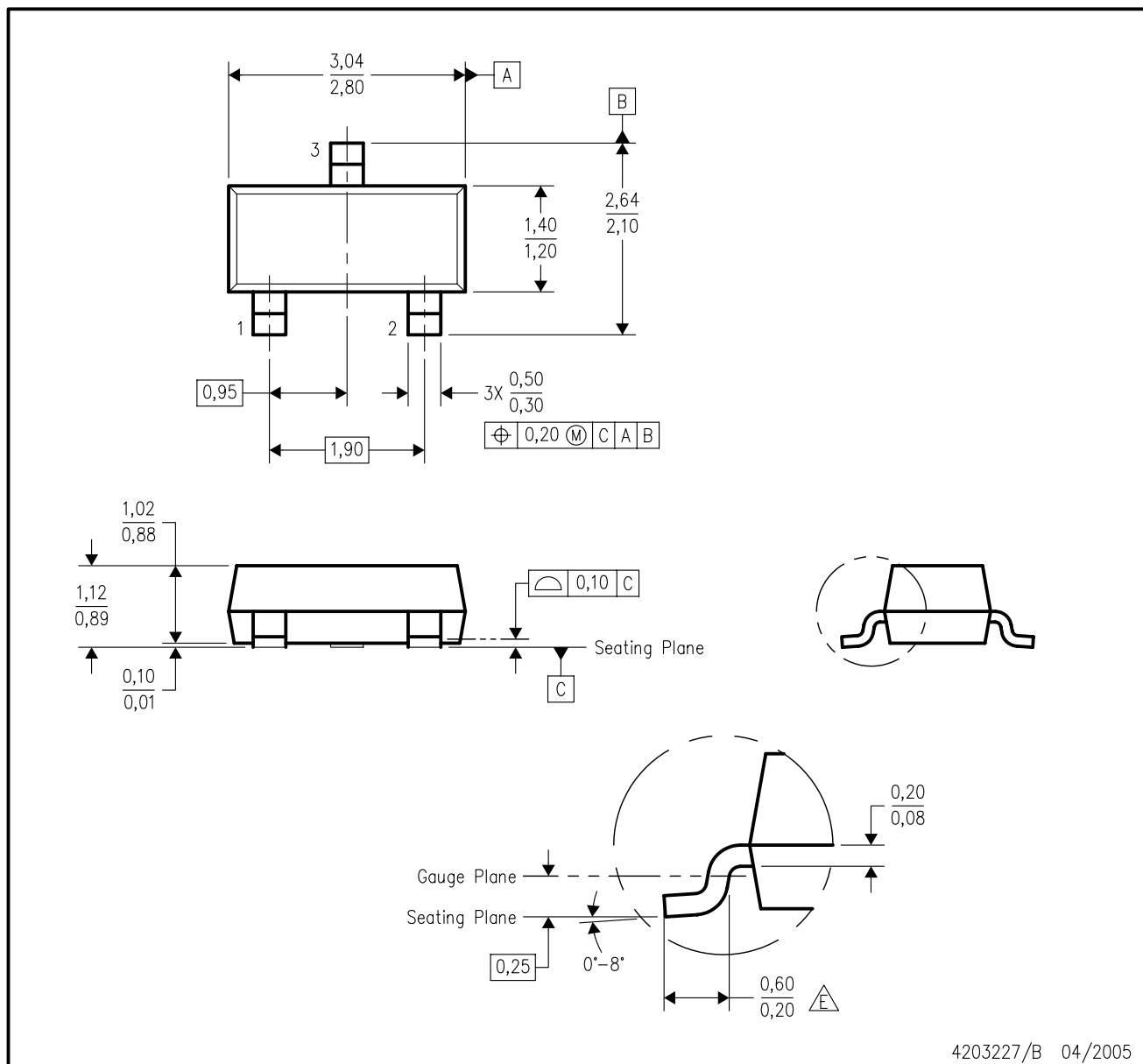
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DBZ (R-PDSO-G3)

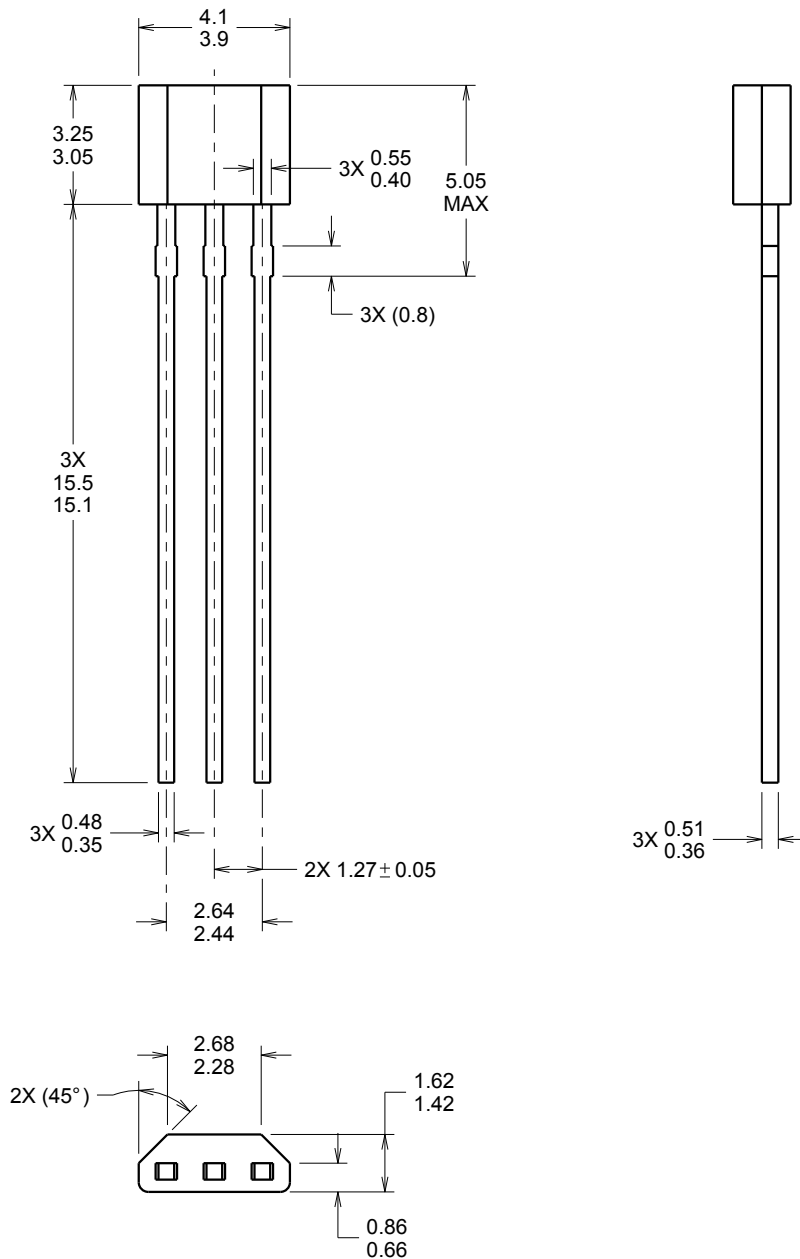
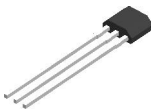
PLASTIC SMALL-OUTLINE



4203227/B 04/2005

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Lead dimensions are inclusive of plating.
- Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
- Falls within JEDEC TO-236 variation AB, except minimum foot length.



4221343/A 02/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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