



FemtoClock® Crystal-to-LVDS Clock Generator

844001I

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

DATA SHEET

GENERAL DESCRIPTION

The 844001I is a Fibre Channel Clock Generator. The 844001I uses an 18pF parallel resonant crystal over the range of 20.4MHz - 28.3MHz. For Fibre Channel applications, a 26.5625MHz crystal is used. The frequency select pin allows the device to generate either 106.25MHz or 212.5MHz from a 26.5625MHz crystal. To generate 187.5MHz for 12Gb Ethernet, a 23.4375MHz crystal is used. The 844001I uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Fibre Channel and Ethernet jitter requirements. The 844001I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

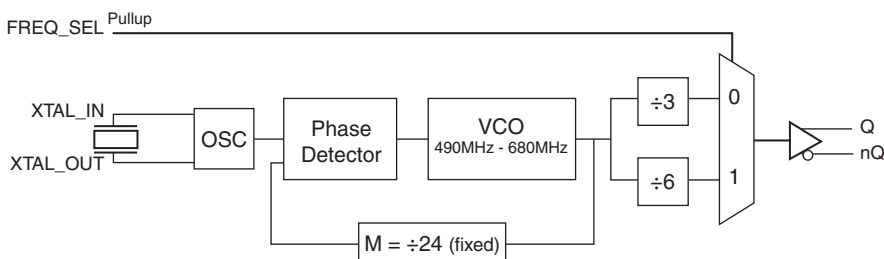
FEATURES

- One Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (20.4MHz - 28.3MHz)
- Output frequency range: 81.66MHz - 226.66MHz
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.74ps (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **For functional replacement part use 8T49N242**

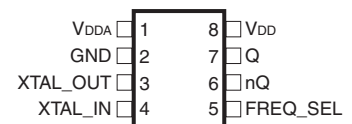
COMMON CONFIGURATION TABLE - FIBRE CHANNEL, 12Gb ETHERNET

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
26.5625	1	24	6	4	106.25
26.5625	0	24	3	8	212.5
23.4375	0	24	3	8	187.5

BLOCK DIAGRAM



PIN ASSIGNMENT



844001I

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{DDA}	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pullup	Frequency select pin.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V _{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	V_{DD}	V
I_{DD}	Power Supply Current				115	mA
I_{DDA}	Analog Supply Current				12	mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.12$	2.5	V_{DD}	V
I_{DD}	Power Supply Current				110	mA
I_{DDA}	Analog Supply Current				12	mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	FREQ_SEL $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	μA
I_{IL}	Input Low Current	FREQ_SEL $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			μA

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		350	415	480	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.225	1.325	1.425	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	390	480	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.0	1.2	1.325	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		20.4		28.3	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: It is not recommended to overdrive the crystal input with an external clock.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.66		226.66	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	106.25MHz @ Integration Range: 637kHz - 10MHz		0.74		ps
		187.5MHz @ Integration Range: 637kHz - 10MHz		0.48		ps
		212.5MHz @ Integration Range: 637kHz - 10MHz		0.70		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		500	ps
odc	Output Duty Cycle	FREQ_SEL = 1	48		52	%
		FREQ_SEL = 0	45		55	%

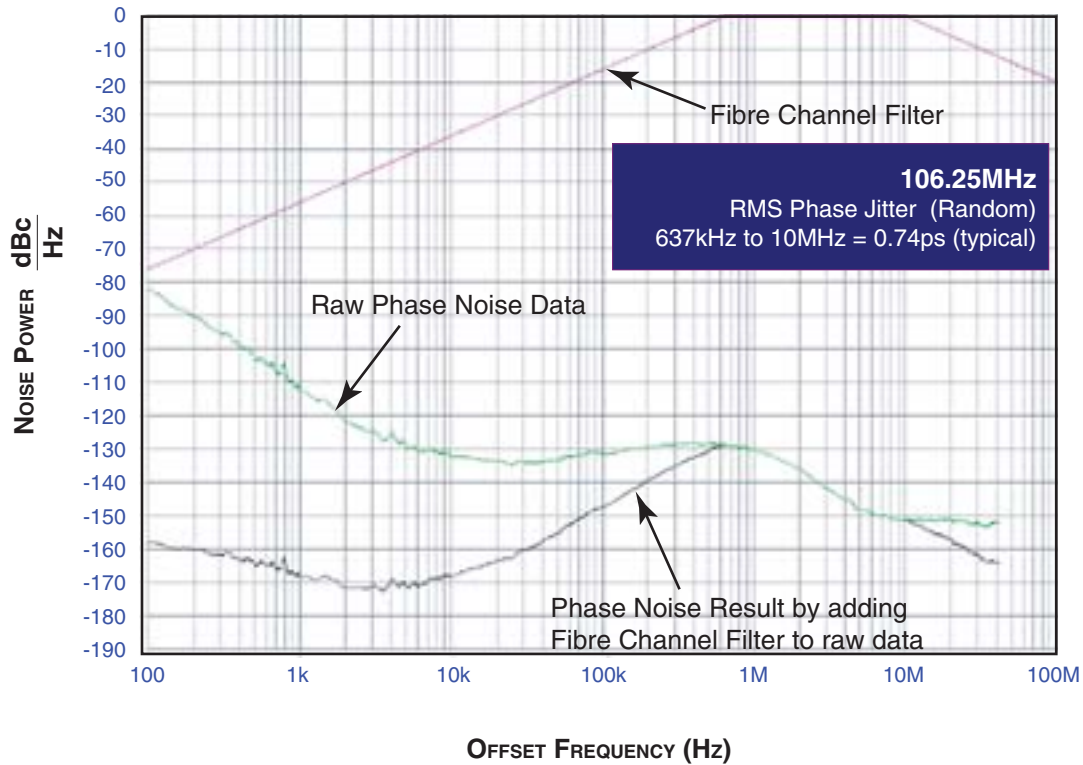
NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

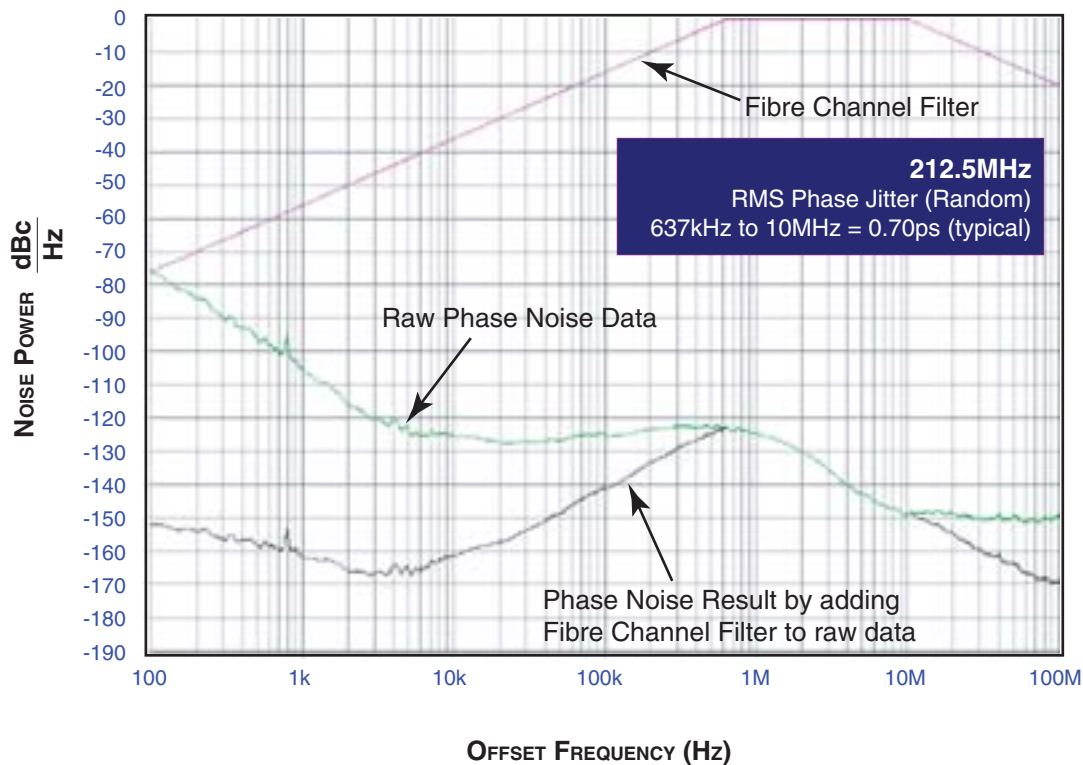
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		81.66		226.66	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	106.25MHz @ Integration Range: 637kHz - 10MHz		0.97		ps
		187.5MHz @ Integration Range: 637kHz - 10MHz		0.58		ps
		212.5MHz @ Integration Range: 637kHz - 10MHz		0.95		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		500	ps
odc	Output Duty Cycle	FREQ_SEL = 1	48		52	%
		FREQ_SEL = 0	45		55	%

NOTE 1: Please refer to the Phase Noise Plots following this section.

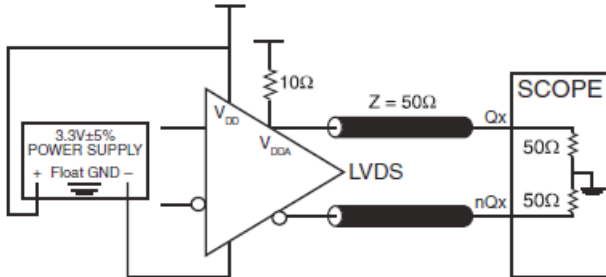
TYPICAL PHASE NOISE AT 106.25MHz @3.3V



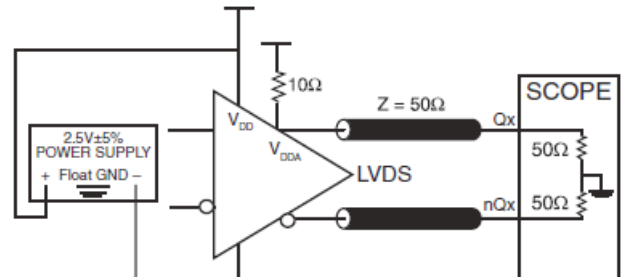
TYPICAL PHASE NOISE AT 212.5MHz @3.3V



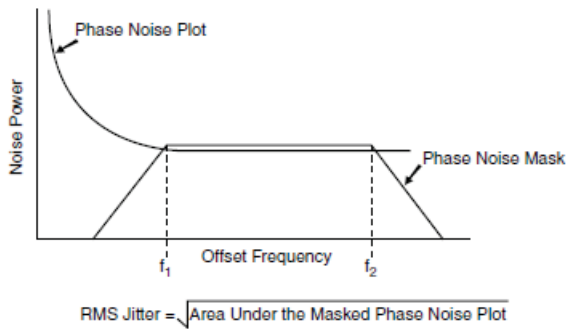
PARAMETER MEASUREMENT INFORMATION



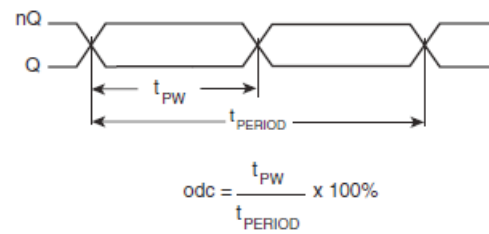
LVDS 3.3V OUTPUT LOAD TEST CIRCUIT



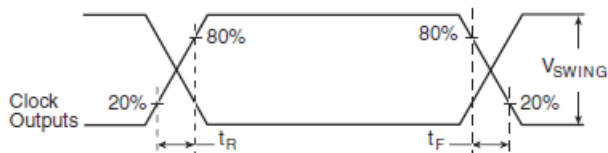
LVDS 2.5V OUTPUT LOAD TEST CIRCUIT



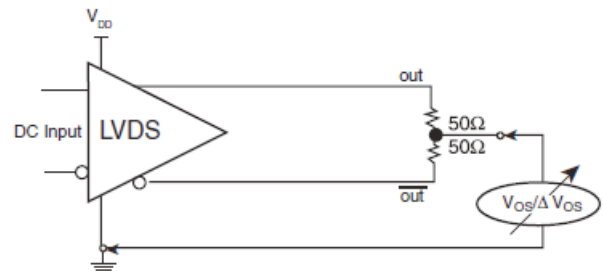
RMS PHASE JITTER



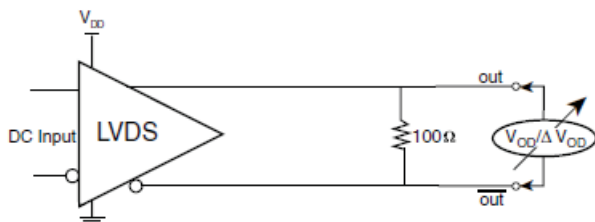
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 844001I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} pin.

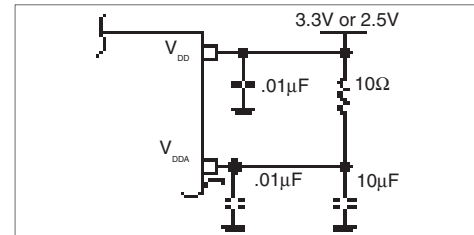


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 844001I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

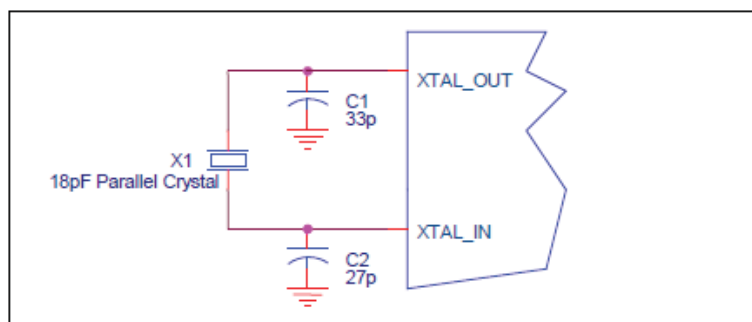


Figure 2. CRYSTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

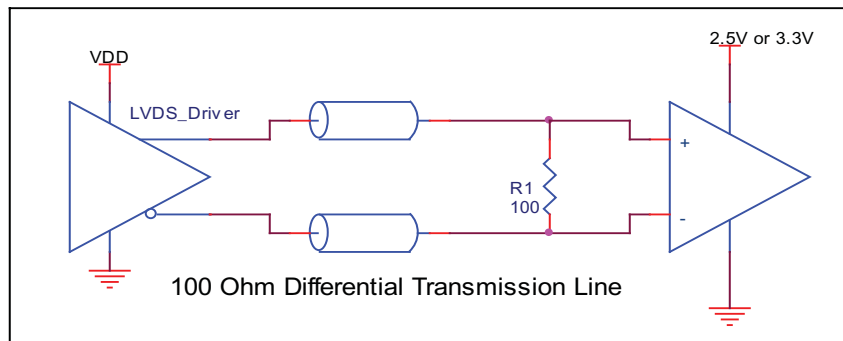


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844001I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844001I is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (115mA + 12mA) = 440mW$

2. Junction Temperature.

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_J is as follows: $T_J = \theta_{JA} * Pd_total + T_A$

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, T_J for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.440W * 90.5^\circ C/W = 124.8^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W
NOTE: An airflow of 1 meter per second is strongly recommended.			

TRANSISTOR COUNT

The transistor count for 844001I is: 2533

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

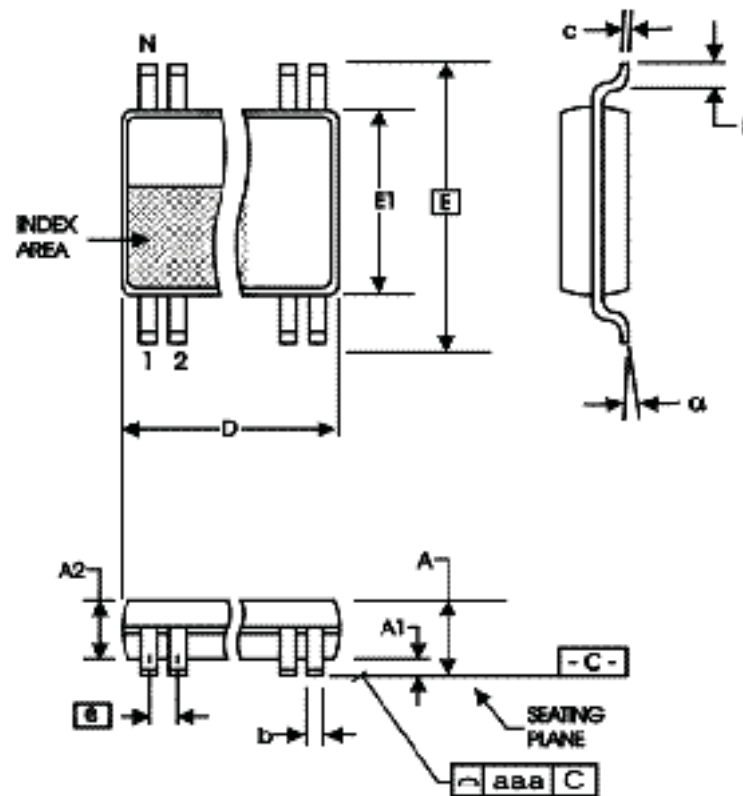


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844001AGILF	01AIL	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844001AGILFT	01AIL	8 lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology, Incorporated (IDT) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T4	1	Deleted HiPerClockS references.	11/5/12
		4	Crystal Characteristics Table - added note.	
		8	Deleted application note, LVCMOS to XTAL Interface.	
		12	Deleted quantity from tape and reel.	
A	T9	12	Ordering Information - removed leaded devices. Updated data sheet format.	10/26/15
A			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	6/2/16

**Corporate Headquarters**

6024 Silver Creek Valley Road
San Jose, California 95138

Sales

800-345-7015 or +408-284-8200
Fax: 408-284-2775
www.IDT.com

Technical Support

email: clocks@idt.com

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2016. All rights reserved.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[IDT \(Integrated Device Technology\):](#)

[844001AGILF](#) [844001AGILFT](#)