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LV5725JA

Bi-CMOS LSI

Step-down Switching Regulator

Overview

The LV5725JA is a step-down voltage switching regulator.

Functions

- Wide input dynamic range: 4.5V to 50V.
- Built-in pulse-by-pulse OCP circuit: detection is on resistance of an external MOS.
- Over current protection: HICCUP mode.
- Load-independent soft start circuit
- Synchronous operation by external signal.
- External voltage is usable when output voltage is high.
- Current mode type.
- Thermal shutdown.
- ON/OFF pin
- Power good pin

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{IN} max		55	V
Allowable pin voltage	V _{IN} , SW, OUT, PGOOD		55	V
	HDRV, CBOOT		61	V
	LDRV		6.0	V
	Between CBOOT to SW		6.0	V
	Between CBOOT to HDRV			
	EN, ILIM		V _{IN} +0.3	V
	Between V _{IN} to ILIM		1.0	V
	V _{DD}		6.0	V
	SS, FB, COMP, RT, SYNC		V _{DD} +0.3	V
Allowable Power dissipation	Pd max	Mounted on a specified board. *	1.45	W
Operating temperature	T _{opr}		-40 to +85	°C
Storage temperature	T _{stg}		-55 to +150	°C
Parameter	Symbol	Conditions	Ratings	Unit
Maximum junction temperature	T _J max		150	°C

* Specified board : 58.0mm × 78.0mm × 1.6mm, fiberglass epoxy printed board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V _{IN}		4.5 to 50	V
Error amplifier input voltage	V _{FB}		0 to 1.6	V
Oscillatory frequency	F _{OSC}		50 to 500	kHz

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	V _{ref}	Including offset of E/A	0.698	0.708	0.718	V
5V power supply	V _{DD}	I _{OUT} = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	F _{OSC}	RT= 56kΩ	317	365	412	kHz
Frequency variation	F _{OSC} DV	V _{IN} = 4.5 to 50V		1		%
Fold back detection voltage	V _{OSC} FB	After power is supplied to SS, voltage is detected FB.		0.5		V
Fold back oscillation frequency	F _{OSC} FB	RT= 56kΩ, V _{FB} = 0V	100	130	160	kHz
ON/OFF circuit block						
IC start-up voltage	V _{EN} on		-	2.5	3.0	V
Hysteresis of startup voltage	V _{EN} hys		0.3	0.6	-	V
Soft start circuit block						
Soft start source current	I _{SS} SC	EN > 3.0V	4	5	6	μA
Soft start sink current	I _{SS} SK	EN < 1V, V _{DD} = 5V		2		mA
Soft start end voltage	V _{SS} END		0.7	0.9	1.1	V
UVLO circuit block						
UVLO voltage	V _{UVLO}		3.7	4.0	4.3	V
Hysteresis of UVLO	V _{UVLO} H			0.3		V
Error amplifier						
Input bias current	I _{EA} IN				100	nA
Error amplifier gain	G _{EA}		1000	1400	1800	μA/V
Range of common-mode input voltage	V _{EA} R	V _{IN} = 4.5 to 50V	0		1.6	V
Output sink current	I _{EA} OSK	FB = 1.0V		-100		μA
Output source current	I _{EA} OSC	FB = 0V		100		μA
Current detection amplifier gain	G _{ISNS}			2.4		
Over current limiter circuit block						
Reference current	I _{LIM}		-10%	20	+10%	μA
Over current detection comparator offset voltage	V _{LIM} _OFS		-5		+5	mV
Range of over current detection comparator common mode input	V _{LIM} _CM		V _{IN} -0.45		V _{IN}	V
PWM comparator						
Input threshold voltage	V _t max	Duty cycle = D _{MAX} , SW = V _{IN}	1.15	1.25	1.35	V
	V _{t0}	Duty cycle = 0%, SW = V _{IN}	0.5	0.6	0.7	V
Maximum ON duty	D _{MAX}		92			%

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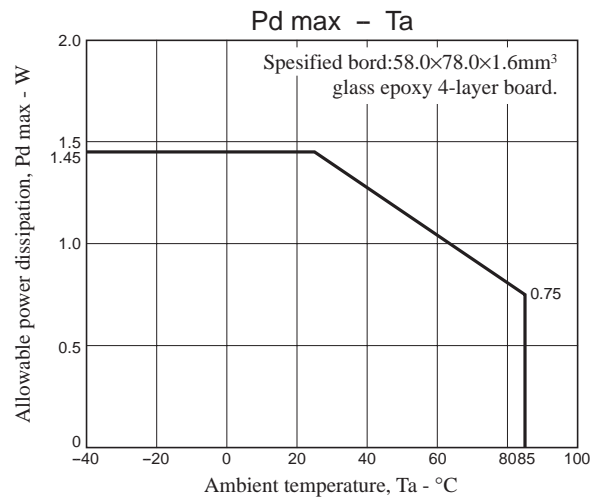
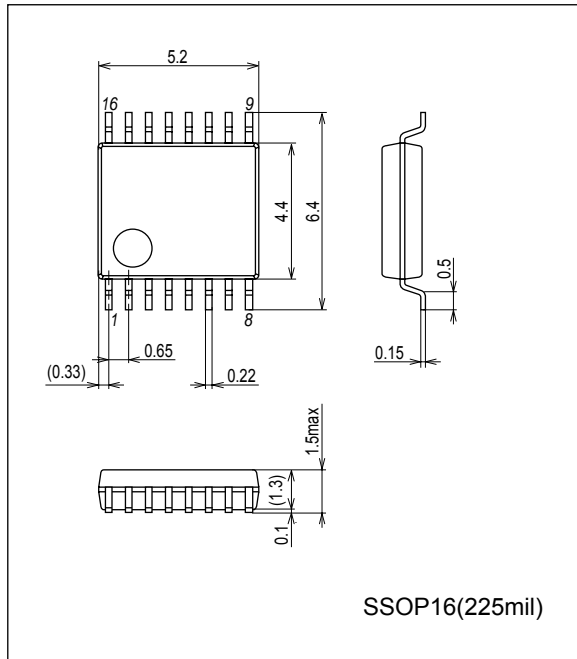
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power good						
Power good “L” sink current	I _{PGL}	PGOOD = 5V		5		mA
Power good “H” sink current	I _{PGH}	PGOOD = 5V			1	μA
Power good voltage	P _G thresh	When FB voltage rises		0.612		V
Hysteresis of power good	P _G hys			12		mV
Output block						
High side output ON resistance (upper)	R _{ONH_HIGH}	CBOOT – HDRV = -0.1V		12		Ω
High side output ON resistance (lower)	R _{ONL_HIGH}	HDRV – SW = +0.1V		3.3		Ω
Low side output ON resistance (upper)	R _{ONH_LOW}	V _{DD} – LDRV = -0.1V		7.9		Ω
Low side output ON resistance (lower)	R _{ONL_LOW}	LDRV – GND = +0.1V		3.8		Ω
High side output ON current (upper)	I _{ONH_HIGH}	CBOOT – HDRV = -4.5V	160			mA
High side output ON current (lower)	I _{ONL_HIGH}	HDRV – SW = +4.5V	330			mA
Low side output ON current (upper)	I _{ONH_LOW}	V _{DD} – LDRV = -5.2V	190			mA
Low side output ON current (lower)	I _{ONL_LOW}	LDRV – GND = +5.2V	250			mA
Entire device						
Standby current	I _{CCS}	EN < 1V			1	μA
Average current consumption	I _{CCA}	EN > 3.0V		2.5		mA

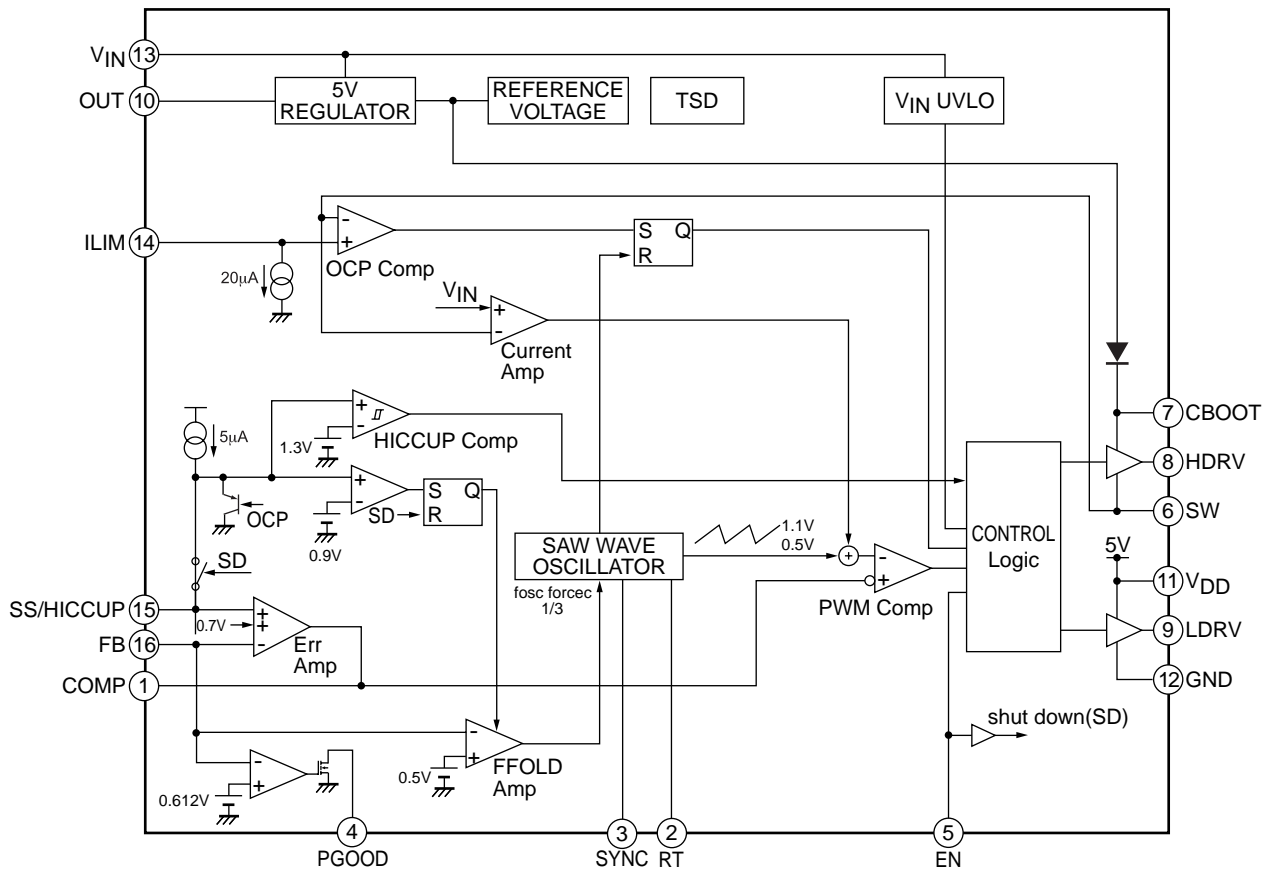
Package Dimensions

unit : mm (typ)

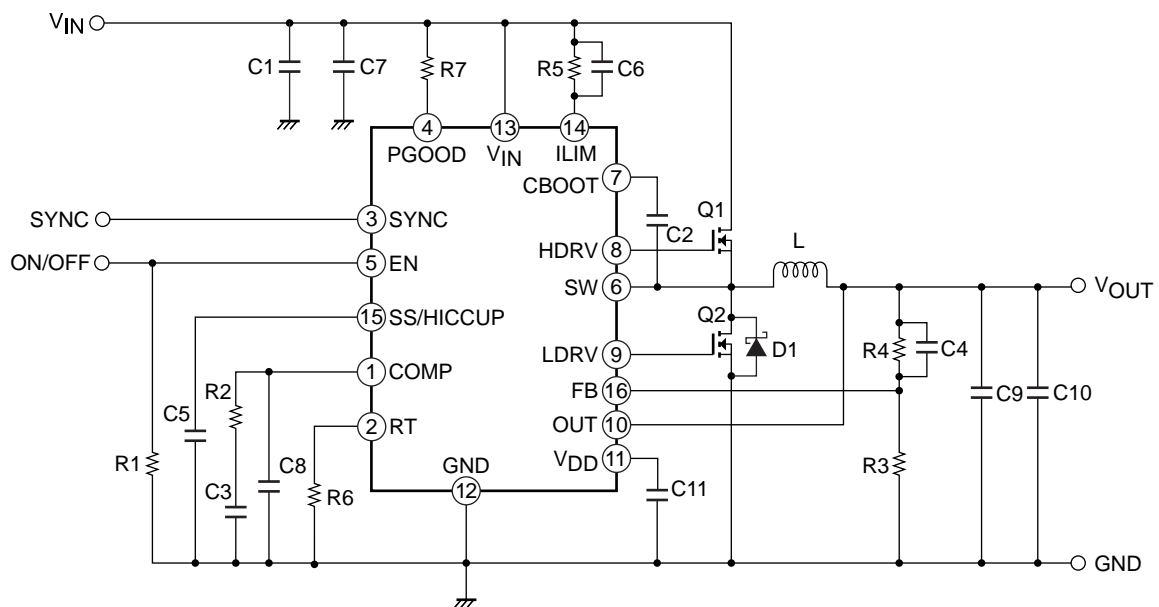
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Block Diagram

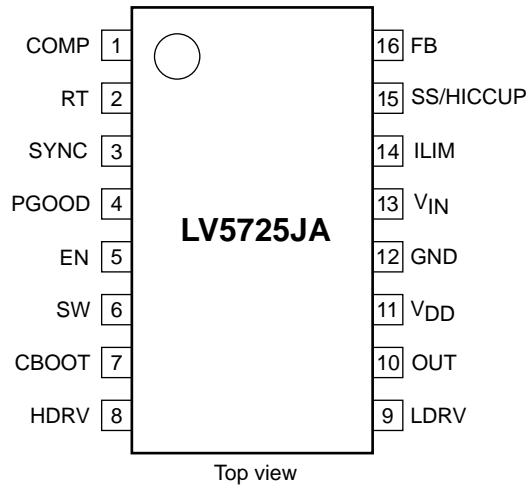


Sample application circuit



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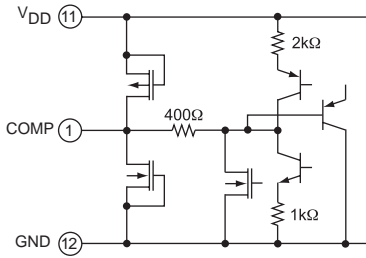
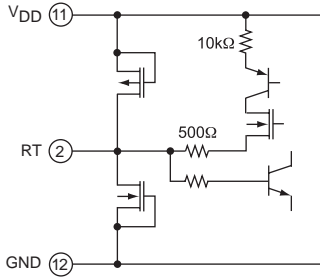
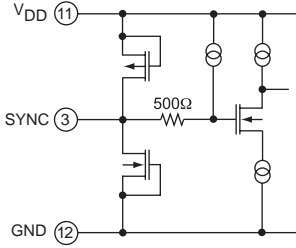
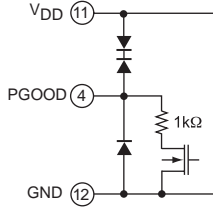
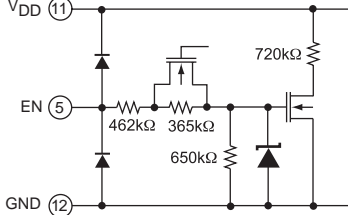
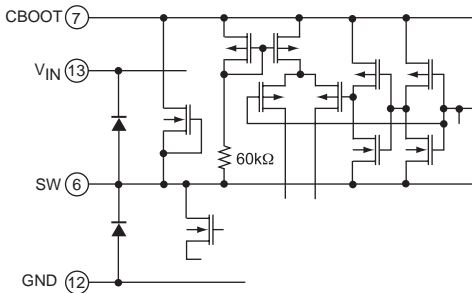
Pin Assignment



Pin Function

Pin No.	Pin name	Description
1	COMP	Error amplifier output pin. Make sure to connect a phase compensation network between COMP and GND.
2	RT	Oscillating frequency setting pin. Make sure to connect a resistor between this pin and GND.
3	SYNC	External synchronous signal input pin.
4	PGOOD	Power good pin.
5	EN	ON/OFF pin.
6	SW	This pin is connected to switching node. Connect the source of Nch MOSFET to this pin.
7	CBOOT	Bootstrap capacitor connected pin. This pin is used as gate driving power supply for external Nch MOSFET. Make sure to connect a capacitor between CBOOT and SW.
8	HDRV	External upper MOSFET gate driving pin.
9	LDRV	External lower MOSFET gate driving pin.
10	OUT	Internal regulator power supply pin. This pin is connected to V_{OUT} .
11	V_{DD}	Power supply pin for gate drive of the external lower MOS-FET.
12	GND	Ground pin. GND pin voltage is the reference for each reference voltage.
13	V_{IN}	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes higher than 4.3V by UVLO function, the IC starts up and mode shifts to soft start operation.
14	ILIM	Reference current pin for current detection. The inlet current of approx. 20 μ A flows into this pin. Connect a resistor externally between this pin and V_{IN} and when the voltage supplied to SW pin is lower than the pin voltage of this resistor, the upper Nch MOSFET is turned off by current limiter comparator. This operation is reset at every PWM pulse.
15	SS/HICCUP	Capacitor connection pin for soft start. This pin enables to charge the soft start capacitor by 5 μ A. (approx) When this pin turns approx. 0.9V, soft start period ends and frequency fold back function is activated.
16	FB	Error amplifier reverse input pin. Converter operates to set this pin to 0.708V. The output voltage divided by the external resistance is applied to this pin. After soft start, frequency fold back function operates when the voltage of this pin becomes 0.5V or lower. And oscillating frequency decreases together with FB voltage.

I/O pin equivalent circuit chart

Pin No.	Pin No.	Equivalent Circuit
1	COMP	
2	RT	
3	SYNC	
4	PGOOD	
5	EN	
6	SW	

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Pin No.	Pin No.	Equivalent Circuit
7	CBOOT	
8	LDRV	
9	HDRV	
10	OUT	
11	V _{DD}	
12, 13	GND, V _{IN}	
14	ILIM	

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Pin No.	Pin No.	Equivalent Circuit
15	SS/HICCUP	
16	FB	

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