

3.3V Dual Micropower High-Side/Low-Side MOSFET Driver

FEATURES

- Allows Lowest Drop 3.3V Supply Switching
- Operates on 3.3V or 5V Nominal Supplies
- 3 Microamps Standby Current
- 80 Microamps ON Current
- Drives Low Cost N-Channel Power MOSFETs
- No External Charge Pump Components
- Controlled Switching ON and OFF Times
- Compatible with 3.3V and 5V Logic Families
- Available in 8-Pin SOIC

APPLICATIONS

- Notebook Computer Power Management
- Palmtop Computer Power Management
- P-Channel Switch Replacement
- Battery Charging and Management
- Mixed 5V and 3.3V Supply Switching
- Stepper Motor and DC Motor Control
- Cellular Telephones and Beepers

DESCRIPTION

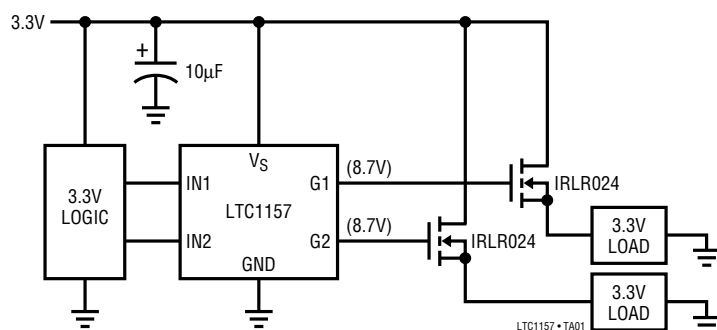
The LTC1157 dual 3.3V micropower MOSFET gate driver makes it possible to switch either supply or ground reference loads through a low $R_{DS(ON)}$ N-channel switch (N-channel switches are required at 3.3V because P-channel MOSFETs do not have guaranteed $R_{DS(ON)}$ with $V_{GS} \leq 3.3V$). The LTC1157 internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground), fully enhancing a logic level N-channel switch for 3.3V high-side applications and a standard N-channel switch for 3.3V low-side applications. The gate drive voltage at 5V is typically 8.8V above supply (13.8V above ground), so standard N-channel MOSFET switches can be used for both high-side and low-side applications.

Micropower operation, with 3 μ A standby current and 80 μ A operating current, makes the LTC1157 well suited for battery-powered applications.

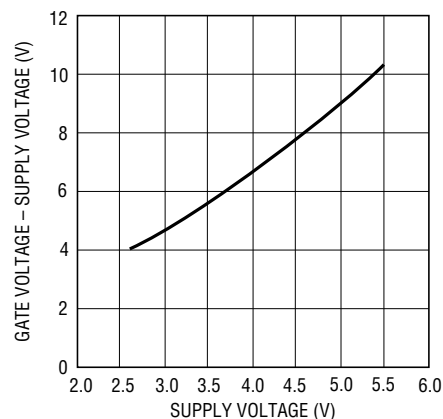
The LTC1157 is available in both 8-pin DIP and SOIC.

TYPICAL APPLICATION

Ultra Low Voltage Drop 3.3V Dual High-Side Switch



Gate Voltage Above Supply



LTC1157 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -0.3V to 7V
 Any Input Voltage $(V_S + 0.3\text{V})$ to $(\text{GND} - 0.3\text{V})$
 Any Output Voltage $(V_S + 12\text{V})$ to $(\text{GND} - 0.3\text{V})$
 Current (Any Pin) 50mA

Operating Temperature Range

LTC1157C 0°C to 70°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PLASTIC DIP $T_{JMAX} = 100^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$	ORDER PART NUMBER	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 100^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$	ORDER PART NUMBER
	LTC1157CN8		LTC1157CS8
			S8 PART MARKING
			1157

ELECTRICAL CHARACTERISTICS $V_S = 2.7\text{V}$ to 5.5V , $T_A = 25^\circ\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1157C			UNITS
				MIN	TYP	MAX	
I _Q	Quiescent Current OFF	V _S = 3.3V, V _{IN1} = V _{IN2} = 0V (Note 1)			3	10	μA
	Quiescent Current ON	V _S = 3.3V, V _{IN} = 3.3V (Note 2)			80	160	μA
		V _S = 5V, V _{IN} = 5V (Note 2)			180	400	μA
V _{INH}	Input High Voltage		●	70% × V _S			V
V _{INL}	Input Low Voltage		●	15% × V _S			V
I _{IN}	Input Current	0V ≤ V _{IN} ≤ V _S	●	±1			μA
C _{IN}	Input Capacitance			5			pF
V _{GATE} – V _S	Gate Voltage Above Supply	V _S = 3V	●	4.0	4.7	6.5	V
		V _S = 3.3V	●	4.5	5.4	7.0	V
		V _S = 5V	●	7.5	8.8	12.0	V
t _{ON}	Turn-ON Time	V _S = 3.3V, C _{GATE} = 1000pF					
		Time for V _{GATE} > V _S + 1V		30	130	300	μs
		Time for V _{GATE} > V _S + 2V		75	240	750	μs
		V _S = 5V, C _{GATE} = 1000pF					
		Time for V _{GATE} > V _S + 1V		30	85	300	μs
		Time for V _{GATE} > V _S + 2V		75	230	750	μs
t _{OFF}	Turn-OFF Time	V _S = 3.3V, C _{GATE} = 1000pF					
		Time for V _{GATE} < 0.5V		10	36	60	μs
		V _S = 5V, C _{GATE} = 1000pF					
		Time for V _{GATE} < 0.5V		10	31	60	μs

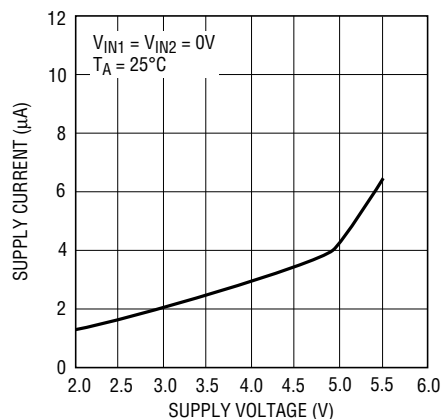
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Quiescent current OFF is for both channels in OFF condition.

Note 2: Quiescent current ON is per driver and is measured independently.

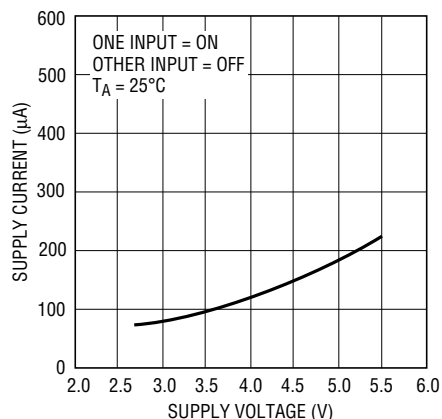
TYPICAL PERFORMANCE CHARACTERISTICS

Standby Supply Current



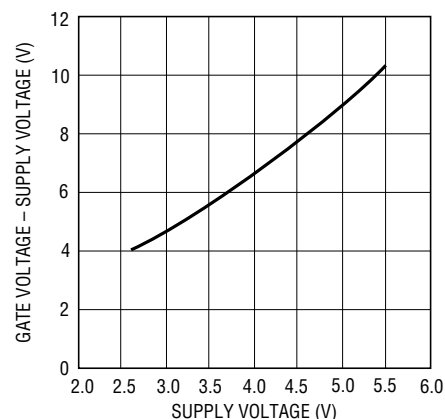
LTC1157 • TPC01

Supply Current per Driver ON



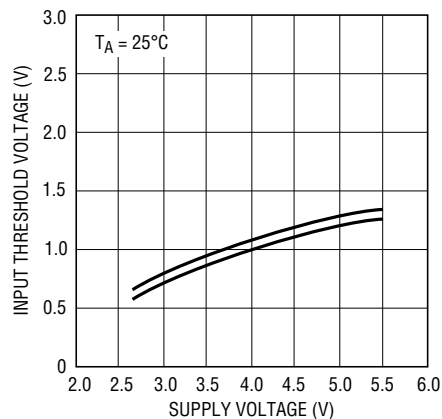
LTC1157 • TPC02

Gate Voltage Above Supply



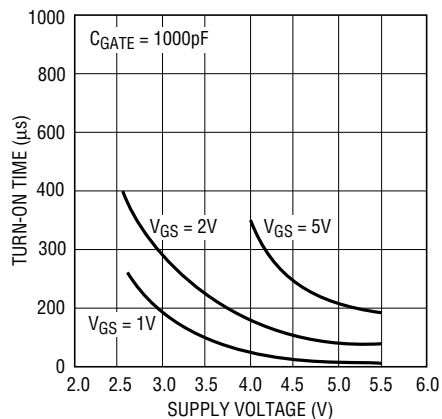
LTC1157 • TPC03

Input Threshold Voltage



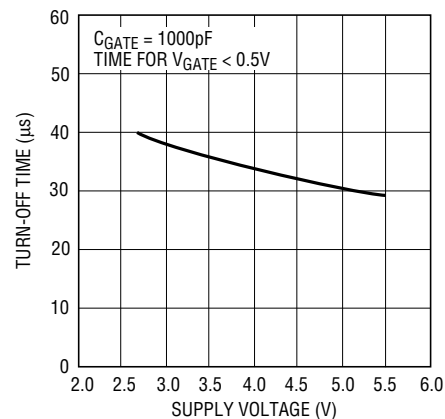
LTC1157 • TPC04

Turn-ON Time



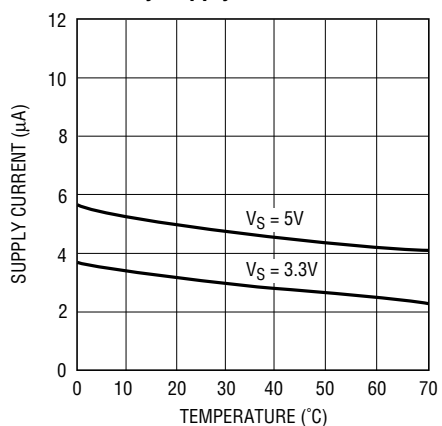
LTC1157 • TPC05

Turn-OFF Time



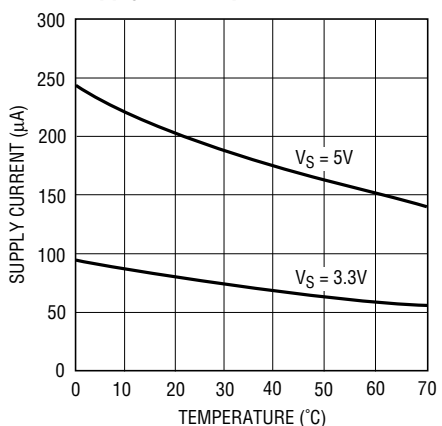
LTC1157 • TPC06

Standby Supply Current



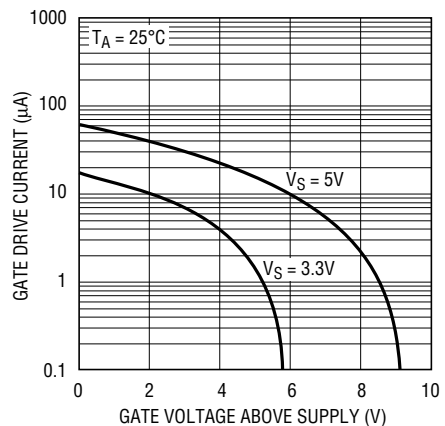
LTC1157 • TPC07

Supply Current per Driver ON



LTC1157 • TPC08

Gate Drive Current



LTC1157 • TPC09

PIN FUNCTIONS

Input Pins: The LTC1157 input pins are active high and activate the charge pump circuitry when switched ON. The LTC1157 logic inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails.

Gate Drive Pins: The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a

relatively high impedance when driven above the rail (the equivalent of a few hundred k Ω). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin: *The supply pin of the LTC1157 should never be forced below ground as this may result in permanent damage to the device.* A 300 Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

OPERATION

The LTC1157 is a dual micropower MOSFET driver designed specifically for operation at 3.3V and 5V and includes the following functional blocks:

3.3V Logic Compatible Inputs

The LTC1157 inputs have been designed to accommodate a wide range of 3.3V and 5V logic families. Approximately 50mV of hysteresis is provided to ensure clean switching.

An ultra low standby current voltage regulator provides continuous bias for the logic-to-CMOS converter. The logic-to-CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to an absolute minimum in the standby mode.

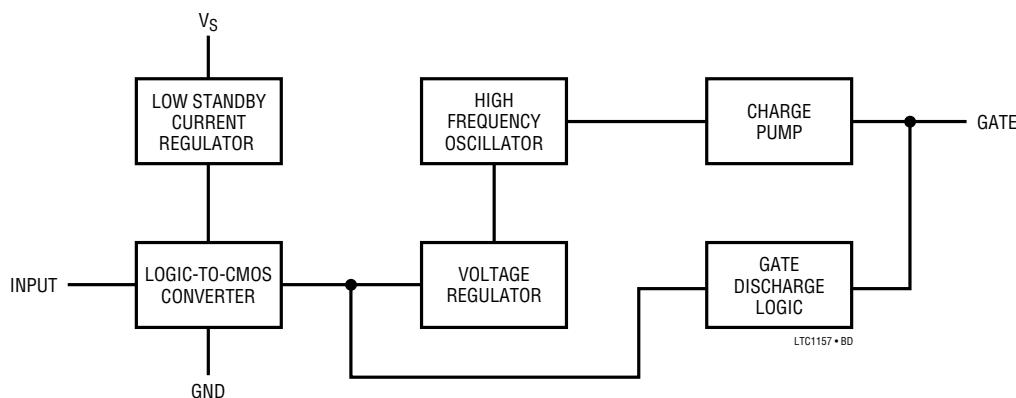
Gate Charge Pump

Gate drive for the power MOSFET is produced by an internal charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and therefore no external components are required to generate the gate drive.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

MOSFET Selection

The LTC1157 is designed to operate with both standard and logic level N-channel MOSFET switches. The choice of switch is determined primarily by the operating supply voltage.

Logic Level MOSFET Switches at 3.3V

Logic level switches should be used with the LTC1157 when powered from 2.7V to 4V. Although there is some variation among manufacturers, logic level MOSFET switches are typically rated with $V_{GS} = 4V$ with a maximum continuous V_{GS} rating of $\pm 10V$. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic level MOSFETs are frequently designated by an “L” and are usually available in surface mount packaging. Some logic level MOSFETs are rated up to $\pm 15V$ and can be used in applications which require operation over the entire 2.7V to 5.5V range.

Standard MOSFET Switches at 5V

Standard N-channel MOSFET switches should be used with the LTC1157 when powered from 4V to 5.5V supply as the built-in charge pump produces ample gate drive to fully enhance these switches when powered from a 5V nominal supply. Standard N-channel MOSFET switches are rated with $V_{GS} = 10V$ and are generally restricted to a maximum of $\pm 20V$.

Powering Large Capacitive Loads

Electrical subsystems in portable battery-powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly powered however, these capacitors may themselves become the source of supply glitching.

For example, if a $100\mu F$ capacitor is powered through a switch with a slew rate of $0.1V/\mu s$, the current during start-up is:

$$\begin{aligned} I_{START} &= C(dV/dt) \\ &= (100 \times 10^{-6}) (1 \times 10^5) \\ &= 10A \end{aligned}$$

Obviously, this is too much current for the regulator (or output capacitor) to supply and the output will glitch by as much as a few volts.

The start-up current can be substantially reduced by limiting the slew rate at the gate of an N-channel switch as shown in Figure 1. The gate drive output of the LTC1157

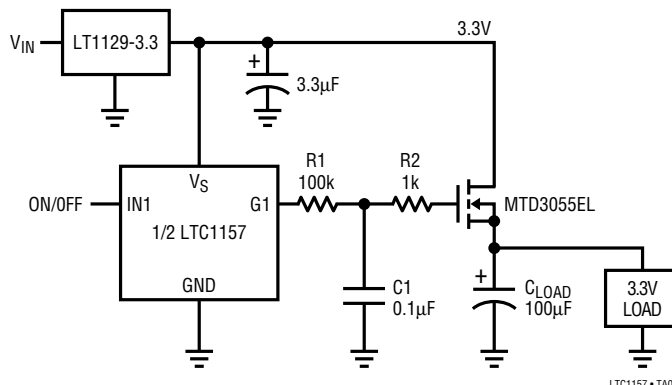


Figure 1. Powering a Large Capacitive Load

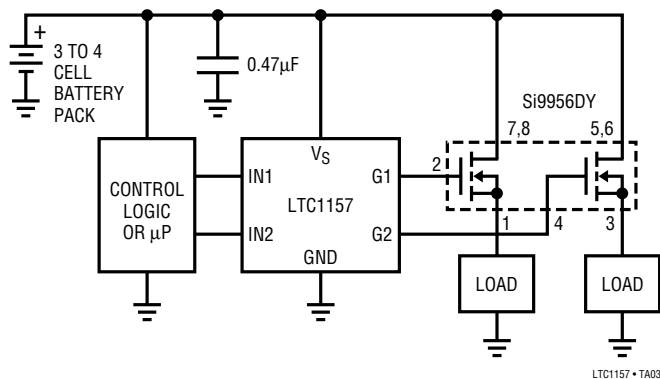
is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately $1.5 \times 10^{-4} V/\mu s$. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the start-up current to approximately 15mA which is easily managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. Also, it is good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Reverse Battery Protection

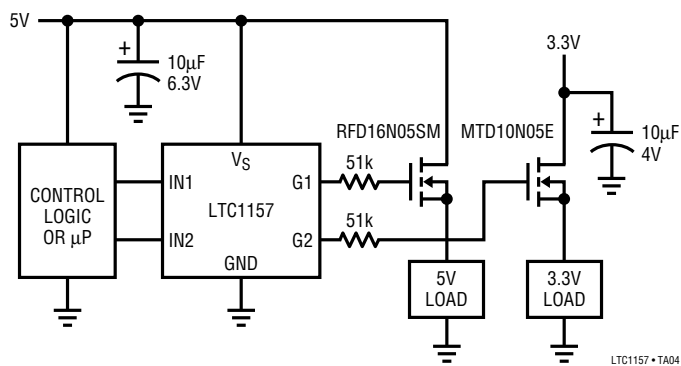
The LTC1157 can be protected against reverse battery conditions by connecting a 300Ω resistor in series with the ground pin. The resistor limits the supply current to less than 12mA with $-3.6V$ applied. Since the LTC1157 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 3.3V μP (or control logic) can be protected by adding 10k resistors in series with the input pins.

TYPICAL APPLICATIONS

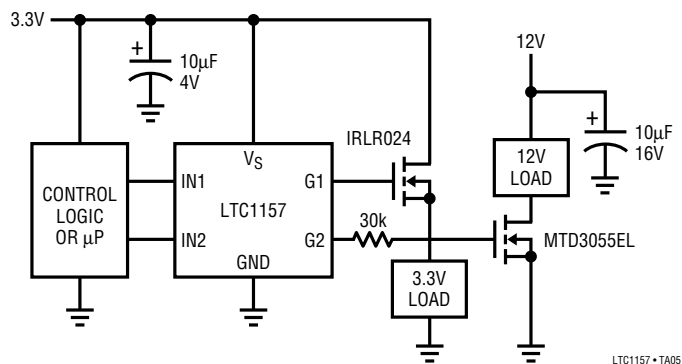
Ultra Low Drop 3 to 4 Cell Dual High-Side Switch



Mixed 5V and 3.3V Dual High-Side Switch



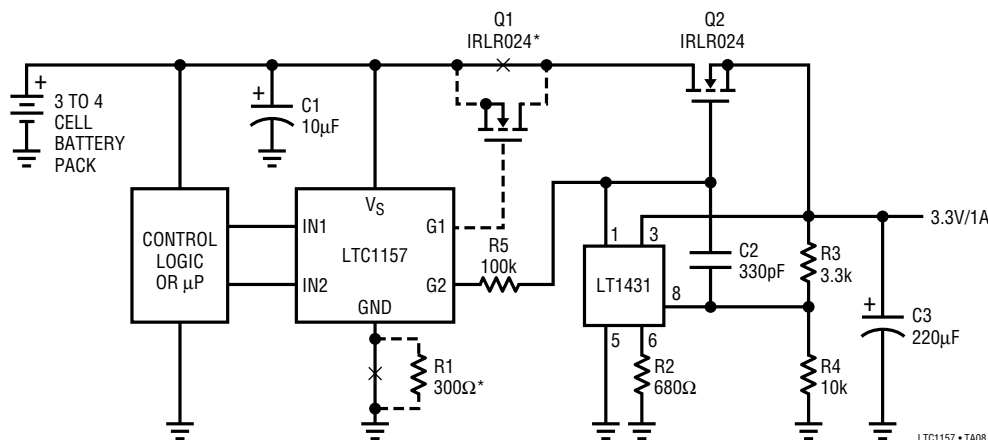
Mixed 3.3V and 12V High- and Low-Side Switching



The schematic diagram illustrates a switched (ramped) battery circuit. A 3 TO 4 CELL BATTERY PACK is connected to the input of the LTC1157. The LTC1157 is configured with its IN1 pin connected to the battery pack, IN2 pin connected to GND, and G1 pin connected to the output. The output of the LTC1157 is connected to a 100k resistor, which is in series with a 1k resistor. The output of the 1k resistor is connected to a 0.1μF capacitor. The output of the capacitor is connected to a 100μF capacitor, which is connected to the output of the circuit. The output of the circuit is labeled SWITCHED (RAMPED) BATTERY. The LTC1157 is also connected to a 300Ω resistor at its G2 pin. The output of the LTC1157 is also connected to a 0.47μF capacitor. The output of the 0.47μF capacitor is connected to a 5,6,7,8 pin header. The output of the 5,6,7,8 pin header is connected to the output of the circuit. The output of the circuit is also connected to a 100μF capacitor, which is connected to the output of the circuit.

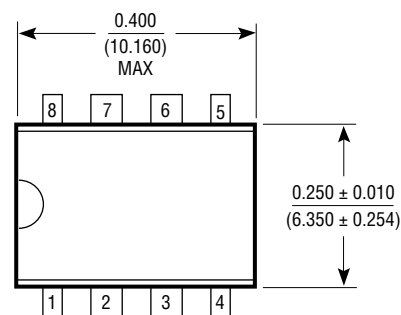
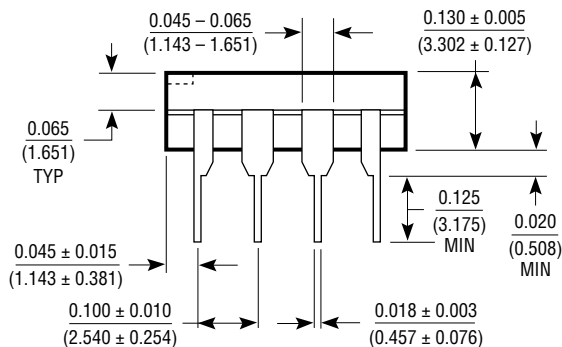
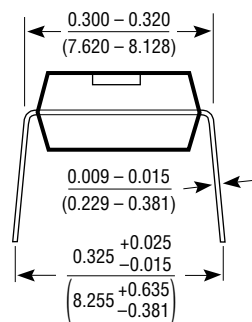
*CTX20-3 COILTRONICS

TYPICAL APPLICATIONS

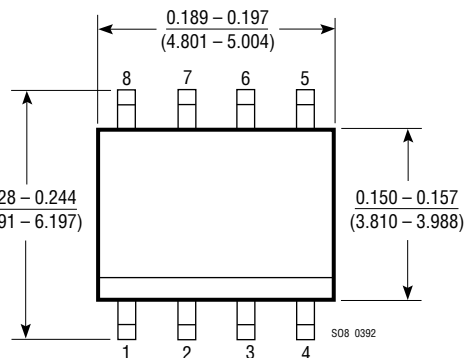
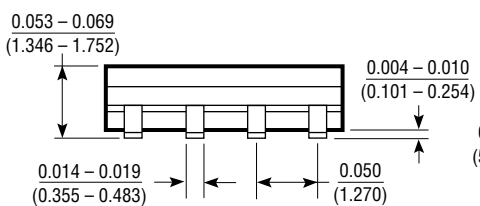
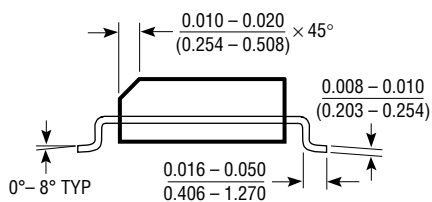
3.3V Ultra Low Voltage Drop Regulator with Optional Reverse Battery Protection and 3 μ A Standby Current

*OPTIONAL REVERSE BATTERY PROTECTION. ADD R1 IN SERIES WITH THE GROUND LEAD AND ADD Q1 IN SERIES WITH THE BATTERY AS SHOWN.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package
8-Lead Plastic DIP

NB 0392

S Package
8-Lead SOIC

S08 0392