COM20022I

10 Mbps ARCNET (ANSI 878.1) Controller with 2Kx8 On-Chip RAM

Datasheet

Product Features

- **New Features**
  - Data Rates up to 10 Mbps
  - Selectable 8/16 Bit Wide Bus With Data Swapper
  - Programmable DMA Channel
  - Programmable Reconfiguration Times
  - 48 Pin TQFP Package; Lead-Free RoHS Compliant Package also available
- Ideal for Industrial/Factory/Building Automation and Transportation Applications
- Deterministic, (ANSI 878.1), Token Passing ARCNET Protocol
- Minimal Microcontroller and Media Interface Logic Required
- Flexible Interface For Use With All Microcontrollers or Microprocessors
- Automatically Detects Type of Microcontroller Interface
- 2Kx8 On-Chip Dual Port RAM
- Command Chaining for Packet Queuing
- Sequential Access to Internal RAM
- Software Programmable Node ID
- Eight, 256 Byte Pages Allow Four Pages TX and RX Plus Scratch-Pad Memory
- Next ID Readable
- Internal Clock Scaler and Clock Multiplier for Adjusting Network Speed
- Operating Temperature Range of -40^{o}C to +85^{o}C
- Self-Reconfiguration Protocol
- Supports up to 255 Nodes
- Supports Various Network Topologies (Star, Tree, Bus...)
- CMOS, Single +5V Supply
- Duplicate Node ID Detection
- Powerful Diagnostics
- Receive All Packets Mode
- Flexible Media Interface:
  - Traditional Hybrid Interface For Long Distances up to Four Miles at 2.5Mbps
  - RS485 Differential Driver Interface For Low Cost, Low Power, High Reliability

ORDERING INFORMATION

Order Numbers:

COM20022ITQFP for 48 pin TQFP package

COM20022I-HT for 48 pin, TQFP Lead-Free RoHS Compliant package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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For more details on the ARCNET protocol engine and traditional dipulse signaling schemes, please refer to the ARCNET Local Area Network Standard, or the ARCNET Designer's Handbook, available from Datapoint Corporation.

Chapter 1 General Description

SMSC's COM20022I is a member of the family of Embedded ARCNET Controllers from Standard Microsystems Corporation. The device is a general purpose communications controller for networking microcontrollers and intelligent peripherals in industrial, automotive, and embedded control environments using an ARCNET protocol engine. The small 48 pin package, flexible microcontroller and media interfaces, eight- page message support, and extended temperature range of the COM20022I make it the only true network controller optimized for use in industrial, embedded, and automotive applications. Using an ARCNET protocol engine is the ideal solution for embedded control applications because it provides a deterministic token-passing protocol, a highly reliable and proven networking scheme, and a data rate of up to 10 Mbps when using the COM20022I. A token-passing protocol provides predictable response times because each network event occurs within a predetermined time interval, based upon the number of nodes on the network. The deterministic nature of ARCNET is essential in real time applications. The integration of the 2Kx8 RAM buffer on-chip, the Command Chaining feature, the 10 Mbps maximum data rate, and the internal diagnostics make the COM20022I the highest performance embedded communications device available. With only one COM20022I and one microcontroller, a complete communications node may be implemented.

Chapter 2 Pin Configuration

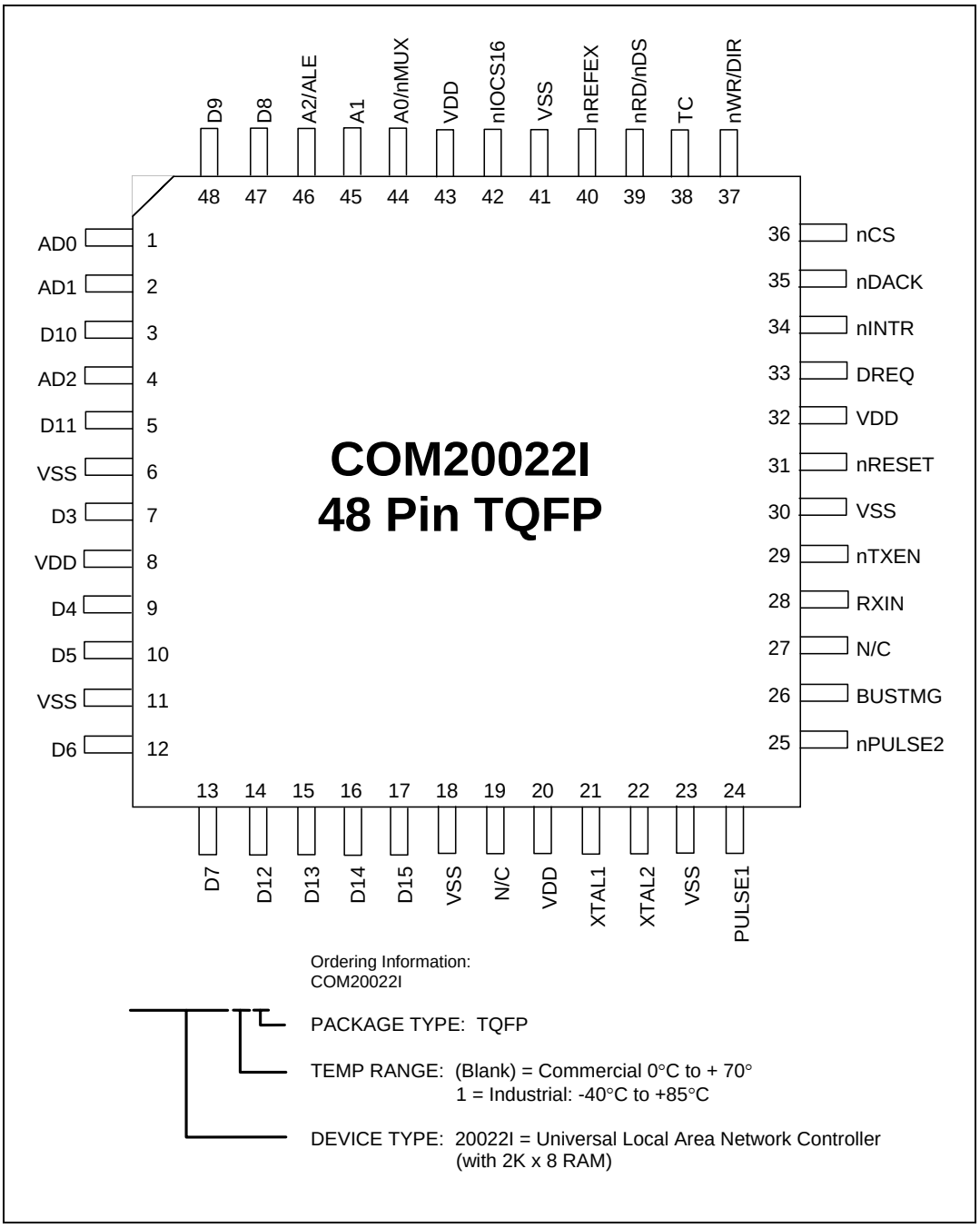


Figure 2.1 - COM20022I Pin Configuration

Chapter 3 Description of Pin Functions

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
MICROCONTROLLER INTERFACE				
44,45, 46	Address 0-2	A0/nMUX A1 A2/ALE	IN IN IN	On a non-multiplexed mode, A0-A2 are address input bits. (A0 is the LSB) On a multiplexed address/data bus, nMUX tied Low, A1 is left open, and ALE is tied to the Address Latch Enable signal. A1 is connected to an internal pull-up resistor.
1,2,4, 7,9, 10,12, 13	Data 0-7	AD0-AD2, D3-D7	I/O	On a non-multiplexed bus, these signals are used as the lower byte data bus lines. On a multiplexed address/data bus, AD0-AD2 act as the address lines (latched by ALE) and as the low data lines. D3-D7 are always used for data only. These signals are connected to internal pull-up resistors.
47, 48, 3,5, 14-17	Data 8-15	D8-D15	I/O	D8-D15 are always used as the higher byte data bus lines only for 16bit internal RAM access. When the 16bit access is disabled, these signals are always Hi-Z. Enabling or disabling the 16bit access is programmable. A data swapper is built in. These signals are connected to internal pull-up resistors.
37	nWrite/ Direction	nWR/DIR	IN	nWR is for 80xx CPU, nWR is Write signal input. Active Low. DIR is for 68xx CPU, DIR is Bus Direction signal input. (Low: Write, High: Read.)
39	nRead/ nData Strobe	nRD/nDS	IN	nRD is for 80xx CPU, nRD is Read signal input. Active Low. nDS is for 68xx CPU, nDS is Data Strobe signal input. Active Low.
31	nReset In	nRESET	IN	Hardware reset signal. Active Low.
34	nInterrupt	nINTR	OUT	Interrupt signal output. Active Low.
36	nChip Select	nCS	IN	Chip Select input. Active Low.
42	nI/O 16 Bit Indicator	nIOCS16	OUT	This signal is an active Low signal which indicates accessing 16bit data only by CPU. This signal becomes active when CPU accesses to data register only if W16 bit is 1. This signal is same as on ISA Bus signal, but it's not OPEN-DRAIN. An external OPEN-DRAIN Buffer is needed when this signal connects to the ISA Bus.
26	Read/Write Bus Timing Select	BUSTMG	IN	Read and Write Bus Access Timing mode selecting signal. Status of this signal effects CPU and DMA Timing. L: High speed timing mode (only for non-multiplexed bus) H: Normal timing mode This signal is connected to internal pull-up registers.
33	DMA Request	DREQ	OUT	DMA Request signal. Active polarity is programmable. Default is active high.
35	DMA Ack	nDACK	IN	DMA Acknowledge signal. Active Low. When BUSTMG is High, this signal is connected to internal pull-up registers
38	Terminal Count	TC	IN	Terminal Count signal. Active polarity is programmable. Default is active high. When BUSTMG is High, this signal is connected to the internal pull-up resistor.
40	Refresh Execution	nREFEX	IN	Refresh execution signal. Falling edge detection. This signal is connected to the internal pull-up resistor.

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
TRANSMISSION MEDIA INTERFACE				
24 25	nPulse 1 nPulse 2	nPULSE1 nPULSE2	OUT I/O	In Normal Mode, these active low signals carry the transmit data information, encoded in pulse format as DIPULSE waveform. In Backplane Mode, the nPULSE1 signal driver is programmable (push/pull or open-drain), while the nPULSE2 signal provides a clock with frequency of doubled data rate. nPULSE1 is connected to a weak internal pull-up resistor on the open/drain driver in backplane mode.
28	Receive In	RXIN	IN	This signal carries the receive data information from the line transceiver.
29	nTransmit Enable	nTXEN	OUT	Transmission Enable signal. Active polarity is programmable through the nPULSE2 pin. nPULSE2 floating before power-up; nTXEN active low nPULSE2 grounded before power-up; nTXEN active high (this option is only available in Back Plane mode)
21 22	Crystal Oscillator	XTAL1 XTAL2	IN OUT	An external crystal should be connected to these pins. Oscillation frequency range is from 10 MHz to 20 MHz. If an external TTL clock is used instead, it must be connected to XTAL1 with a 390ohm pull-up resistor, and XTAL2 should be left floating.
8,20, 32,43	Power Supply	VDD	PWR	+5 Volt power supply pins.
6,11, 18,23, 30,41	Ground	VSS	PWR	Ground pins.
19,27	N/C	N/C		Non-connection

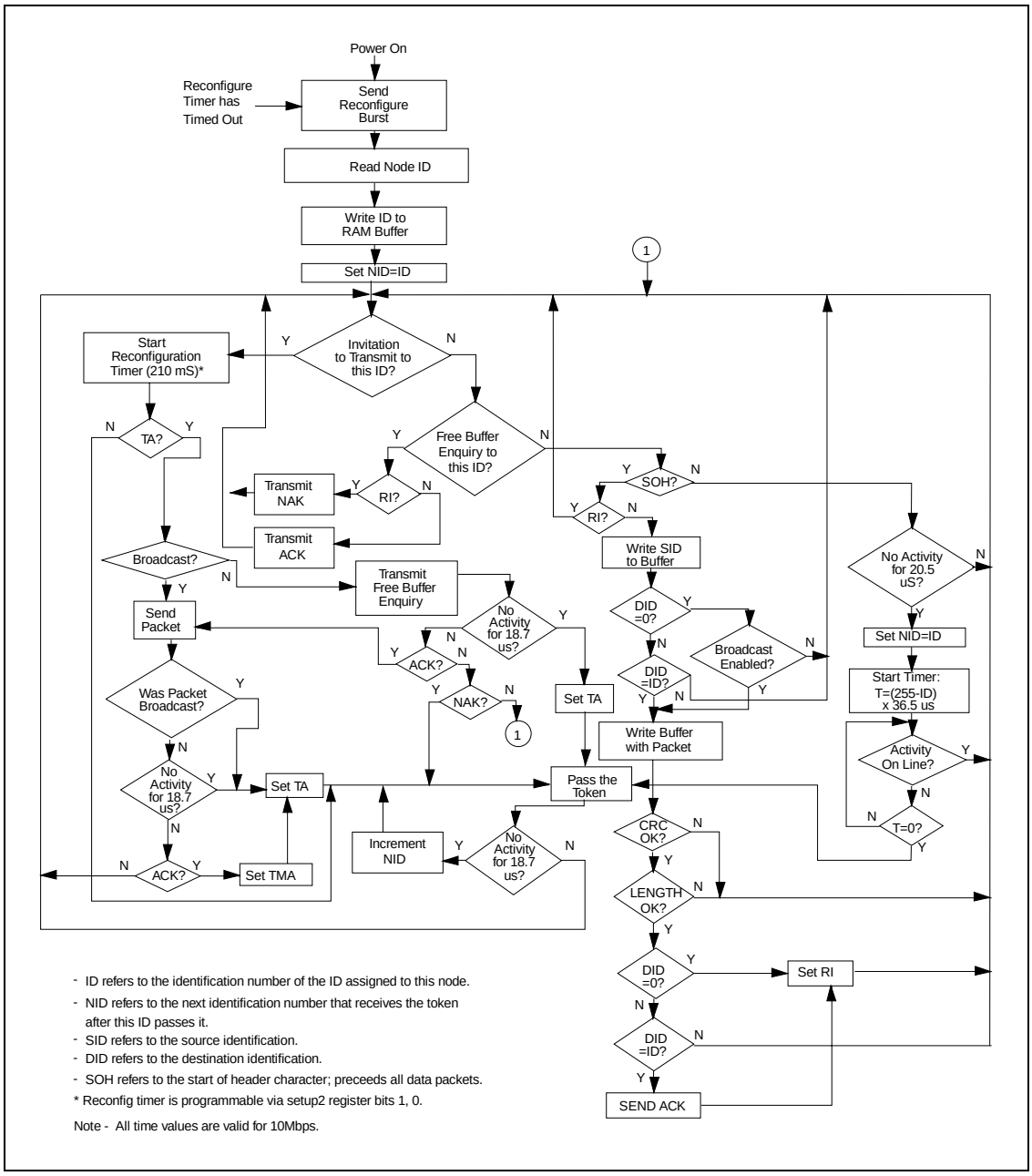


Figure 3.1 - COM20022I Operation

Chapter 4 Protocol Description

4.1 Network Protocol

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM20022I's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the COM20022I's internal RAM buffer, and issuing a command to enable the transmitter. When the COM20022I next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16-bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node verifies the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is not received successfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM20022I to generate an interrupt to the processor when selected status bits become true. Figure 2.1 is a flow chart illustrating the internal operation of the COM20022I connected to a 20 MHz crystal oscillator.

4.2 Data Rates

The COM20022I is capable of supporting data rates from 156.25 Kbps to 10 Mbps. The following protocol description assumes a 10 Mbps data rate. To attain the faster data rates, the clock frequency may be doubled or quadrupled by the internal clock multiplier (see next section). For slower data rates, an internal clock divider scales down the clock frequency. Thus all timeout values are scaled as shown in the following table:

Example:

IDLE LINE Timeout @ 10 Mbps = 20.5 μs. IDLE LINE Timeout for 156.2 Kbps is 20.5 μs * 64 = 1.3 ms

INTERNAL CLOCK FREQUENCY	CLOCK PRESCALER	DATA RATE	TIMEOUT SCALING FACTOR (MULTIPLY BY)
80 MHz	Div. by 8	10 Mbps	1
40 MHz	Div. by 8	5 Mbps	2
20 MHz	Div. by 8	2.5 Mbps	4
	Div. by 16	1.25 Mbps	8
	Div. by 32	625 Kbps	16
	Div. by 64	312.5 Kbps	32
	Div. by 128	156.25 Kbps	64

4.2.1 Selecting Clock Frequencies Above 2.5 Mbps

To realize a 10 Mbps network, an external 80 MHz clock must be input. However, since 80 MHz is the frequency of FM radio band, it is not practical for use for noise emission reasons. Therefore, higher frequency clocks are generated from the 20 MHz crystal as selected through two bits in the Setup2 register, CKUP[1,0] as shown below. The selected clock is supplied to the ARCNET controller.

CKUP1	CKUP0	CLOCK FREQUENCY (DATA RATE)
0	0	20 MHz (Up to 2.5Mbps) Default (Bypass)
0	1	40 MHz (Up to 5Mbps)
1	0	Reserved
1	1	80 MHz (Only 10Mbps)

This clock multiplier is powered-down (bypassed) on default. After changing the CKUP1 and CKUP0 bits, the ARCNET core operation is stopped and the internal PLL in the clock generator is awakened and it starts to generate the 40 MHz or 80 MHz. The lock out time of the internal PLL is 8uSec typically. After more than 8 μsec (this wait time is defined as 1 msec in this data sheet), it is necessary to write command data '18H' to the command register to re-start the ARCNET core operation. This clock generator is called “clock multiplier”.

Changing the CKUP1 and CKUP0 bits must be one time or less after releasing a hardware reset.

The EF bit in the SETUP2 register must be set when the data rate is over 5 Mbps.

4.3 Network Reconfiguration

A significant advantage of the COM20022I is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM20022I is turned on (creating a new active node on the network), or if the COM20022I has not received an INVITATION TO TRANSMIT for 210mS, or if a software reset occurs, the COM20022I causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM20022I senses an idle line for greater than 20.5μS, which occurs only when the token Is lost, each COM20022I starts an internal timeout equal to 36.5μs times the quantity 255 minus its own ID. The COM20022I starts network reconfiguration by sending an invitation to transmit first to itself and then to all other nodes by decrementing the destination Node ID. If the timeout expires with no line activity, the COM20022I starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM20022I will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM20022I waits for activity on the line. If there is no activity for 18.7μS, the COM20022I increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 18.7μS timeout expires, the COM20022I releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT are sent to all NIDs *(1-255).*

Each COM20022I on the network will finally have saved a NID value equal to the ID of the COM20022I that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node attempts to pass the token to it by issuing an INVITATION TO TRANSMIT. Since this node does not respond, the previous node times out and transmits another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The NETWORK RECONFIGURATION time depends on the number of nodes in the network, the propagation delay between nodes, and the highest ID number on the network, but is typically within the range of 6 to 15.3 mS.

4.4 Broadcast Messages

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 5.7 illustrates the position of each byte in the packet with the DID residing at address 0X01 or 1 Hex of the current page selected in the "Enable Transmit from Page fnn" command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the "Enable Receive to Page fnn" command (see Table 6.5) to a logic "0".

4.5 Extended Timeout Function

There are three timeouts associated with the COM20022I operation. The values of these timeouts are controlled by bits 3 and 4 of the Configuration Register and bit 5 of the Setup 1 Register.

4.5.1 Response Time

The Response Time determines the maximum propagation delay allowed between any two nodes, and should be chosen to be larger than the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM20022I to start sending a message in response to a received message) which is approximately 3.2 μS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 7.75 μS translates to a distance of about 1 mile. The flow chart in Figure 3.1Figure 2.1 uses a value of 18.7 μS (7.75 + 7.75 + 3.2) to determine if any node will respond.

4.5.2 Idle Time

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 3.1Figure 2.1 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. All other nodes on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 20.5 μS. This 20.5 μS is equal to the Response Time of 18.7 μS plus the time it takes the COM20022I to start retransmitting another message (usually another INVITATION TO TRANSMIT).

4.5.3 Reconfiguration Time

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION. The ET2 and ET1 bits of the Configuration Register allow the network to operate over longer distances than the 1 mile stated earlier. The logic levels on these bits control the maximum distances over which the COM20022I can operate by controlling the three timeout values described above. For proper network operation, all COM20022I's connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

4.6 Line Protocol

The ARCNET line protocol is considered isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. *On a 10 Mbps network,* each byte takes exactly 11 clock intervals of 100ns each. As a result, one byte is transmitted every 1.1 μS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a negative pulse of 50nS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent, with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

4.6.1 Invitations To Transmit

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission: ASCII code 04H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	EOT	DID	DID

4.6.2 Free Buffer Enquiries

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data. It is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENQuiry: ASCII code 85H)
- Two (repeated) DID (Destination ID) characters

ALERT BURST	ENQ	DID	DID

4.6.3 Data Packets

A Data Packet consists of the actual data being sent to another node. It is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01H)
- An SID (Source ID) character
- Two (repeated) DID (Destination ID) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is sent, or 00H followed by a COUNT character if a long packet is sent.
- N data bytes where COUNT = 256-N (or 512-N for a long packet)
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is: $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

4.6.4 Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86H) character

ALERT BURST	ACK

4.6.5 Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative Acknowledgement--ASCII code 15H) character

ALERT BURST	NAK

Chapter 5 System Description

5.1 Microcontroller Interface

The top halves of Figure 5.1 and Figure 5.2 illustrate typical COM20022I interfaces to the microcontrollers. The interfaces consist of a 8-bit data bus, an address bus and a control bus. In order to support a wide range of microcontrollers without requiring glue logic and without increasing the number of pins, the COM20022I automatically detects and adapts to the type of microcontroller being used. Upon hardware reset, the COM20022I first determines whether the read and write control signals are separate READ and WRITE signals (like the 80XX) or DIRECTION and DATA STROBE (like the 68XX). To determine the type of control signals, the device requires the software to execute at least one write access to external memory before attempting to access the COM20022I. The device defaults to 80XX-like signals. Once the type of control signals are determined, the COM20022I remains in this interface mode until the next hardware reset occurs. The second determination the COM20022I makes is whether the bus is multiplexed or non-multiplexed. To determine the type of bus, the device requires the software to write to an odd memory location followed by a read from an odd location before attempting to access the COM20022I. The signal on the A0 pin during the odd location access tells the COM20022I the type of bus. Since multiplexed operation requires A0 to be active low, activity on the A0 line tells the COM20022I that the bus is non-multiplexed. The device defaults to multiplexed operation. Both determinations may be made simultaneously by performing a WRITE followed by a READ operation to an odd location within the COM20022I Address space 20022 registers. Once the type of bus is determined, the COM20022I remains in this interface mode until hardware reset occurs.

Whenever nCS and nRD are activated, the preset determinations are assumed as final and will not be changed until hardware reset. Refer to Description of Pin Functions section for details on the related signals. All accesses to the internal RAM and the internal registers are controlled by the COM20022I. The internal RAM is accessed via a pointer-based scheme (refer to the Sequential Access Memory section), and the internal registers are accessed via direct addressing. Many peripherals are not fast enough to take advantage of high-speed microcontrollers. Since microcontrollers do not typically have READY inputs, standard peripherals cannot extend cycles to extend the access time. The access time of the COM20022I, on the other hand, is so fast that it does not need to limit the speed of the microcontroller. The COM20022I is designed to be flexible so that it is independent of the microcontroller speed.

The COM20022I provides for no wait state arbitration via direct addressing to its internal registers and a pointer based addressing scheme to access its internal RAM. The pointer may be used in auto-increment mode for typical sequential buffer emptying or loading, or it can be taken out of auto-increment mode to perform random accesses to the RAM. The data within the RAM is accessed through the data register. Data being read is prefetched from memory and placed into the data register for the microcontroller to read. It is important to notice that only by writing a new address pointer (writing to an address pointer low), one obtains the contents of COM20022I internal RAM. Performing only read from the Data Register does not load new data from the internal RAM. During a write operation, the data is stored in the data register and then written into memory. Whenever the pointer is loaded for reads with a new value, data is immediately prefetched to prepare for the first read operation.

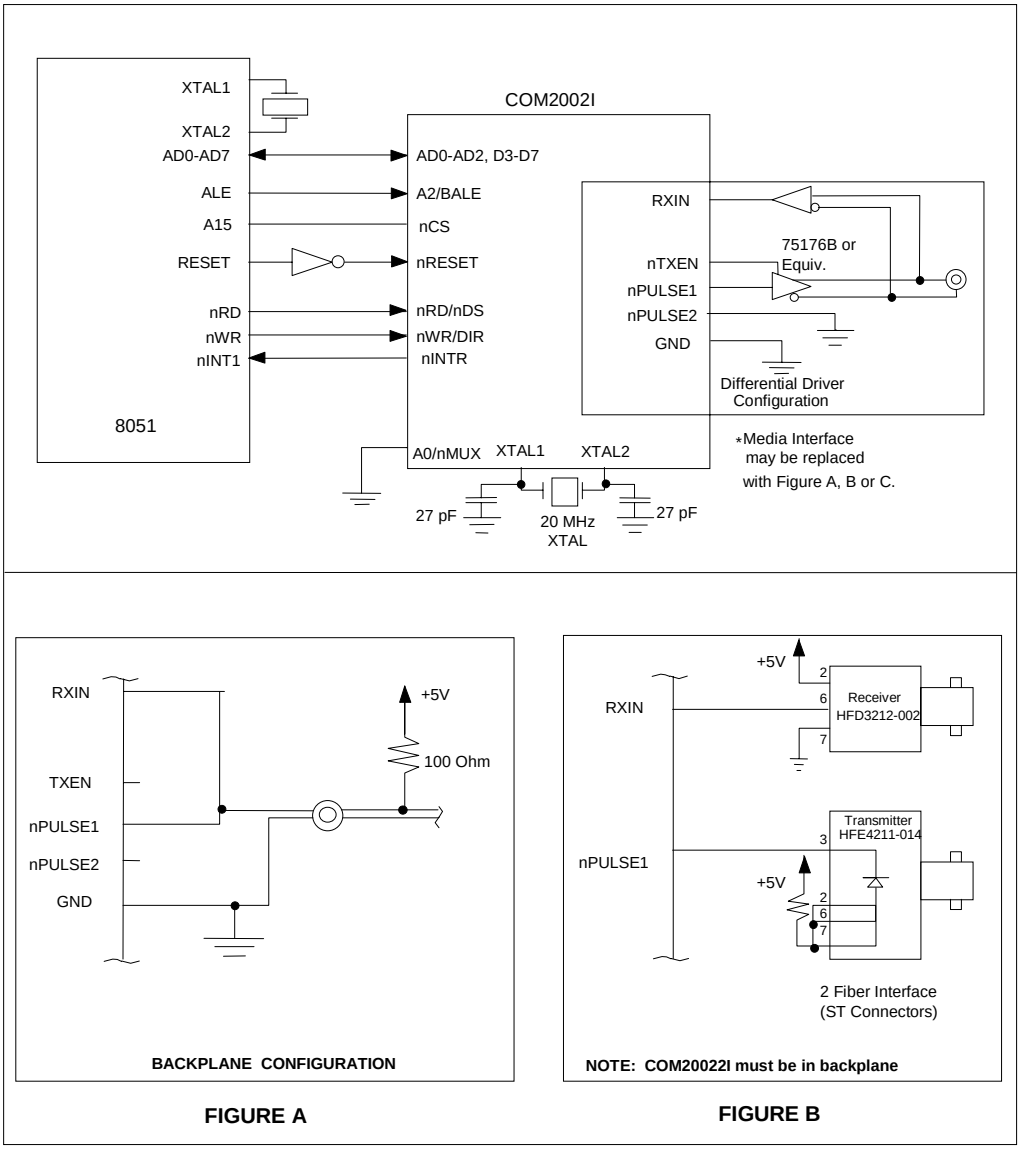


Figure 5.1 - Multiplexed, 8051-Like Bus Interface with RS-485 Interface

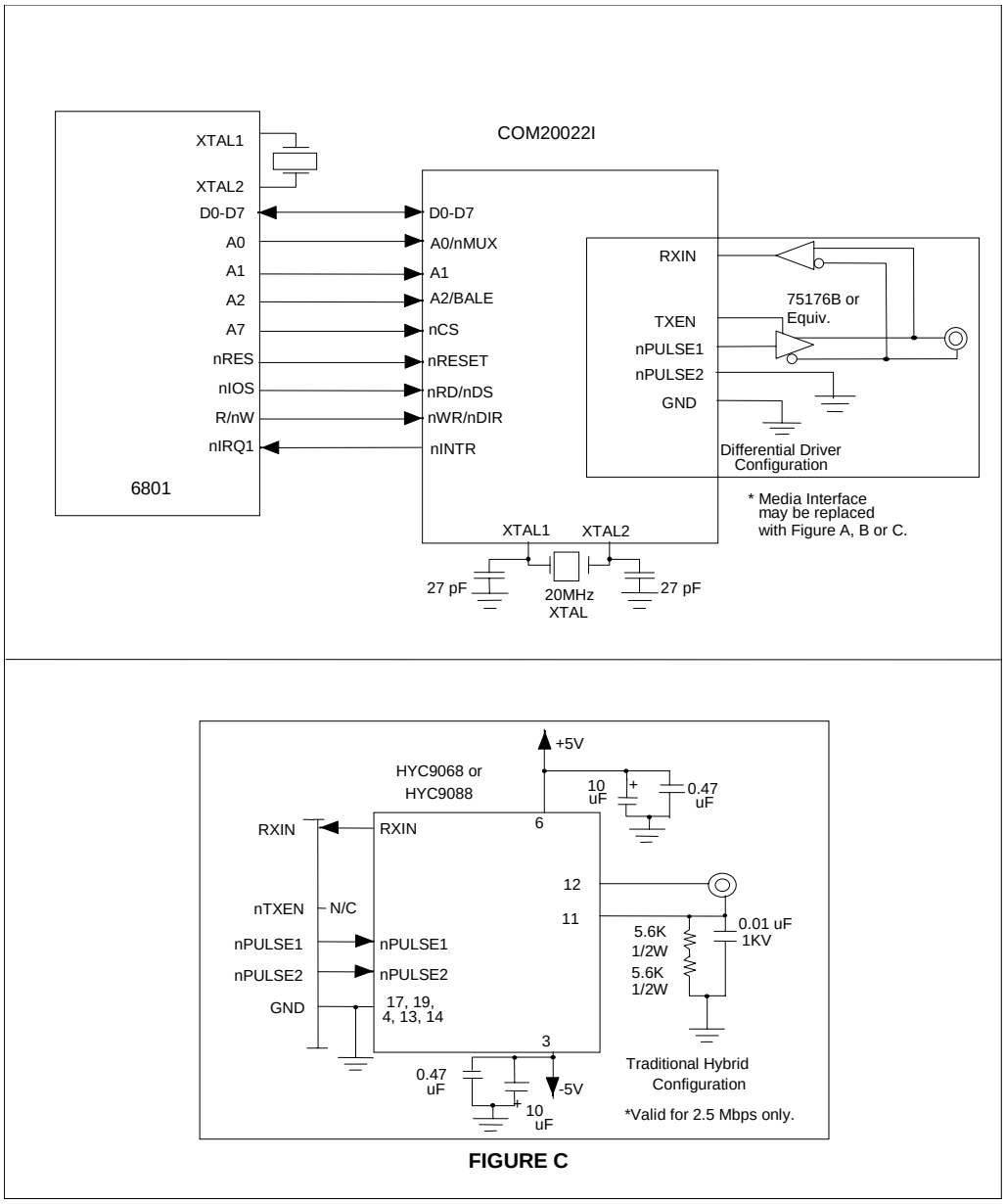


FIGURE C

Figure 5.2 - Non-Multiplexed, 6801-Like Bus Interface with RS-485 Interface

5.1.1 Selection of 8/16-Bit Access

The interface to the internal RAM is software selectable as either 8 or 16-bit. This feature is new to the COM20022I. The D15-D8 pins are the upper-byte data bus pins. The nIOCS16 pin is the 16-bit I/O access enable output pin. This pin is active low for a 16-bit RAM access by the CPU (not a DMA access).

The 16-bit access mode is enabled and disabled through the W16 bit located in the Bus Control Register at bit 7. The SWAP bit is used to swap the upper and lower data bytes in 16-bit mode, as shown in the table below. The SWAP bit is located at bit 0 of Address Low Pointer. This location is same as the A0 bit; when 16 bit access is enabled (W16 =1), the A0 bit becomes the SWAP bit.

DETECTED HOST I/F MODE	SWAP BIT (NOTE)	D15-D8 PINS	D7-D0 PINS
Intel 80xx Mode	0	Odd	Even
(RD,WR Mode)	1	Even	Odd
Motorola 68xx Mode	0	Even	Odd
(DIR, DS Mode)	1	Odd	Even

Note: The SWAP bit is undefined after a hardware reset

As shown on the table above, even address data is to/from D7-D0 pins and odd address data is to/from D15-D8 pins when detected host interface mode is Intel 80xx mode and the SWAP bit is not set. The odd address data is to/from the D7-D0 pins and the even address data is to/from D15-D8 pins when detected host interface mode is Motorola 68xx mode and the SWAP bit is not set.

When disabling 16-bit access, the D15-D8 pins are always Hi-Z. The D15-D8 pins are Hi-Z when enabling 16-bit access except for internal RAM access.

W16 bit and SWAP bit influence both the CPU cycle and DMA cycle.

5.1.2 DMA Transfers To And From Internal RAM

The COM20022I supports DMA transfers to and from the internal RAM. This feature is new to the COM20022I. The software selectable 8/16 bit interface to the RAM pertains to DMA transfers. When the W16 bit=0, the microcontroller interface and DMA transfers are both 8-bit data transfers to/from internal RAM. When W16=1 they are both 16-bit data transfers. An 8-bit microcontroller interface and 16-bit DMA data transfer cannot be selected; they must be the same width data transfers to/from internal RAM.

The data swapping operation on 16-bit data transfers also pertains to both.

The DMA interface consists of several added pins. The DREQ pin is the DMA Request output pin. The active polarity of this pin is programmable; the default is active-high. The nDACK pin is the active-low DMA acknowledge input pin. The TC pin is the external terminal count input pin. This pin determines when the nDACK pin is active. It's active polarity is programmable; the default is active-high. The nREFEX pin is the active-low refresh execution pulse input pin.

The DMA interface is controlled by the following bits. The DMAEND bit selects whether or not to mask the interrupt upon finishing the DMA. This bit is located at bit 4 of the Mask register. The DMAEN bit is used to disable/enable the assertion of the DMA Request (DREQ pin) after writing the Address Pointer Low register. This bit is located in the Address Pointer High register, bit 3. The following bits are located in the Bus Control Register: DRPOL, TCPOL and DMAMD[1,0]. The DRQPOL bit sets the active polarity of the DREQ pin; the TCPOL bit sets the active polarity of the TC pin; the DMAMD[1,0] bits select the data transfer mode of the DMA.

The ITCEN/RTRG bit has one of two functions, depending on the DMA transfer mode selected. ITCEN is the Internal Terminal Counter Enable. It is used to select whether the DMA is terminated by external TC

only or by either internal or external TC. ITCEN is for Non-Burst or Burst mode. RTRG selects the re-trigger mode as either external or internal. It is for the two Programmable-Burst modes.

The TC8/RSYN/GTTM bit has one of three functions, depending on the DMA transfer mode selected. TC8 is bit 8 of the Terminal Count. It is the MSB of the 9 bit Terminal Count setting register (the other 8 bits are in the DMA Count register). TC8 is for Non-Burst or Burst mode. RSYN is the Refresh Synchronous bit. This bit is used to select whether the DMA is started immediately or after Refresh execution. GTTM is the Gate Time bit. This bit selects whether the Gate Time is 350nS (min) or 750nS (min). RSYN and GTTM are for the two Programmable-Burst modes. RSYN is for External Re-Trigger mode; GTTM is for internal Re-Trigger mode.

Located in the DMA Count Register, the TC7-TC0 /TIM7-TIM0 /CYC7-CYC0 bits have one of three functions depending on the DMA transfer mode. TC7-TC0 are for non-burst or burst mode. These are the lower 8 bits of the Terminal Count setting register (the MSB is in the Bus Control Register). The TIM7-TIM0 bits are for setting the time of the continuous DMA transfer in Programmable-Burst by Timer mode. The CYC7-CYC0 bits are for setting the time of the continuous DMA transfer in Programmable-Burst by Cycle mode.

5.1.3 DMA Operation

The DMA interface operates in one of four transfer modes: Non-Burst, Burst, Programmable-Burst (by timer) and Programmable-Burst (by cycle counter). The data transfer mode of the DMA is selected through the DMAMD[1,0] bits in the Bus Control register, bits [3,2]. These modes are described below.

Non-Burst mode is a Single Transfer mode wherein, the DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1. Actually, DREQ pin is asserted 4T$_{ARB}$ time after writing the Address Pointer Low Register when DMAEN = 1 (refer to Figure 5.3). This mode operates as follows:

1. The nDACK pin is asserted by the DMA Controller detecting the DREQ pin asserted.
2. The DREQ pin is deasserted by the COM20022I detecting the nDACK pin asserted.
3. The nDACK pin is deasserted by the DMA Controller detecting the DREQ pin deasserted after executing the present read or write cycle.
4. The DREQ pin is asserted by the COM20022I detecting the DACK pin deasserted.

Repeat above 4 steps until the TC pin goes active. This mode is called "Cycle steal mode".

Burst mode is a Demand Transfer mode. In this mode, the DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1. Actually, DREQ pin is asserted 4T$_{ARB}$ time after writing the Address Pointer Low Register when DMAEN = 1 (refer to Figure 5.3). The DACK pin is asserted by the DMA Controller detecting the DREQ pin asserted. The DREQ pin stays asserted until the TC pin goes High.

Programmable-Burst mode is a Demand Transfer mode with temporary DREQ deassertion for a Refresh cycle. The DREQ pin is asserted after writing the Address Pointer Low Register when DMAEN=1 (refer to Figure 5.3). The DACK pin is asserted by the DMA Controller detecting the DREQ pin asserted. If the continuous DMA operation time is longer than the set Refresh period, then DREQ is deasserted. The DREQ is held deasserted after negating nDACK for the Gate time. After the Gate time, the DREQ pin is asserted again. The DREQ pin stays asserted until the TC pin goes High. In Programmable-Burst mode, the gating can be by timer or by cycle counter.

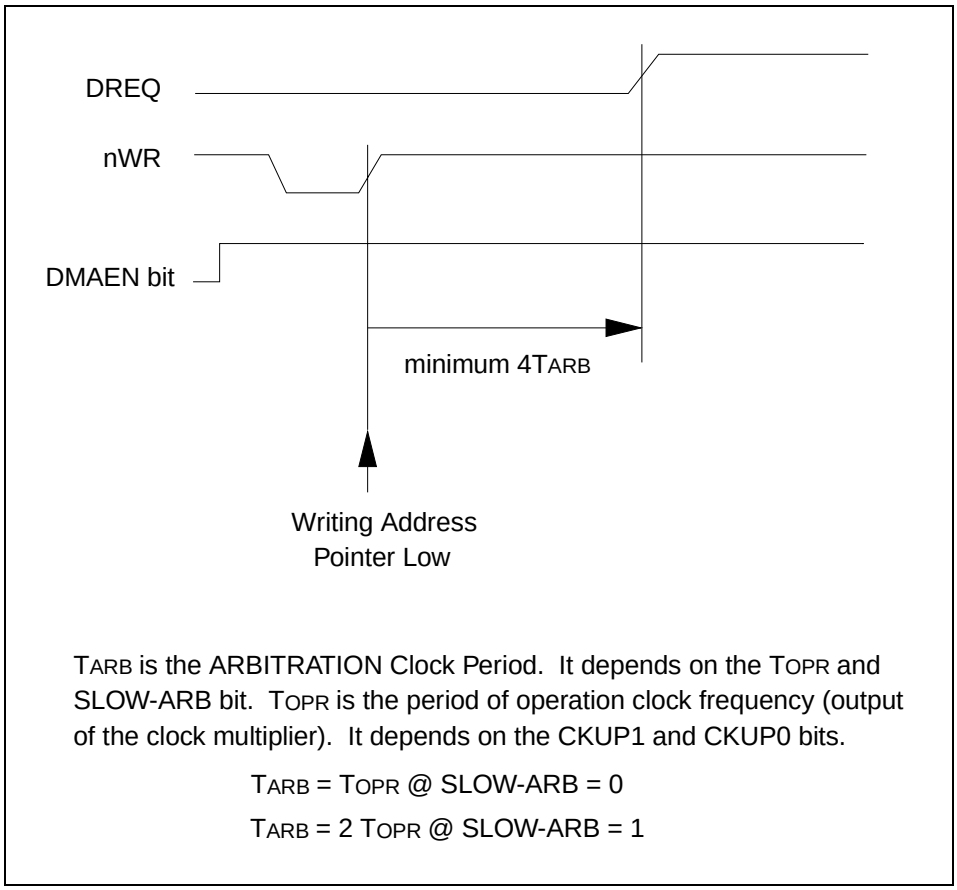


Figure 5.3 - DREQ Pin First Assertion Timing for All DMA Modes

As an example of gating by cycle, in an ISA bus system, the Refresh period is 15µS. Continuous transfer by DMA must be less than 15µS to prevent blocking by the Refresh cycle. A DMA cycle of consecutive DMA cycles is approximately 1uS. The DMA overhead time is approximately 2.5µS. The Refresh execution time is 500nS. This computes to 15µS - 2.5µS - 500nS = 12µS or 12 cycles. Therefore the DREQ pin must be negated every 12 cycles. Figure 5.4 illustrates the rough timing of the Programmable-Burst mode DMA transfer.

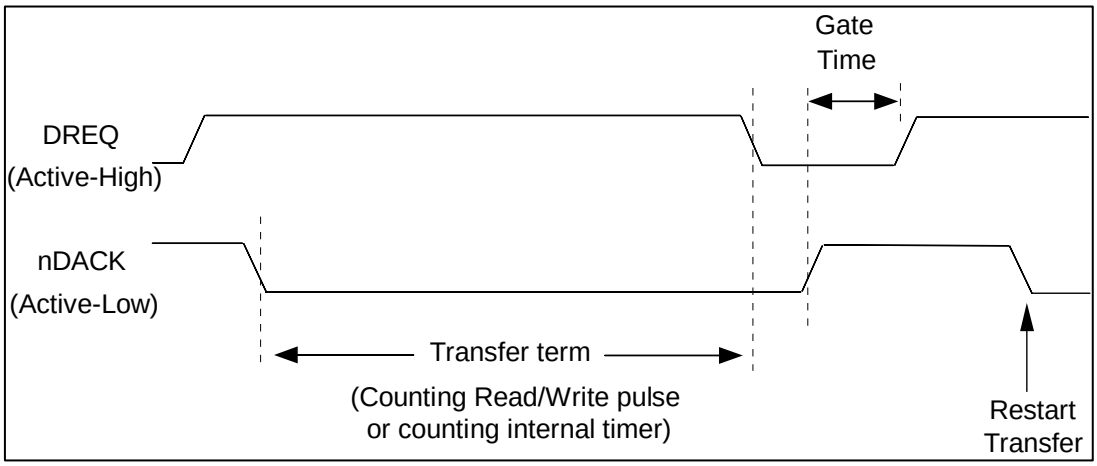


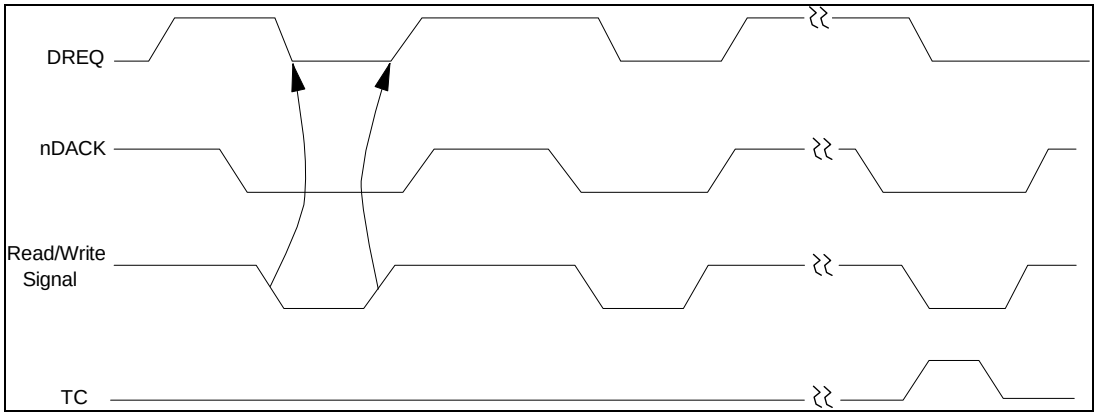
Figure 5.4 - Programmable Burst Mode DMA Transfer (Rough Timing)

The timing of the Non-Burst mode DMA data transfer is found in the Timing Diagrams section of this data sheet. The basic sequence of operation is as follows:

- nDACK becomes active (low) upon DREQ becoming active (high) and catching the host bus (AEN=1).
- DREQ becomes inactive after nDACK and read/write signal become active.
- DREQ becomes active after nDACK or read/write signal becomes inactive.
- DREQ becomes inactive after TC and the read/write signal assert (when nDACK=0). In this case, DREQ doesn't become active again after nDACK becomes inactive.
- nDACK becomes inactive after DREQ=0 and the present cycle finishes.

The following rough timing diagram of the non-burst mode DMA data transfer is included for illustration purposes.

Figure 5.5 - Non-Burst Mode DMA Data Transfer Rough Timing



The timing of the Burst mode DMA data transfer is found in the Timing Diagrams section of this data sheet. The basic sequence of operation is as follows:

- nDACK becomes active (low) upon DREQ becoming active (high) and catching the host bus (AEN= “1”).
- DREQ becomes inactive after TC asserts (when nDACK= “0”). In this case, DREQ doesn't become active again after nDACK becomes inactive.
- nDACK becomes inactive after DREQ= 0 and the present cycle finishes.

The following rough timing diagram of the non-burst mode DMA data transfer is included for illustration purposes.

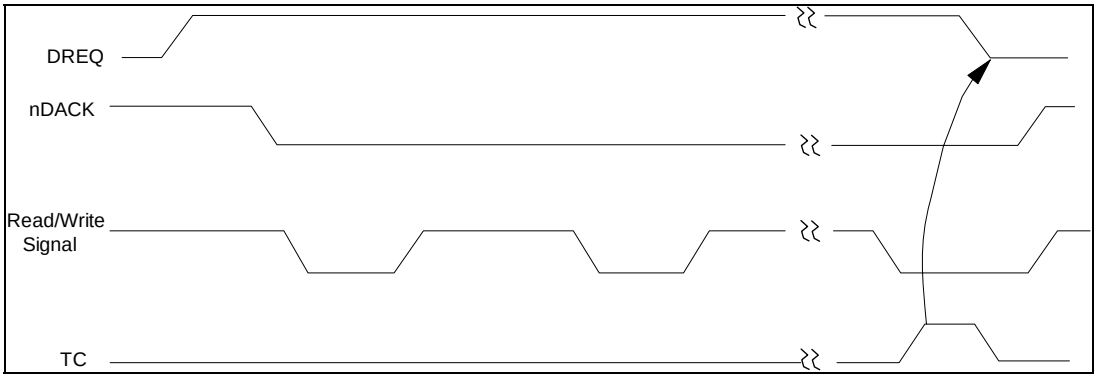


Figure 5.6 - Burst Mode DMA Data Transfer Rough Timing

The following sequences show the data transfer for a DMA read and a DMA write. The transfer of data between system memory and internal RAM functions as a memory to I/O DMA transfer. Since it is treated as an I/O device, the COM20022I has to create the RAM address. Therefore the COM20022I's address pointers must be programmed before starting the DMA transfers.

5.1.4 DMA Data Transfer Sequence (I/O to Memory: Read A Packet)

step1: Set DMA-controller (ex. 8237)
step2: Set DRQPOL, TCPOL, DMAMD1 and DMAMD0 bits
>>Finished DMA SETUP
>>A packet received
step3: Set address, byte count and etc. of DMA controller
step4: Set pointer High and Low (RDDATA=1,AUTOINC=1, DMAEN=0)
step5: Read SID, DID, CP in the received packet
step6: Set DMAEN=1 (RDDATA=1, AUTOINC=1)
step7: DMAEND=1 in Mask REG.
step8: Set pointer = CP
>>DREQ is asserted by step8
>>Interrupt occurs upon finishing DMA

5.1.5 DMA Data Transfer Sequence (Memory to I/O: Write A Packet)

step1: Set DMA-controller (ex. 8237)
step2: Set DRQPOL, TCPOL, DMAMD1 and DMAMD0 bits
>>Finished DMA SETUP
step3: Set address, byte count and etc. of DMA controller
step4: Set pointer High and Low (RDDATA=0,AUTOINC=1, DMAEN = 0)
step5: Write SID,DID,CP in the sending packet
step6: Set DMAEN=1 (RDDATA=0, AUTOINC=1)
step7: DMAEND=1 in Mask REG.
step8: Set pointer = CP
>>DREQ is asserted by step8
>>Interrupt occurs upon finishing DMA transfer
step9: Write Enable Transmit command to command register

5.1.6 High Speed CPU Bus Timing Support

High speed CPU bus support was added to the COM20022I. The reasoning behind this is as follows: With the Host interface in Non-multiplexed Bus mode, I/O address and Chip Select signals must be stable before the read signal is active and remain after the read signal is inactive. But the High Speed CPU bus timing doesn't adhere to these timings. For example, a RISC type single chip microcontroller (like the HITACHI SH-1 series) changes I/O address at the same time as the read signal. Therefore, several external logic ICs would be required to connect to this microcontroller.

In addition, the Diagnostic Status (DIAG) register is cleared automatically by reading itself. The internal DIAG register read signal is generated by decoding the Address (A2-A0), Chip Select (nCS) and Read (nRD) signals. The decoder will generate a noise spike at the above tight timing. The DIAG register is cleared by the spike signal without reading itself. This is unexpected operation. Reading the internal RAM and Next Id Register have the same mechanism as reading the DIAG register.

Therefore, the address decode and host interface mode blocks were modified to fit the above CPU interface to support high speed CPU bus timing. In Intel CPU mode (nRD, nWR mode), 3 bit I/O address (A2-A0) and Chip Select (nCS) are sampled internally by Flip-Flops on the falling edge of the internal delayed nRD signal. The internal real read signal is the more delayed nRD signal. But the rising edge of nRD doesn't delay. By this modification, the internal real address and Chip Select are stable while the internal real read signal is active. Refer to Figure 5.7 on the following page.

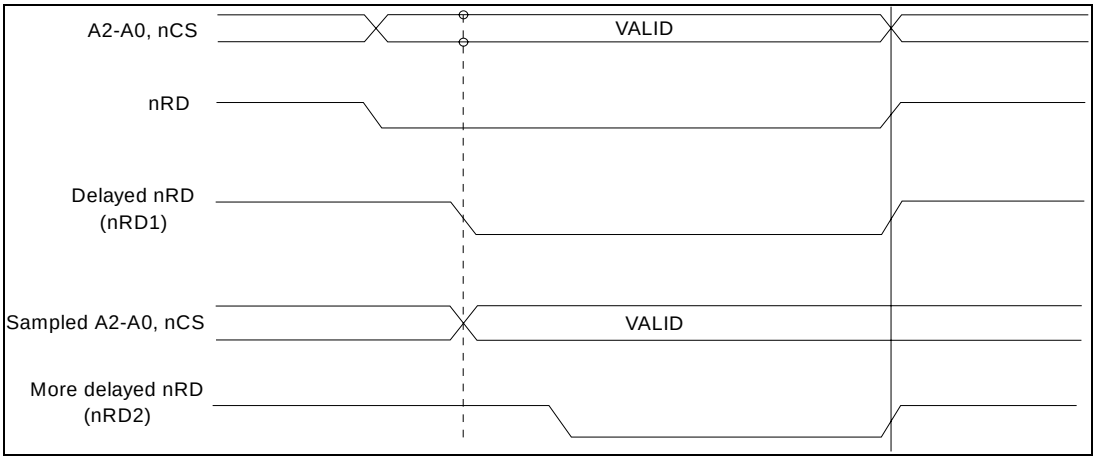


Figure 5.7 - High Speed CPU Bus Timing - Intel CPU Mode

The I/O address and Chip Select signals, which are supplied to the data output logic, are not sampled. Also, the nRD signal is not delayed, because the above sampling and delaying paths decrease the data access time of the read cycle.

The above sampling and delaying signals are supplied to the Read Pulse Generation logic which generates the clearing pulse for the Diagnostic register and generates the starting pulse of the RAM Arbitration. Typical delay time between nRD and nRD1 is around 15nS and between nRD1 and nRD2 is around 10nS.

Longer pulse widths are needed due to these delays on nRD signal. However, the CPU can insert some wait cycles to extend the width without any impact on performance.

The BUSTMG pin is used to support this function. It is used to Enable/Disable the High Speed CPU Read and Write function. It is defined as: BUSTMG = 0, the High Speed CPU Read and Write operations are enabled; BUSTMG = 1, the High Speed CPU Read and Write operations are disabled if the RBUSTMG bit is 0. If BUSTMG = 1 and RBUSTMG = 1, High Speed CPU Read operations are enabled (see definition of RBUSTMG bit below).

The RBUSTMG bit was added to Disable/Enable the High Speed CPU Read function. It is defined as: RBUSTMG=0, Disabled (Default); RBUSTMG=1, Enabled.

In the MOTOROLA CPU mode (DIR, nDS mode), the same modifications apply.

BUSTMG PIN	RBUSTMG BIT	BUS TIMING MODE
0	X	High Speed CPU Read and Write
1	0	Normal Speed CPU Read and Write
1	1	High Speed CPU Read and Normal Speed CPU Write

5.2 Transmission Media Interface

The bottom halves of Figure 5.1 and Figure 5.2 illustrate the COM20022I interface to the transmission media used to connect the node to the network. Table 5.1 lists different types of cable which are suitable for ARCNET applications. The user may interface to the cable of choice in one of three ways:

5.2.1 Traditional Hybrid Interface

The Traditional Hybrid Interface is that which is used with previous ARCNET devices. The Hybrid Interface is recommended if the node is to be placed in a network with other Hybrid-Interfaced nodes. The Traditional Hybrid Interface is for use with nodes operating at 2.5 Mbps only. The transformer coupling of the Hybrid offers isolation for the safety of the system and offers high Common Mode Rejection. The Traditional Hybrid Interface uses circuits like SMSC's HYC9068 or HYC9088 to transfer the pulse-encoded data between the cable and the COM20022I. The COM20022I transmits a logic "1" by generating two 100nS non-overlapping negative pulses, nPULSE1 and nPULSE2. Lack of pulses indicates a logic "0". The nPULSE1 and nPULSE2 signals are sent to the Hybrid, which creates a 200nS dipulse signal on the media. A logic "0" is transmitted by the absence of the dipulse. During reception, the 200nS dipulse appearing on the media is coupled through the RF transformer of the LAN Driver, which produces a positive pulse at the RXIN pin of the COM20022I. The pulse on the RXIN pin represents a logic "1". Lack of pulse represents a logic "0". Typically, RXIN pulses occur at multiples of 400nS. The COM20022I can tolerate distortion of plus or minus 100nS and still correctly capture and convert the RXIN pulses to NRZ format. Figure 5.4 illustrates the events which occur in transmission or reception of data consisting of 1, 1, 0.

5.2.2 Backplane Configuration

The Backplane Open Drain Configuration is recommended for cost-sensitive, short-distance applications like backplanes and instrumentation. This mode is advantageous because it saves components, cost, and power.

Since the Backplane Configuration encodes data differently than the traditional Hybrid Configuration, nodes utilizing the Backplane Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. The Backplane Configuration does not isolate the node from the media nor protects it from Common Mode noise, but Common Mode Noise is less of a problem in short distances.

The COM20022I supplies a programmable output driver for Backplane Mode operation. A push/pull or open drain driver can be selected by programming the P1MODE bit of the Setup 1 Register (see register descriptions for details). The COM20022I defaults to an open drain output.

The Backplane Configuration provides for direct connection between the COM20022I and the media. Only one pull-up resistor (in open drain configuration of the output driver) is required somewhere on the media (not on each individual node). The nPULSE1 signal, in this mode, is an open drain or push/pull driver and is used to directly drive the media. It issues a 200nS negative pulse to transmit a logic "1". Note that when used in the open-drain mode, the COM20022I does not have a fail/safe input on the RXIN pin. The nPULSE1 signal actually contains a weak pull-up resistor. This pull-up should not take the place of the resistor required on the media for open drain mode.

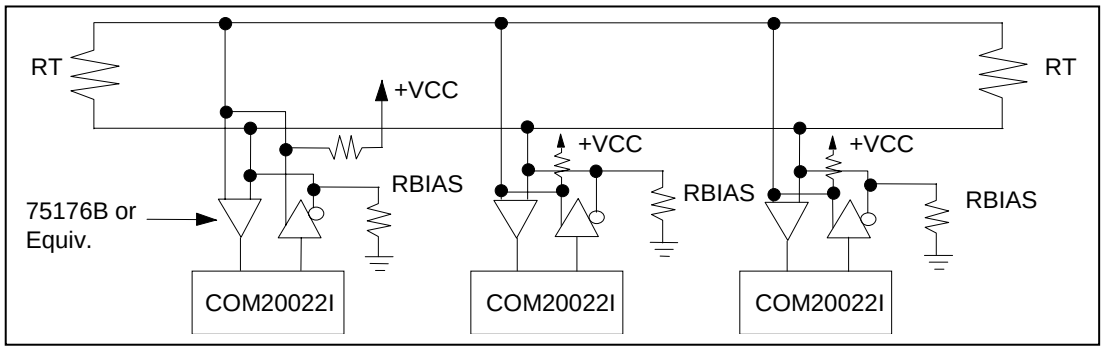


Figure 5.8 - COM20022I Network Using RS-485 Differential Transceivers

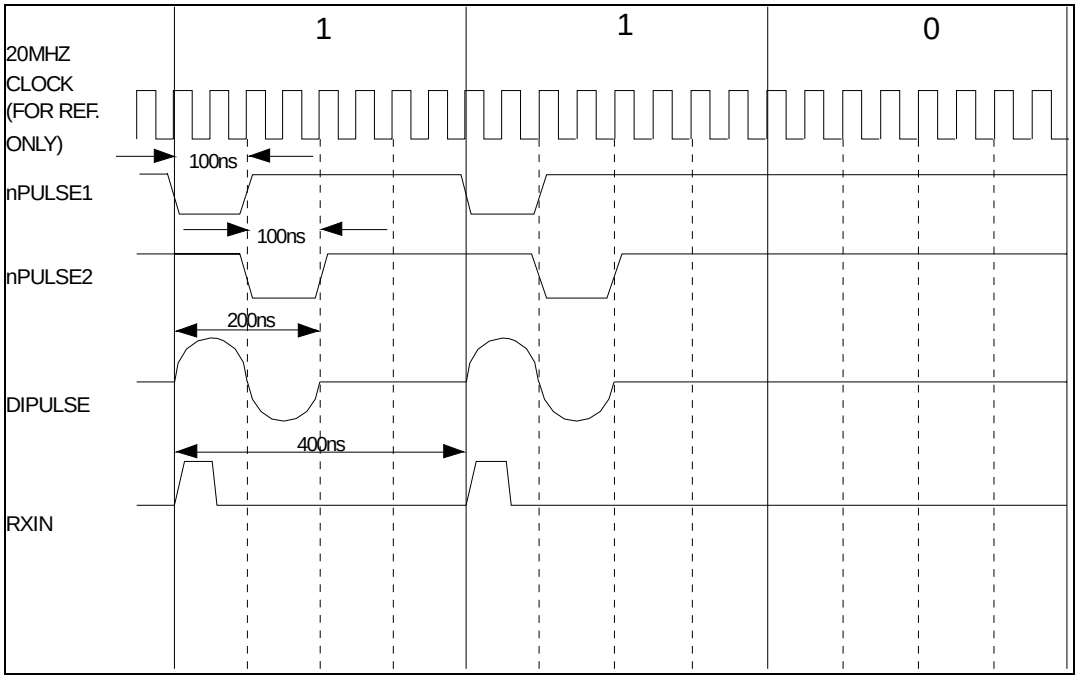


Figure 5.9 - Dipulse Waveform for Data of 1-1-0

In typical applications, the serial backplane is terminated at both ends and a bias is provided by the external pull-up resistor.

The RXIN signal is directly connected to the cable via an internal Schmitt trigger. A negative pulse on this input indicates a logic "1". Lack of pulse indicates a logic "0". For typical single-ended backplane applications, RXIN is connected to nPULSE1 to make the serial backplane data line. A ground line (from the coax or twisted pair) should run in parallel with the signal. For applications requiring different treatment of the receive signal (like filtering or squelching), nPULSE1 and RXIN remain as independent pins. External differential drivers/receivers for increased range and common mode noise rejection, for example, would require the signals to be independent of one another. When the device is in Backplane Mode, the clock provided by the nPULSE2 signal may be used for encoding the data into a different encoding scheme or other synchronous operations needed on the serial data stream.

5.2.3 Differential Driver Configuration

The Differential Driver Configuration is a special case of the Backplane Mode. It is a dc coupled configuration recommended for applications like car-area networks or other cost-sensitive applications which do not require direct compatibility with existing ARCNET nodes and do not require isolation. The Differential Driver Configuration cannot communicate directly with nodes utilizing the Traditional Hybrid Configuration. Like the Backplane Configuration, the Differential Driver Configuration does not isolate the node from the media.

The Differential Driver interface includes a RS485 Driver/Receiver to transfer the data between the cable and the COM20022I. The nPULSE1 signal transmits the data, provided the Transmit Enable signal is active. The nPULSE1 signal issues a 200nS (at 2.5Mbps) negative pulse to transmit a logic "1". Lack of pulse indicates a logic "0". The RXIN signal receives the data, the transmitter portion of the COM20022I is disabled during reset and the nPULSE1, nPULSE2 and nTXEN pins are inactive.

5.2.4 Programmable TXEN Polarity

To accommodate transceivers with active high ENABLE pins, the COM20022I contains a programmable TXEN output. To program the TXEN pin for an active high pulse, the nPULSE2 pin should be connected to ground. To retain the normal active low polarity, nPULSE2 should be left open. The polarity determination is made at power on reset and is valid only for Backplane Mode operation. The nPULSE2 pin should remain grounded at all times if an active high polarity is desired.

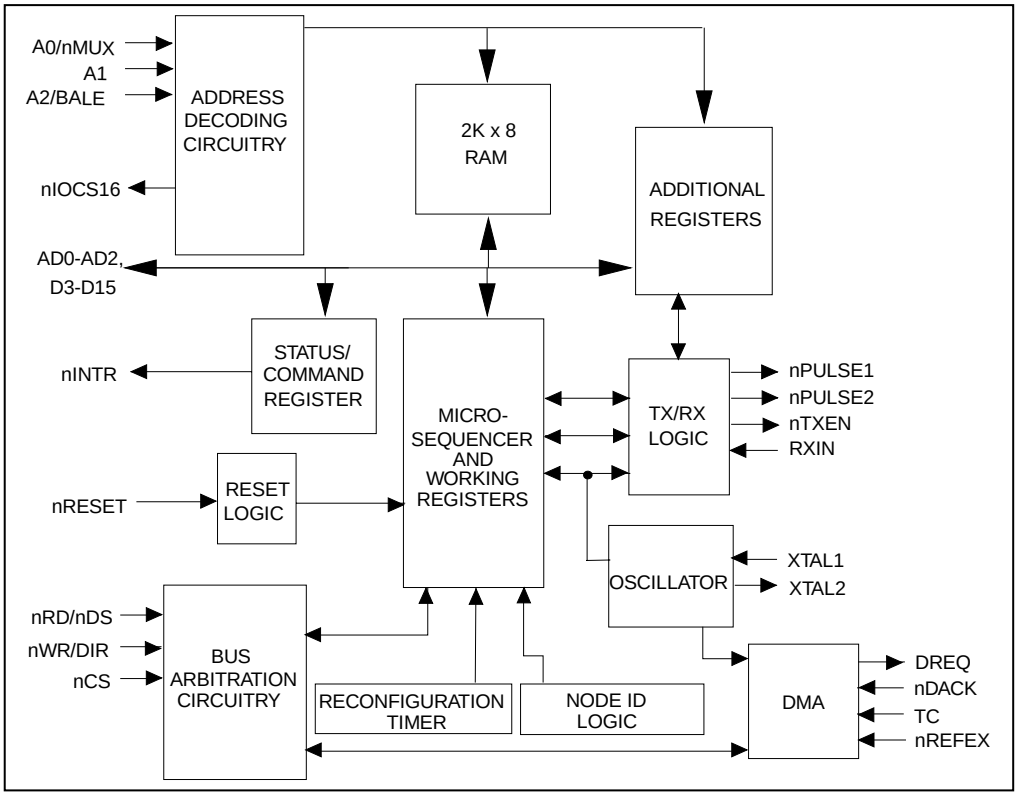


Figure 5.10 - Internal Block Diagram

Table 5.1 - Typical Media

CABLE TYPE	NOMINAL IMPEDANCE	ATTENUATION PER 1000 FT. AT 5 MHZ
RG-62 Belden #86262	93Ω	5.5dB
RG-59/U Belden #89108	75Ω	7.0dB
RG-11/U Belden #89108	75Ω	5.5dB
IBM Type 1* Belden #89688	150Ω	7.0dB
IBM Type 3* Telephone Twisted Pair Belden #1155A	100Ω	17.9dB
COMCODE 26 AWG Twisted Pair Part #105-064-703	105Ω	16.0dB

Note*: Non-plenum-rated cables of this type are also available.

Chapter 6 Functional Description

6.1 Microsequencer

The COM20022I contains an internal microsequencer which performs all of the control operations necessary to carry out the ARCNET protocol. It consists of a clock generator, a 544 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a no-op generator, jump logic, and reconfiguration logic.

The COM20022I derives a 20 MHz and a 10 MHz clock from the output clock of the Clock Multiplier. These clocks provide the rate at which the instructions are executed within the COM20022I. The 20 MHz clock is the rate at which the program counter operates, while the 10 MHz clock is the rate at which the instructions are executed. The microprogram is stored in the ROM and the instructions are fetched and then placed into the instruction registers. One register holds the opcode, while the other holds the immediate data. Once the instruction is fetched, it is decoded by the internal instruction decoder, at which point the COM20022I proceeds to execute the instruction. When a no-op instruction is encountered, the microsequencer enters a timed loop and the program counter is temporarily stopped until the loop is complete. When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM20022I contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out. At this point the program counter is cleared and the MYRECON bit of the Diagnostic Status Register is set.

Table 6.1 - Read Register Summary

REGISTER	READ MSB							LSB	ADDR
STATUS	RI/TRI	X/RI	X/TA	POR	TEST	RECON	TMA	TA/ TTA	**00**
DIAG. STATUS	MY-RECON	DUPID	RCV-ACT	TOKEN	EXC-NAK	TENTID	NEW NEXTID	X	**01**
ADDRESS PTR HIGH	RD-DATA	AUTO-INC	X	X	DMA-EN	A10	A9	A8	**02**
ADDRESS PTR LOW	A7	A6	A5	A4	A3	A2	A1	A0/ SWAP	**03**
DATA*	D7	D6	D5	D4	D3	D2	D1	D0	**04**
SUB ADR	(R/W)*	0	0	0	(R/W)*	SUB-AD2	SUB-AD1	SUB-AD0	**05**
CONFIG-URATION	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	**06**
TENTID	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	**07-0**
NODE ID	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	**07-1**
SETUP1	P1 MODE	FOUR NAKS	X	RCV-ALL	CKP3	CKP2	CKP1	SLOW-ARB	**07-2**
NEXT ID	NXT ID7	NXT ID6	NXT ID5	NXT ID4	NXT ID3	NXT ID2	NXT ID1	NXT ID0	**07-3**
SETUP2	RBUS-TMG	X	CKUP1	CKUP0	EF	NO-SYNC	RCN-TM1	RCM-TM2	**07-4**
BUS CONTROL	W16	X	ITCEN/ RTRG	TC8/ RSYN/ GTTM	DMA-MD1	DMA-MD0	TCPOL	DRQ-POL	**07-5**
DMA COUNT	TC7/ TIM7/ CYC7	TC6/ TIM6/ CYC6	TC5/ TIM5/ CYC5	TC4/ TIM4/ CYC4	TC3/ TIM3/ CYC3	TC2/ TIM2/ CYC2	TC1/ TIM1/ CYC1	TC0/ TIM0/ CYC0	07-6

Note*: This bit can be written and read.

***DATA REGISTER AT 16 BIT ACCESS**

REGISTER	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDR
DATA	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	04

Table 6.2 - Write Register Summary

ADDR	WRITE MSB							LSB	REGISTER
00	RI/TR1	0	0	DMA END	EXCNAK	RECON	NEW NEXTID	TA/ TTA	**INTERRUPT MASK**
01	C7	C6	C5	C4	C3	C2	C1	C0	**COMMAND**
02	RD-DATA	AUTO-INC	0	0	DMAEN	A10	A9	A8	**ADDRESS PTR HIGH**
03	A7	A6	A5	A4	A3	A2	A1	A0/ SWAP	**ADDRESS PTR LOW**
04	D7	D6	D5	D4	D3	D2	D1	D0	**DATA***
05	(R/W)*	0	0	0	(R/W)*	SUB-AD2	SUB-AD1	SUB-AD0	**SUBADR**
06	RESET	CCHEN	TXEN	ET1	ET2	BACK-PLANE	SUB-AD1	SUB-AD0	**CONFIG-URATION**
07-0	TID7	TID6	TID5	TID4	TID3	TID2	TID1	TID0	**TENTID**
07-1	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	**NODEID**
07-2	P1-MODE	FOUR NAKS	0	RCV-ALL	CKP3	CKP2	CKP1	SLOW-ARB	**SETUP1**
07-3	0	0	0	0	0	0	0	0	**TEST**
07-4	RBUS-TMG	0	CKUP1	CKUP0	EF	NO-SYNC	RCN-TM1	RCN-TM0	**SETUP2**
07-5	W16	0	ITCEN/ RTRG	TC8/ RSYN/ GTTM	DMA-MD1	DMA-MD0	TC-POL	DRQ-POL	**BUS CONTROL**
07-6	TC7/ TIM7/ CYC7	TC6/ TIM6/ CYC6	TC5/ TIM5/ CYC5	TC4/ TIM4/ CYC4	TC3/ TIM3/ CYC3	TC2/ TIM2/ CYC2	TC1/ TIM1/ CYC1	TC0/ TIM0/ CYC0	**DMA COUNT**

Note*: This bit can be written and read.

***DATA REGISTER AT 16 BIT ACCESS**

REGISTER	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDR
DATA	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	04

6.2 Internal Registers

The COM20022I contains 16 internal registers. Table 6.1 and Table 6.2 illustrate the COM20022I register map. All undefined bits are read as undefined and must be written as logic "0".

6.2.1 Interrupt Mask Register (IMR)

The COM20022I is capable of generating an interrupt signal when certain status bits become true. A write to the IMR specifies which status bits will be enabled to generate an interrupt. The bit positions in the IMR are in the same position as their corresponding status bits in the Status Register and Diagnostic Status Register. A logic "1" in a particular position enables the corresponding interrupt. The Status bits capable of generating an interrupt include the Receiver Inhibited bit, DMAEND bit (new to the COM20022I), New Next

ID bit, Excessive NAK bit, Reconfiguration Timer bit, and Transmitter Available bit. DMAEND bit is inverted DMAEN bit on ADDRESS PTR High register. No other Status or Diagnostic Status bits can generate an interrupt.

The six maskable status bits are ANDed with their respective mask bits, and the results are ORed to produce the interrupt signal. An RI or TA interrupt is masked when the corresponding mask bit is reset to logic "0", but will reappear when the corresponding mask bit is set to logic "1" again, unless the interrupt status condition has been cleared by this time. A RECON interrupt is cleared when the "Clear Flags" command is issued. An EXCNAK interrupt is cleared when the "POR Clear Flags" command is issued. A New Next ID interrupt is cleared by reading the Next ID Register. If the DMAEND bit is not masked, the interrupt occurs by finishing the DMA operation. The Interrupt Mask Register defaults to the value 0000 0000 upon hardware reset.

6.2.2 Data Register

This read/write 8-bit register is used as the channel through which the data to and from the RAM passes. The data is placed in or retrieved from the address location presently specified by the address pointer. The contents of the Data Register are undefined upon hardware reset. In case of READ operation, the Data Register is loaded with the contents of COM20022I Internal Memory upon writing Address Pointer low only once.

The SWAP bit is used to swap the upper and lower data byte. The SWAP bit is located at bit 0 of ADDRESS PTR_LOW register. When 16 bit access is enabled, (W16=1), A0 becomes the SWAP bit.

6.2.3 Tentative ID Register

The Tentative ID Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Tentative ID Register can be used while the node is on-line to build a network map of those nodes existing on the network. It minimizes the need for operator interaction with the network. The node determines the existence of other nodes by placing a Node ID value in the Tentative ID Register and waiting to see if the Tentative ID bit of the Diagnostic Status Register gets set. The network map developed by this method is only valid for a short period of time, since nodes may join or depart from the network at any time. When using the Tentative ID feature, a node cannot detect the existence of the next logical node to which it passes the token. The Next ID Register will hold the ID value of that node. The Tentative ID Register defaults to the value 0000 0000 upon hardware reset only.

6.2.4 Node ID Register

The Node ID Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Node ID Register contains the unique value which identifies this particular node. Each node on the network must have a unique Node ID value at all times. The Duplicate ID bit of the Diagnostic Status Register helps the user find a unique Node ID. Refer to the Initialization Sequence section for further detail on the use of the DUPID bit. The core of the COM20022I does not wake up until a Node ID other than zero is written into the Node ID Register. During this time, no microcode is executed, no tokens are passed by this node, and no reconfigurations are caused by this node. Once a non-zero NodeID is placed into the Node ID Register, the core wakes up but will not join the network until the TXEN bit of the Configuration Register is set. While the Transmitter is disabled, the Receiver portion of the device is still functional and will provide the user with useful information about the network. The Node ID Register defaults to the value 0000 0000 upon hardware reset only.

6.2.5 Next ID Register

The Next ID Register is an 8-bit, read-only register, accessed when the sub-address bits are set up accordingly (please refer to the Configuration Register and SUB ADR Register). The Next ID Register holds the value of the Node ID to which the COM20022I will pass the token. When used in conjunction with the Tentative ID Register, the Next ID Register can provide a complete network map. The Next ID Register is updated each time a node enters/leaves the network or when a network reconfiguration occurs. Each time the microsequencer updates the Next ID Register, a New Next ID interrupt is generated. This bit is cleared by reading the Next ID Register. Default value is 0000 0000 upon hardware or software reset.

6.2.6 Status Register

The COM20022I Status Register is an 8-bit read-only register. All of the bits, except for bits 5 and 6, are software compatible with previous SMSC ARCNET devices. In previous SMSC ARCNET devices the Extended Timeout status was provided in bits 5 and 6 of the Status Register. In the COM20022I, the COM20020, the COM90C66, and the COM90C165, COM20020-5, COM20051 and COM20051+ these bits exist in and are controlled by the Configuration Register. The Status Register contents are defined as in Table 6.3, but are defined differently during the Command Chaining operation. Please refer to the Command Chaining section for the definition of the Status Register during Command Chaining operation. The Status Register defaults to the value 1XX1 0001 upon either hardware or software reset.

6.2.7 Diagnostic Status Register

The Diagnostic Status Register contains seven read-only bits which help the user troubleshoot the network or node operation. Various combinations of these bits and the TXEN bit of the Configuration Register represent different situations. All of these bits, except the Excessive NAcK bit and the New Next ID bit, are reset to logic "0" upon reading the Diagnostic Status Register or upon software or hardware reset. The EXCNAK bit is reset by the "POR Clear Flags" command or upon software or hardware reset. The Diagnostic Status Register defaults to the value 0000 000X upon either hardware or software reset.

6.2.8 Command Register

Execution of commands are initiated by performing microcontroller writes to this register. Any combinations of written data other than those listed in Table 6.5 are not permitted and may result in incorrect chip and/or network operation.

6.2.9 Address Pointer Registers

These read/write registers are each 8-bits wide and are used for addressing the internal RAM. New pointer addresses should be written by first writing to the High Register and then writing to the Low Register because writing to the Low Register loads the address. The contents of the Address Pointer High and Low Registers are undefined upon hardware reset. Writing to Address Pointer low loads the address.

The DMAEN bit (new to the COM20022I) is located at bit 3 of the ADDRESS PTR HIGH register. The DMAEN bit is used to Disable/Enable the assertion of the DMA Request (DREQ pin) after writing the Address Pointer Low register. The SWAP bit (new to the COM20022I) is located at bit 0 of Address Pointer Low register. The SWAP bit is used to swap the upper and lower data byte. When 16 bit access is enabled, (W16=1), A0 becomes the SWAP bit.

6.2.10 Configuration Register

The Configuration Register is a read/write register which is used to configure the different modes of the COM20022I. The Configuration Register defaults to the value 0001 1000 upon hardware reset only. SUBAD0 and SUBAD1 point to the selection in Register 7.

6.2.11 Sub-Address Register

The sub-address register is new to the COM20022I, previously a reserved register. Bits 2, 1 and 0 are used to select one of the registers assigned to address 7h. SUBAD1 and SUBAD0. They are exactly same as those in the Configuration register. If the SUBAD1 and SUBAD0 bits in the Configuration register are changed, the SUBAD1and SUBAD0 in the Sub-Address register are also changed. SUBAD2 is a new sub-address bit. It Is used to access the 3 new Set Up registers, SETUP2, BUS CONTROL and DMA COUNT. These registers are selected by setting SUBAD2=1. The SUBAD2 bit is cleared automatically by writing the Configuration register.

Write Bits[7:3] to '0' for proper operation.

6.2.12 Setup 1 Register

The Setup 1 Register is a read/write 8-bit register accessed when the Sub Address Bits are set up accordingly (see the bit definitions of the Configuration Register). The Setup 1 Register allows the user to change the network speed (data rate) or the arbitration speed independently, invoke the Receive All feature and change the nPULSE1 driver type. The data rate may be slowed to 156.25Kbps and/or the arbitration speed may be slowed by a factor of two. The Setup 1 Register defaults to the value 0000 0000 upon hardware reset only.

6.2.13 Setup 2 Register

The Setup 2 Register is new to the COM20022I. It is an 8-bit read/write register accessed when the Sub Address Bits SUBAD[2:0] are set up accordingly (see the bit definitions of the Sub Address Register). This register contains bits for various functions. The CKUP1,0 bits select the clock to be generated from the 20 MHz crystal. The RBUSTMG bit is used to Disable/Enable Fast Read function for High Speed CPU bus support. The EF bit is used to enable the new timing for certain functions in the COM20022I (if EF = 0, the timing is the same as in the COM20020 Rev. B). See Appendix "A". The NOSYNC bit is used to enable the NOSYNC function during initialization. If this bit is reset, the line has to be idle for the RAM initialization sequence to be written. If set, the line does not have to be idle for the initialization sequence to be written. See Appendix "A".

The RCNTM[1,0] bits are used to set the time-out period of the recon timer. Programming this timer for shorter time periods has the benefit of shortened network reconfiguration periods. The time periods shown in the table on the following page are limited by a maximum number of nodes in the network. These time-out period values are for 10Mbps. For other data rates, scale the time-out period time values accordingly; the maximum node count remains the same.

RCNTM1	RCNTM0	TIME-OUT PERIOD	MAX NODE COUNT
0	0	210 mS	Up to 255 nodes
0	1	52.5 mS	Up to 64 nodes
1	0	26.25 mS	Up to 32 nodes
1	1	13.125 mS*	Up to 16 nodes **(Note 6.1)**

Note 6.1 The node ID value 255 must exist in the network for the 13.125 mS time-out to be valid.

6.3 Bus Control Register

The Bus Control Register is new to the COM20022I. It is an 8-bit read/write register accessed when the Sub Address Bits SUBAD[2:0] are set up accordingly (see the bit definitions of the Sub Address Register). This register contains bits for control of the DMA functionality. The DRQPOL bit is used to set the active polarity of the DREQ pin. The TCPOL bit is used to set the active polarity of TC pin.

The DMAMD[0,1] bits select the data transfer mode of the DMA, either non-burst, burst, Programmable-Burst by timer or programmable burst by cycle counter.

This transfer mode influences to the timing the DREQ pin. The use of the ITCEN/RTRG bit transfer mode dependent. ITCEN is the Internal Terminal Counter Enable. It is used to select whether the DMA is terminated by external TC or by either internal or external TC. ITCEN is for Non-Burst or Burst mode. RTRG selects the re-trigger mode as either external or internal. It is for the two Programmable-Burst modes. If RTRG = 0, the deasserted DREQ pin is reasserted on the falling edge of the nREFEX pin. If RTRG = 1, the deasserted DREQ pin is reasserted by the timeout of the internal timer (350 ns or 750 ns, as selected by the GTTM bit.) See Figure below.

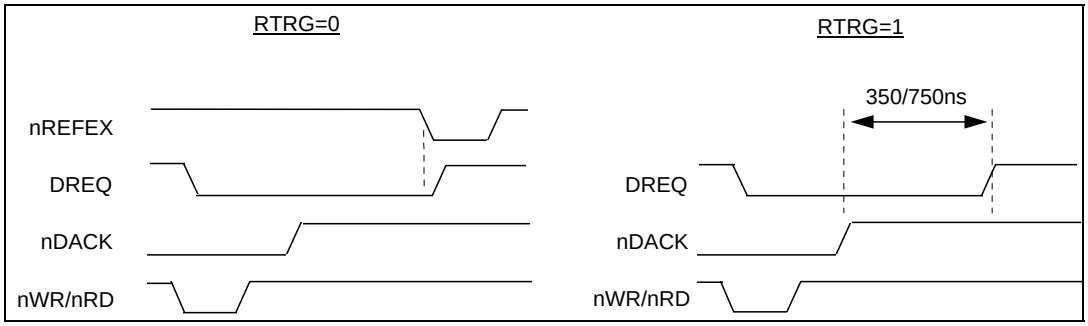


Figure 6.1 - Illustration of the Effect of RTRG Bit on DMA Timing

The use of the TC8/RSYN/GTTM bit is also transfer mode dependent. TC8 is bit 8 of the Terminal Count register. RSYN is the refresh synchronous bit; it is used to select whether the DMA is started immediately or after Refresh execution. GTTM is the Gate Time bit; it is used to select the gate time of the Programmable-Burst transfer.

TC8 is for Non-Burst or Burst mode. RSYN and GTTM are for the two Programmable-Burst modes.

The W16 bit is used to enable/disable the 16 bit access.

6.4 DMA Count Register

The DMA COUNT Register is new to the COM20022I. It is an 8-bit read/write register accessed when the Sub Address Bits SUBAD[2:0] are set up accordingly (see the bit definitions of the Sub Address Register). This register contains bits for control of the DMA functionality. The TC7-TC0 /TIM7-TIM0 /CYC7-CYC0 bits have one of three functions depending on the DMA transfer mode. TC7-TC0 are for Non-Burst or Burst mode. These are the lower 8 bits of the Terminal Count setting register (the MSB is in the Bus Control Register). The TIM7-TIM0 bits are for setting the time of the continuous DMA transfer in Programmable-Burst by Timer mode. The CYC7-CYC0 bits are for setting the cycle count value of the continuous DMA transfer in Programmable-Burst by cycle mode.

Table 6.3 - Status Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Receiver Inhibited	RI	This bit, if high, indicates that the receiver is not enabled because either an "Enable Receive to Page fnn" command was never issued, or a packet has been deposited into the RAM buffer page fnn as specified by the last "Enable Receive to Page fnn" command. No messages will be received until this command is issued, and once the message has been received, the RI bit is set, thereby inhibiting the receiver. The RI bit is cleared by issuing an "Enable Receive to Page fnn" command. This bit, when set, will cause an interrupt if the corresponding bit of the Interrupt Mask Register (IMR) is also set. When this bit is set and another station attempts to send a packet to this station, this station will send a NAK.
6,5	(Reserved)		These bits are undefined.
4	Power On Reset	POR	This bit, if high, indicates that the COM20022I has been reset by either a software reset, a hardware reset, or writing 00H to the Node ID Register. The POR bit is cleared by the "Clear Flags" command.
3	Test	TEST	This bit is intended for test and diagnostic purposes. It is a logic "0" under normal operating conditions.
2	Reconfiguration	RECON	This bit, if high, indicates that the Line Idle Timer has timed out because the RXIN pin was idle for 20.5μS. The RECON bit is cleared during a "Clear Flags" command. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. The interrupt service routine should consist of examining the MYRECON bit of the Diagnostic Status Register to determine whether there are consecutive reconfigurations caused by this node.
1	Transmitter Message Acknowledged	TMA	This bit, if high, indicates that the packet transmitted as a result of an "Enable Transmit from Page fnn" command has been acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast messages are never acknowledged. The TMA bit is cleared by issuing the "Enable Transmit from Page fnn" command.
0	Transmitter Available	TA	This bit, if high, indicates that the transmitter is available for transmitting. This bit is set when the last byte of scheduled packet has been transmitted out, or upon execution of a "Disable Transmitter" command. The TA bit is cleared by issuing the "Enable Transmit from Page fnn" command after the node next receives the token. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set.

Table 6.4 - Diagnostic Status Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	My Reconfiguration	MY-RECON	This bit, if high, indicates that a past reconfiguration was caused by this node. It is set when the Lost Token Timer times out, and should be typically read following an interrupt caused by RECON. Refer to the Improved Diagnostics section for further detail.
6	Duplicate ID	DUPID	This bit, if high, indicates that the value in the Node ID Register matches both Destination ID characters of the token and a response to this token has occurred. Trailing zero's are also verified. A logic "1" on this bit indicates a duplicate Node ID, thus the user should write a new value into the Node ID Register. This bit is only useful for duplicate ID detection when the device is off line, that is, when the transmitter is disabled. When the device is on line this bit will be set every time the device gets the token. This bit is reset automatically upon reading the Diagnostic Status Register. Refer to the Improved Diagnostics section for further detail.
5	Receive Activity	RCVACT	This bit, if high, indicates that data activity (logic "1") was detected on the RXIN pin of the device. Refer to the Improved Diagnostics section for further detail.
4	Token Seen	TOKEN	This bit, if high, indicates that a token has been seen on the network, sent by a node other than this one. Refer to the Improved Diagnostic section for further detail.
3	Excessive NAK	EXCNAK	This bit, if high, indicates that either 128 or 4 Negative Acknowledgements have occurred in response to the Free Buffer Enquiry. This bit is cleared upon the "POR Clear Flags" command. Reading the Diagnostic Status Register does not clear this bit. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. Refer to the Improved Diagnostics section for further detail.
2	Tentative ID	TENTID	This bit, if high, indicates that a response to a token whose DID matches the value in the Tentative ID Register has occurred. The second DID and the trailing zero's are not checked. Since each node sees every token passed around the network, this feature can be used with the device on-line in order to build and update a network map. Refer to the Improved Diagnostics section for further detail.
1	New Next ID	NEW NXTID	This bit, if high, indicates that the Next ID Register has been updated and that a node has either joined or left the network. Reading the Diagnostic Status Register does not clear this bit. This bit, when set, will cause an interrupt if the corresponding bit in the IMR is also set. The bit is cleared by reading the Next ID Register.
1,0	(Reserved)		These bits are undefined.

Table 6.5 - Command Register

DATA	COMMAND	DESCRIPTION
0000 0000	Clear Transmit Interrupt	This command is used only in the Command Chaining operation. Please refer to the Command Chaining section for definition of this command.
0000 0001	Disable Transmitter	This command will cancel any pending transmit command (transmission that has not yet started) and will set the TA (Transmitter Available) status bit to logic "1" when the COM20022I next receives the token.
0000 0010	Disable Receiver	This command will cancel any pending receive command. If the COM20022I is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set to logic "1" the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
b0fn n100	Enable Receive to Page fnn	This command allows the COM20022I to receive data packets into RAM buffer page fnn and resets the RI status bit to logic "0". The values placed in the "nn" bits indicate the page that the data will be received into (page 0, 1, 2, or 3). If the value of "f" is a logic "1", an offset of 256 bytes will be added to that page specified in "nn", allowing a finer resolution of the buffer. Refer to the Selecting RAM Page Size section for further detail. If the value of "b" is logic "1", the device will also receive broadcasts (transmissions to ID zero). The RI status bit is set to logic "1" upon successful reception of a message.
00fn n011	Enable Transmit from Page fnn	This command prepares the COM20022I to begin a transmit sequence from RAM buffer page fnn the next time it receives the token. The values of the "nn" bits indicate which page to transmit from (0, 1, 2, or 3). If "f" is logic "1", an offset of 256 bytes is the start of the page specified in "nn", allowing a finer resolution of the buffer. Refer to the Selecting RAM Page Size section for further detail. When this command is loaded, the TA and TMA bits are reset to logic "0". The TA bit is set to logic "1" upon completion of the transmit sequence. The TMA bit will have been set by this time if the device has received an ACK from the destination node. The ACK is strictly hardware level, sent by the receiving node before its microcontroller is even aware of message reception. Refer to Figure 3.1 for details of the transmit sequence and its relation to the TA and TMA status bits.
0000 c101	Define Configuration	This command defines the maximum length of packets that may be handled by the device. If "c" is a logic "1", the device handles both long and short packets. If "c" is a logic "0", the device handles only short packets.
000r p110	Clear Flags	This command resets certain status bits of the COM20022I. A logic "1" on "p" resets the POR status bit and the EXCNAK Diagnostic status bit. A logic "1" on "r" resets the RECON status bit.
0000 1000	Clear Receive Interrupt	This command is used only in the Command Chaining operation. Please refer to the Command Chaining section for definition of this command.
0001 1000	Start Internal Operation	This command restarts the stopped internal operation after changing CKUP1 or CKUP0 bit.
0001 0000	Clear Mask bit of DMAEND	This command resets a mask bit of the DMAEND. It is for clearing interrupt by DMA transfer finished.

Table 6.6 - Address Pointer High Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Read Data	RDDATA	This bit tells the COM20022I whether the following access will be a read or write. A logic "1" prepares the device for a read, a logic "0" prepares it for a write.
6	Auto Increment	AUTOINC	This bit controls whether the address pointer will increment automatically. A logic "1" on this bit allows automatic increment of the pointer after each access, while a logic "0" disables this function. Please refer to the Sequential Access Memory section for further detail.
5-4	(Reserved)		These bits are undefined.
3	DMA Enable	DMAEN	This bit is used to Disable/Enable the assertion of the DMA Request (DREQ pin) after writing the Address Pointer Low register. DMAEN=0: Disable (Default). DMAEN=1: Enable the assertion of the DREQ pin after writing the Address Pointer Low register. Writing DMAEN=0 during the DMA operation will negate the DREQ pin immediately. The DMA operation is terminated immediately after the next DACK pin negation. The inverting signal of DAMEN is the Interrupt source signal DMAEND. The DMAEN bit is cleared automatically by finishing the DMA. If the DMAEND bit in the Mask register is not masked, the Interrupt occurs by finishing the DMA operation.
2-0	Address 10-8	A10-A8	These bits hold the upper three address bits which provide addresses to RAM.

Table 6.7 - Address Pointer Low Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7-0	Address 7-0	A7-A0 SWAP	These bits hold the lower 8 address bits which provide the addresses to RAM. When 16 bit access is enabled, (W16=1), A0 becomes the SWAP bit. Swap bit is undefined after a hardware reset. The swap bit must be set before W16 bit is set to "1". The swap bit is used to swap the upper and lower data byte. The swap bit influences both CPU cycle and DMA cycle. See Table Below.

Detected Host Interface Mode	Swap Bit	D15-D8 Pin	D7-D0 Pin
Intel 80xx Mode	0	Odd	Even
(RD, WR Mode)	1	Even	Odd
Motorola 68xx Mode	0	Even	Odd
(DIR, DS Mode)	1	Odd	Even

Table 6.8 - Sub Address Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7-3	Reserved		These bits are undefined.
2,1,0	Sub Address 2,1,0	SUBAD 2,1,0	These bits determine which register at address 07 may be accessed. The combinations are as follows:

SUBAD2	SUBAD1	SUBAD0	Register
0	0	0	Tentative ID \ (Same
0	0	1	Node ID \ as in
0	1	0	Setup 1 / Config
0	1	1	Next ID / Register)
1	0	0	Setup 2
1	0	1	Bus Control
1	1	0	DMA Count
1	1	1	Reserved

SUBAD1 and SUBAD0 are exactly the same as exist in the Configuration Register. SUBAD2 is cleared automatically by writing the Configuration Register.

Table 6.9 - Configuration Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Reset	RESET	A software reset of the COM20022I is executed by writing a logic "1" to this bit. A software reset does not reset the microcontroller interface mode, nor does it affect the Configuration Register. The only registers that the software reset affect are the Status Register, the Next ID Register, and the Diagnostic Status Register. This bit must be brought back to logic "0" to release the reset.
6	Command Chaining Enable	CCHEN	This bit, if high, enables the Command Chaining operation of the device. Please refer to the Command Chaining section for further details. A low level on this bit ensures software compatibility with previous SMSC ARCNET devices.
5	Transmit Enable	TXEN	When low, this bit disables transmissions by keeping nPULSE1, nPULSE2 if in non-Backplane Mode, and nTXEN pin inactive. When high, it enables the above signals to be activated during transmissions. This bit defaults low upon reset. This bit is typically enabled once the Node ID is determined, and never disabled during normal operation. Please refer to the Improved Diagnostics section for details on evaluating network activity.
4,3	Extended Timeout 1,2	ET1, ET2	These bits allow the network to operate over longer distances than the default maximum 1 mile by controlling the Response, Idle, and Reconfiguration Times. All nodes should be configured with the same timeout values for proper network operation. For the COM20022I with a 20 MHz crystal oscillator, the bit combinations follow:
			ET2 / ET1 / Response Time (µS) / Idle Time (µS) / Reconfig Time (mS) 0 / 0 / 298.4 / 328 / 420 0 / 1 / 149.2 / 164 / 420 1 / 0 / 74.7 / 82 / 420 1 / 1 / 18.7 / 20.5 / 210
			Note: These values are for 10Mbps and RCNTMR[1,0]=00. Reconfiguration time is changed by the RCNTMR1 and RCNTMR0 bits.
2	Backplane	BACK-PLANE	A logic "1" on this bit puts the device into Backplane Mode signaling which is used for Open Drain and Differential Driver interfaces.
1,0	Sub Address 1,0	SUBAD 1,0	These bits determine which register at address 07 may be accessed. The combinations are as follows: SUBAD1 / SUBAD0 / Register 0 / 0 / Tentative ID 0 / 1 / Node ID 1 / 0 / Setup 1 1 / 1 / Next ID See also the Sub Address Register.

Table 6.10 - Setup 1 Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Pulse1 Mode	P1MODE	This bit determines the type of PULSE1 output driver used in Backplane Mode. When high, a push/pull output is used. When low, an open drain output is used. The default is open drain.
6	Four NACKS	FOUR NACKS	This bit, when set, will cause the EXNACK bit in the Diagnostic Status Register to set after four NACKs to Free Buffer Enquiry are detected by the COM20022I. This bit, when reset, will set the EXNACK bit after 128 NACKs to Free Buffer Enquiry. The default is 128.
5	Reserved		Do not set.
4	Receive All	RCVALL	This bit, when set, allows the COM20022I to receive all valid data packets on the network, regardless of their destination ID. This mode can be used to implement a network monitor with the transmitter on- or off-line. Note that ACKs are only sent for packets received with a destination ID equal to the COM20022I's programmed node ID. This feature can be used to put the COM20022I in a 'listen-only' mode, where the transmitter is disabled and the COM20022I is not passing tokens. Defaults low.
3,2,1	Clock Prescaler Bits 3,2,1	CKP3,2,1	These bits are used to determine the data rate of the COM20022I. The following table is for a 20 MHz crystal: (Clock Multiplier is bypassed) CKP3 CKP2 CKP1 DIVISOR SPEED 0 0 0 8 2.5Mbs 0 0 1 16 1.25Mbs 0 1 0 32 625Kbs 0 1 1 64 312.5Kbs 1 0 0 128 156.25Kbs **Note:** The lowest data rate achievable by the COM20022I is 156.25Kbs. Defaults to 000 or 2.5Mbs. For Clock Multiplier output clock speed greater than 20 MHz, CKP3, CKP2 and CKP1 must all be zero.
0	Slow Arbitration Select	SLOWARB	This bit, when set, will divide the arbitration clock by 2. Memory cycle times will increase when slow arbitration is selected. **Note:** For clock multiplier output clock speeds greater than 40 MHz, SLOWARB must be set. Defaults to low.

Table 6.11 - Setup 2 Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Read Bus Timing Select	RBUSTMG	This bit is used to Disable/Enable the High Speed CPU Read function for High Speed CPU bus support. RBUSTMG=0: Disable (Default), RBUSTMG=1: Enable. That is, if BUSTMG (pin 26) = 1 and RBUSTMG = 1, High Speed CPU Read operations are enabled. It does not influence write operation. High speed CPU Read operation is only for non-multiplexed bus.
6	Reserved		This bit is undefined.
5,4	Clock Multiplier	CKUP1, 0	Higher frequency clocks are generated from the 20 MHz crystal through the selection of these two bits as shown. This clock multiplier is powered-down on default. After changing the CKUP1 and CKUP0 bits, the ARCNET core operation is stopped and the internal PLL in the clock multiplier is awakened and it starts to generate the 40 MHz. The lock out time of the internal PLL is 8µSec typically. After 1 mS it is necessary to write command data '18H' to command register for re-starting the ARCNET core operation. EF bit must be '1' if the data rate is over 5Mbps. CAUTION: Changing the CKUP1 and CKUP0 bits must be one time or less after releasing a hardware reset. CKUP1 / CKUP0 / Clock Frequency (Data Rate) 0 / 0 / 20 MHz (Up to 2.5Mbps) Default 0 / 1 / 40 MHz (Up to 5Mbps) 1 / 0 / Reserved 1 / 1 / 80 MHz (Only 10Mbps) **Note:** After changing the CKUP1 or CKUP0 bits, it is necessary to write a command data '18H' to the command register. Because after changing the CKUP [1, 0] bits, the internal operation is stopped temporarily. The writing of the command is to start the operation. These initializing steps are shown below. 1. Hardware reset (Power ON) 2. Change CKUP[1, 0] bit 3. Wait 1mSec (wait until stable oscillation) 4. Write command '18H' (start internal operation) 5. Start initializing routine (Execute existing software)
3	Enhanced Functions	EF	This bit is used to enable the new enhanced functions in the COM20022I. EF = 0: Disable (Default), EF = 1: Enable. If EF = 0, the timing and function is the same as in the COM20020, Revision B. See appendix "A". EF bit must be '1' if the data rate is over 5Mbps. EF bit should be '1' for new design customers. EF bit should be '0' for replacement customers.
2	No Synchronous	NOSYNC	This bit is used to enable the SYNC command during initialization. NOSYNC= 0, Enable (Default) The line must be idle for the RAM initialization sequence to be written. NOSYNC= 1, Disable:) The line does not have to be idle for the RAM initialization sequence to be written. See appendix "A".

BIT	BIT NAME	SYMBOL	DESCRIPTION
1,0	Reconfiguration Timer 1, 0	RCNTM1,0	These bits are used to program the reconfiguration timer as a function of maximum node count. These bits set the time out period of the reconfiguration timer as shown below. The time out periods shown are for 10 Mbps. RCNTM1 RCNTM0 Time Out Period Max Node Count 0 0 210 mS Up to 255 nodes 0 1 52.5 mS Up to 64 nodes 1 0 26.25 mS Up to 32 nodes 1 1 13.125 mS* Up to 16 nodes **Note*:** The node ID value 255 must exist in the network for 13.125 mS timeout to be valid.

Table 6.12 - Bus Control Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	16 Bit Access	W16	This bit is used to Disable/Enable the 16 bit access. It influences both CPU cycle and DMA cycle. W16= 0: Disable (Default); W16= 1: Enable
6	Reserved		This bit is undefined.
5	Internal Terminal Counter Enable; Re-Trigger mode	ITCEN/ RTRG	The function of this bit is mode dependent. ITCEN is for Non-Burst or Burst mode. RTRG is for the two Programmable-Burst modes. ITCEN = 0: Terminate the DMA only by External TC. ITCEN = 1: Terminate the DMA by Internal or External TC. RTRG = 0: External Re-Trigger mode; Negated DREQ pin is Re-asserted by falling edge of nREFEX pin. RTRG = 1: Internal Re-Trigger mode; Negated DREQ pin is Re-asserted by timeout of internal gate timer (350ns/750ns).
4	Terminal Count Bit 8 Refresh Synchronous Gate Time	TC8/ RSYN/ GTTM	The function of this bit is mode dependent. TC8 is for Non-burst or burst mode. RSYN and GTTM are for the two Programmable-Burst modes. RSYN is for External Re-Trigger mode. GTTM is for internal Re-Trigger mode. Non-burst or burst mode: TC8: Bit 8 (MSB) of 9 bit Terminal Count setting register. The other 8 bits are in the DMA Count register. Terminal Count setting register is ignored when ITCEN = 0. Programmable-Burst and External Re-Trigger mode: RSYN = 0: DMA is started Immediately. RSYN = 1: DMA is started after Refresh execution. Programmable-Burst and Internal Re-Trigger mode: GTTM = 0: Gate Time is 350nS (min) GTTM = 1: Gate Time is 750nS (min)
3,2	DMA Transfer Mode	DMAMD1,DMAMD0	These bits select the data transfer mode of the DMA. These transfer modes influence the timing of asserting/negating the DREQ pin. DMAMD1 DMAMD0 Transfer Mode 0 0 Non-Burst (Default) 0 1 Burst 1 0 Programmable-Burst by Timer 1 1 Programmable-Burst by Cycle Counter
1	TC Polarity	TCPOL	This bit sets the Active polarity of TC pin. TCPOL = 0: Active High (Default), TCPOL = 1 Active Low
0	DREQ Polarity	DRQPOL	This bit sets the Active polarity of DREQ pin. DRQPOL = 0: Active High (Default), DRQPOL = 1 Active Low

Table 6.13 - DMA Count Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7-0	Terminal Count	TC7-TC0	TC7-TC0: Used for non-burst or burst mode. These are the lower 8 bits of the Terminal Count setting register. The MSB (TC8) is in the Bus Control Register. The Terminal Count setting range is from 1 to 512 counts (TC8 - TC0 all zeroes means 512 counts).
	Timer Mode	TIM7-TIM0	TIM7-TIM0: Used for Programmable-Burst by Timer mode. These bits are for setting the term of the continuous DMA transfer. The time range is from 100nS to 25.6µS. The step is 100nS (TIM7-TIM0 all zeroes means 25.6µs).
	Cycle Mode	CYC7-CYC0	CYC7-CYC0: Used for Programmable-Burst by Cycle mode. These bits are for setting the term of the continuous DMA transfer. The cycle range is from 2 to 256 cycles. CYC7-CYC0 all zeroes means 256 cycles. (1 is illegal)

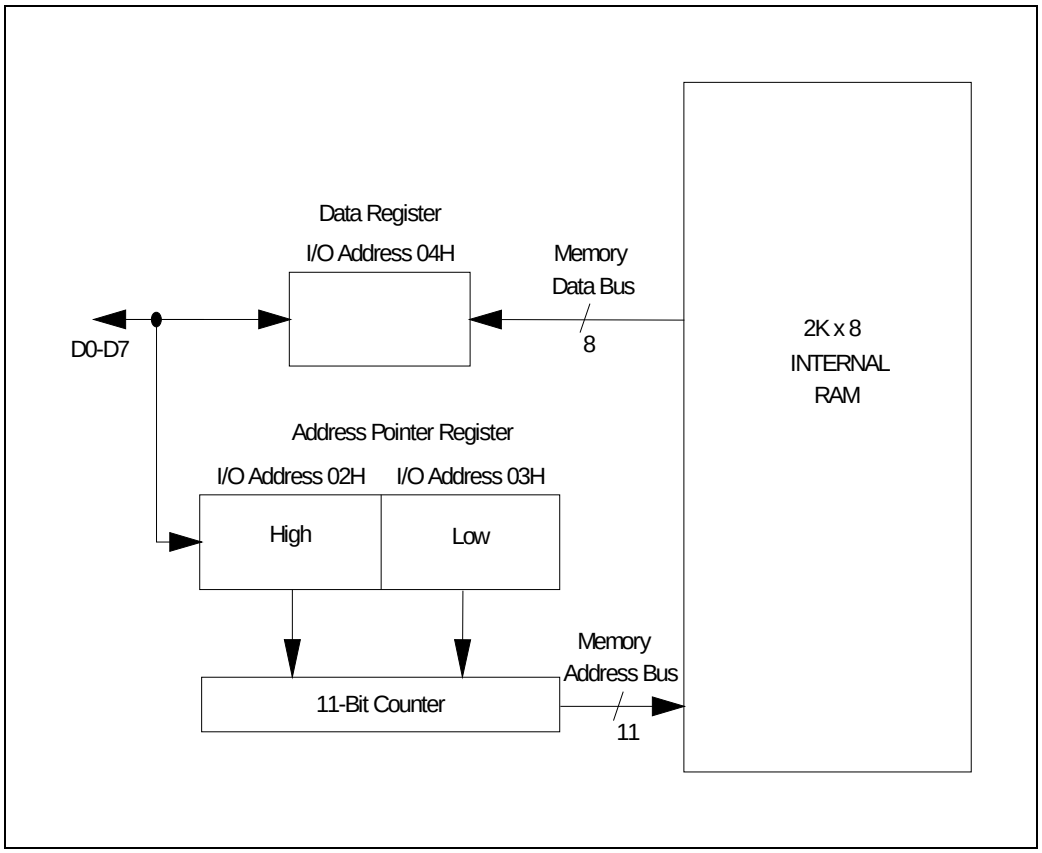


Figure 6.2 - Sequential Access Operation

6.5 Internal RAM

The integration of the 2K x 8 RAM in the COM20022I represents significant real estate savings. The most obvious benefit is the 48 pin package in which the device is now placed (a direct result of the integration of RAM). In addition, the PC board is now free of the cumbersome external RAM, external latch, and multiplexed address/data bus and control functions which were necessary to interface to the RAM. The integration of RAM represents significant cost savings because it isolates the system designer from the changing costs of external RAM and it minimizes reliability problems, assembly time and costs, and layout complexity.

6.5.1 Sequential Access Memory

The internal RAM is accessed via a pointer-based scheme. Rather than interfering with system memory, the internal RAM is indirectly accessed through the Address High and Low Pointer Registers. The data is channeled to and from the microcontroller via the 8-bit data register. For example: a packet in the internal RAM buffer is read by the microcontroller by writing the corresponding address into the Address Pointer High and Low Registers (offsets 02H and 03H). Note that the High Register should be written first, followed by the Low Register, because writing to the Low Register loads the address. At this point the device accesses that location and places the corresponding data into the data register. The microcontroller then reads the data register (offset 04H) to obtain the data at the specified location. If the Auto Increment bit is set to logic "1", the device will automatically increment the address and place the next byte of data into the data register, again to be read by the microcontroller. This process is continued until the entire packet is read out of RAM. Refer to Figure 5.6 for an illustration of the Sequential Access operation. When switching between reads and writes, the pointer must first be written with the starting address. At least one cycle time should separate the pointer being loaded and the first read (see timing parameters).

6.5.2 Access Speed

The COM20022I is able to accommodate very fast access cycles to its registers and buffers. Arbitration to the buffer does not slow down the cycle because the pointer based access method allows data to be prefetched from memory and stored in a temporary register. Likewise, data to be written is stored in the temporary register and then written to memory.

For systems which do not require quick access time, the arbitration clock may be slowed down by setting bit 0 of the Setup1 Register equal to logic "1". Since the Slow Arbitration feature divides the input clock by two, the duty cycle of the input clock may be relaxed.

6.6 Software Interface

The microcontroller interfaces to the COM20022I via software by accessing the various registers. These actions are described in the Internal Registers section. The software flow for accessing the data buffer is based on the Sequential Access scheme. The basic sequence is as follows:

- Disable Interrupts
- Write to Pointer Register High (specifying Auto-Increment mode)
- Write to Pointer Register Low (this loads the address)
- Enable Interrupts
- Read or Write the Data Register (repeat as many times as necessary to empty or fill the buffer)
- The pointer may now be read to determine how many transfers were completed.

The software flow for controlling the Configuration, Node ID, Tentative ID, and Next ID registers is generally limited to the initialization sequence and the maintenance of the network map.

Additionally, it is necessary to understand the details of how the other Internal Registers are used in the transmit and receive sequences and to know how the internal RAM buffer is properly set up. The sequence of events that tie these actions together is discussed as follows.

6.6.1 Selecting RAM Page Size

During normal operation, the 2K x 8 of RAM is divided into four pages of 512 bytes each. The page to be used is specified in the "Enable Transmit (Receive) from (to) Page fnn" command, where "nn" specifies page 0, 1, 2, or 3. This allows the user to have constant control over the allocation of RAM.

When the Offset bit "f" (bit 5 of the "Enable Transmit (Receive) from (to) Page fnn" command word) is set to logic "1", an offset of 256 bytes is added to the page specified. For example: to transmit from the second half of page 0, the command "Enable Transmit from Page fnn" (fnn=100 in this case) is issued by writing 0010 0011 to the Command Register. This allows a finer resolution of the buffer pages without affecting software compatibility. This scheme is useful for applications which frequently use packet sizes of 256 bytes or less, especially for microcontroller systems with limited memory capacity. The remaining portions of the buffer pages which are not allocated for current transmit or receive packets may be used as temporary storage for previous network data, packets to be sent later, or as extra memory for the system, which may be indirectly accessed.

If the device is configured to handle both long and short packets (see "Define Configuration" command), then receive pages should always be 512 bytes long because the user never knows what the length of the receive packet will be. In this case, the transmit pages may be made 256 bytes long, leaving at least 512 bytes free at any given time. Even if the Command Chaining operation is being used, 512 bytes is still guaranteed to be free because Command Chaining only requires two pages for transmit and two for receive (in this case, two 256 byte pages for transmit and two 512 byte pages for receive, leaving 512 bytes free). Please note that it is the responsibility of software to reserve 512 bytes for each receive page if the device is configured to handle long packets. The COM20022I does not check page boundaries during reception. If the device is configured to handle only short packets, then both transmit and receive pages may be allocated as 256 bytes long, freeing at least 1KByte at any given time.

Even if the Command Chaining operation is being used, 1KByte is still guaranteed to be free because Command Chaining only requires two pages for transmit and two for receive (in this case, a total of four 256 byte pages, leaving 1K free).

The general rule which may be applied to determine where in RAM a page begins is as follows:

Address = (nn x 512) + (f x 256).

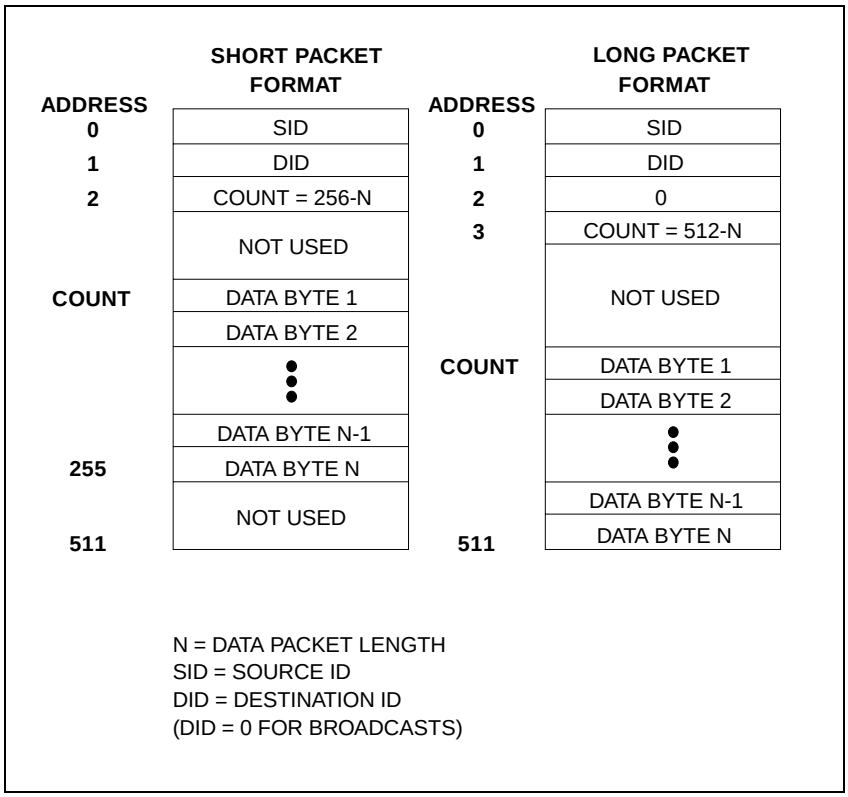


Figure 6.3 - RAM Buffer Packet Configuration

6.6.2 Transmit Sequence

During a transmit sequence, the microcontroller selects a 256 or 512 byte segment of the RAM buffer and writes into it. The appropriate buffer size is specified in the "Define Configuration" command. When long packets are enabled, the COM20022I interprets the packet as either a long or short packet, depending on whether the buffer address 2 contains a zero or non-zero value. The format of the buffer is shown in Figure 5.7 Address 0 contains the Source Identifier (SID); Address 1 contains the Destination Identifier (DID); Address 2 (COUNT) contains, for short packets, the value 256-N, where N represents the number of information bytes in the message, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 (COUNT) would contain the value 512-N, where N represents the number of information bytes in the message. The SID in Address 0 is used by the receiving node to reply to the transmitting node. The COM20022I puts the local ID in this location, therefore it is not necessary to write into this location. Please note that a short packet may contain between 1 and 253 data bytes, while a long packet may contain between 257 and 508 data bytes. A minimum value of 257 exists on a long packet so that the COUNT is expressible in eight bits. This leaves three exception packet lengths which do not fit into either a short or long packet; packet lengths of 254, 255, or 256 bytes. If packets of these lengths must be sent, the user must add dummy bytes to the packet in order to make the packet fit into a long packet.

Once the packet is written into the buffer, the microcontroller awaits a logic "1" on the TA bit, indicating that a previous transmit command has concluded and another may be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted, depending on the traffic on the network and the location of the token at the time the transmit command was issued. The conclusion of the Transmit Command will generate an interrupt if the Interrupt Mask allows it. If the device is configured for the Command Chaining operation, please see the Command Chaining section for further detail on the transmit sequence. Once the TA bit becomes a logic "1", the microcontroller may issue the "Enable Transmit from Page fnn" command, which resets the TA and TMA bits to logic "0". If the

message is not a BROADCAST, the COM20022I automatically sends a FREE BUFFER ENQUIRY to the destination node in order to send the message. At this point, one of four possibilities may occur.

The first possibility is if a free buffer is available at the destination node, in which case it responds with an ACKnowledgement. At this point, the COM20022I fetches the data from the Transmit Buffer and performs the transmit sequence. If a successful transmit sequence is completed, the TMA bit and the TA bit are set to logic "1". If the packet was not transmitted successfully, TMA will not be set. A successful transmission occurs when the receiving node responds to the packet with an ACK. An unsuccessful transmission occurs when the receiving node does not respond to the packet.

The second possibility is if the destination node responds to the Free Buffer Enquiry with a Negative AcKnowledgement. A NAK occurs when the RI bit of the destination node is a logic "1". In this case, the token is passed on from the transmitting node to the next node. The next time the transmitter receives the token, it will again transmit a FREE BUFFER ENQUIRY. If a NAK is again received, the token is again passed onto the next node. The Excessive NAK bit of the Diagnostic Status Register is used to prevent an endless sending of FBE's and NAK's. If no limit of FBE-NAK sequences existed, the transmitting node would continue issuing a Free Buffer Enquiry, even though it would continuously receive a NAK as a response. The EXCNAK bit generates an interrupt (if enabled) in order to tell the microcontroller to disable the transmitter via the "Disable Transmitter" command. This causes the transmission to be abandoned and the TA bit to be set to a logic "1" when the node next receives the token, while the TMA bit remains at a logic "0". Please refer to the Improved Diagnostics section for further detail on the EXCNAK bit.

The third possibility which may occur after a FREE BUFFER ENQUIRY is issued is if the destination node does not respond at all. In this case, the TA bit is set to a logic "1", while the TMA bit remains at a logic "0". The user should determine whether the node should try to reissue the transmit command.

The fourth possibility is if a non-traditional response is received (some pattern other than ACK or NAK, such as noise). In this case, the token is not passed onto the next node, which causes the Lost Token Timer of the next node to time out, thus generating a network reconfiguration.

The "Disable Transmitter" command may be used to cancel any pending transmit command when the COM20022I next receives the token. Normally, in an active network, this command will set the TA status bit to a logic "1" when the token is received. If the "Disable Transmitter" command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, one of three situations exists. Either the node is disconnected from the network, or there are no other nodes on the network, or the external receive circuitry has failed. These situations can be determined by either using the improved diagnostic features of the COM20022I or using another software timeout which is greater than the worst case time for a round trip token pass, which occurs when all nodes transmit a maximum length message.

6.6.3 Receive Sequence

A receive sequence begins with the RI status bit becoming a logic "1", which indicates that a previous reception has concluded. The microcontroller will be interrupted if the corresponding bit in the Interrupt Mask Register is set to logic "1". Otherwise, the microcontroller must periodically check the Status Register. Once the microcontroller is alerted to the fact that the previous reception has concluded, it may issue the "Enable Receive to Page fnn" command, which resets the RI bit to logic "0" and selects a new page in the RAM buffer. Again, the appropriate buffer size is specified in the "Define Configuration" command. Typically, the page which just received the data packet will be read by the microcontroller at this point. Once the "Enable Receive to Page fnn" command is issued, the microcontroller attends to other duties.

There is no way of knowing how long the new reception will take, since another node may transmit a packet at any time. When another node does transmit a packet to this node, and if the "Define Configuration" command has enabled the reception of long packets, the COM20022I interprets the packet as either a long or short packet, depending on whether the content of the buffer location 2 is zero or non-zero. The format of the buffer is shown in Figure 5.7. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 contains the value 512-N, where N represents the message length. Note that on reception,

the COM20022I deposits packets into the RAM buffer in the same format that the transmitting node arranges them, which allows for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer other than the SID and DID. Once the packet is received and stored correctly in the selected buffer, the COM20022I sets the RI bit to logic "1" to signal the microcontroller that the reception is complete.

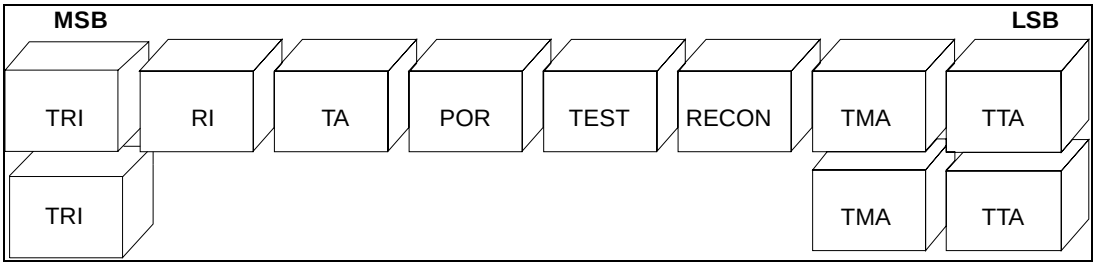


Figure 6.4 - Command Chaining Status Register Queue

6.7 Command Chaining

The Command Chaining operation allows consecutive transmissions and receptions to occur without host microcontroller intervention.

Through the use of a dual two-level FIFO, commands to be transmitted and received, as well as the status bits, are pipelined.

In order for the COM20022I to be compatible with previous SMSC ARCNET device drivers, the device defaults to the non-chaining mode. In order to take advantage of the Command Chaining operation, the Command Chaining Mode must be enabled via a logic "1" on bit 6 of the Configuration Register.

In Command Chaining, the Status Register appears as in Figure 6.4.

The following is a list of Command Chaining guidelines for the software programmer. Further detail can be found in the Transmit Command Chaining and Receive Command Chaining sections.

- The device is designed such that the interrupt service routine latency does not affect performance.
- Up to two outstanding transmissions and two outstanding receptions can be pending at any given time. The commands may be given in any order.
- Up to two outstanding transmit interrupts and two outstanding receive interrupts are stored by the device, along with their respective status bits.
- The Interrupt Mask bits act on TTA (Rising Transition on Transmitter Available) for transmit operations and TRI (Rising Transition of Receiver Inhibited) for receive operations. TTA is set upon completion of a packet transmission only. TRI is set upon completion of a packet reception only. Typically there is no need to mask the TTA and TRI bits after clearing the interrupt.
- The traditional TA and RI bits are still available to reflect the present status of the device.

6.7.1 Transmit Command Chaining

When the processor issues the first "Enable Transmit to Page fnn" command, the COM20022I responds in the usual manner by resetting the TA and TMA bits to prepare for the transmission from the specified page. The TA bit can be used to see if there is currently a transmission pending, but the TA bit is really meant to be used in the non-chaining mode only. The TTA bits provide the relevant information for the device in the Command Chaining mode. In the Command Chaining Mode, at any time after the first command is issued, the processor can issue a second "Enable Transmit from Page fnn" command. The COM20022I stores the fact that the second transmit command was issued, along with the page number.

After the first transmission is completed, the COM20022I updates the Status Register by setting the TTA bit, which generates an interrupt. The interrupt service routine should read the Status Register. At this point, the TTA bit will be found to be a logic "1" and the TMA (Transmit Message Acknowledge) bit will tell the processor whether the transmission was successful. After reading the Status Register, the "Clear Transmit Interrupt" command is issued, thus resetting the TTA bit and clearing the interrupt. Note that only the "Clear Transmit Interrupt" command will clear the TTA bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the transmit operation is double buffered in order to retain the results of the first transmission for analysis by the processor. This information will remain in the Status Register until the "Clear Transmit Interrupt" command is issued. Note that the interrupt will remain active until the command is issued, and the second interrupt will not occur until the first interrupt is acknowledged. The COM20022I guarantees a minimum of 200nS (at EF=1) interrupt inactive time interval between interrupts. The TMA bit is also double buffered to reflect whether the appropriate transmission was a success. The TMA bit should only be considered valid after the corresponding TTA bit has been set to a logic "1". The TMA bit never causes an interrupt.

When the token is received again, the second transmission will be automatically initiated after the first is completed by using the stored "Enable Transmit from Page fnn" command. The operation is as if a new "Enable Transmit from Page fnn" command has just been issued. After the first Transmit status bits are cleared, the Status Register will again be updated with the results of the second transmission and a second interrupt resulting from the second transmission will occur. The COM20022I guarantees a minimum of 200ns (at EF=1) interrupt inactive time interval before the following edge.

The Transmitter Available (TA) bit of the Interrupt Mask Register now masks only the TTA bit of the Status Register, not the TA bit as in the non-chaining mode. Since the TTA bit is only set upon transmission of a packet (not by RESET), and since the TTA bit may easily be reset by issuing a "Clear Transmit Interrupt" command, there is no need to use the TA bit of the Interrupt Mask Register to mask interrupts generated by the TTA bit of the Status Register.

In Command Chaining mode, the "Disable Transmitter" command will cancel the oldest transmission. This permits canceling a packet destined for a node not ready to receive. If both packets should be canceled, two "Disable Transmitter" commands should be issued.

6.7.2 Receive Command Chaining

Like the Transmit Command Chaining operation, the processor can issue two consecutive "Enable Receive from Page fnn" commands.

After the first packet is received into the first specified page, the TRI bit of the Status Register will be set to logic "1", causing an interrupt. Again, the interrupt need not be serviced immediately. Typically, the interrupt service routine will read the Status Register. At this point, the RI bit will be found to be a logic "1". After reading the Status Register, the "Clear Receive Interrupt" command should be issued, thus resetting the TRI bit and clearing the interrupt. Note that only the "Clear Receive Interrupt" command will clear the TRI bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the receive operation is double buffered in order to retain the results of the first reception for analysis by the processor, therefore the information will remain in the Status Register until the "Clear Receive Interrupt" command is issued. Note that the interrupt will remain active until the "Clear Receive Interrupt" command is issued, and the second interrupt will be stored until the first interrupt is acknowledged. A minimum of 200nS (at EF=1) interrupt inactive time interval between interrupts is guaranteed.

The second reception will occur as soon as a second packet is sent to the node, as long as the second "Enable Receive to Page fnn" command was issued. The operation is as if a new "Enable Receive to Page fnn" command has just been issued. After the first Receive status bits are cleared, the Status Register will again be updated with the results of the second reception and a second interrupt resulting from the second reception will occur.

In the COM20022I, the Receive Inhibit (RI) bit of the Interrupt Mask Register now masks only the TRI bit of the Status Register, not the RI bit as in the non-chaining mode. Since the TRI bit is only set upon

reception of a packet (not by RESET), and since the TRI bit may easily be reset by issuing a "Clear Receive Interrupt" command, there is no need to use the RI bit of the Interrupt Mask Register to mask interrupts generated by the TRI bit of the Status Register. In Command Chaining mode, the "Disable Receiver" command will cancel the oldest reception, unless the reception has already begun. If both receptions should be canceled, two "Disable Receiver" commands should be issued.

6.8 Reset Details

6.8.1 Internal Reset Logic

The COM20022I includes special reset circuitry to guarantee smooth operation during reset. Special care is taken to assure proper operation in a variety of systems and modes of operation. The COM20022I contains digital filter circuitry and a Schmitt Trigger on the nRESET signal to reject glitches in order to ensure fault-free operation.

The COM20022I supports two reset options; software and hardware reset. A software reset is generated when a logic "1" is written to bit 7 of the Configuration Register. The device remains in reset as long as this bit is set. The software reset does not affect the microcontroller interface modes determined after hardware reset, nor does it affect the contents of the Address Pointer Registers, the Configuration Register, or the Setup1 Register. A hardware reset occurs when a low signal is asserted on the nRESET input. The minimum reset pulse width is $5T_{XTL}$. This pulse width is used by the internal digital filter, which filters short glitches to allow only valid resets to occur.

Upon reset, the transmitter portion of the device is disabled and the internal registers assume those states outlined in the Internal Registers section. After the nRESET signal is removed the user may write to the internal registers. Since writing a non-zero value to the Node ID Register wakes up the COM20022I core, the Setup1 Register should be written before the Node ID Register. Once the Node ID Register is written to, the COM20022I reads the value and executes two write cycles to the RAM buffer. Address 0 is written with the data D1H and address 1 is written with the Node ID. The data pattern D1H was chosen arbitrarily, and is meant to provide assurance of proper microsequencer operation.

6.9 Initialization Sequence

6.9.1 Bus Determination

Writing to and reading from an odd address location from the COM20022I's address space causes the COM20022I to determine the appropriate bus interface. When the COM20022I is powered on the internal registers may be written to. Since writing a non-zero value to the Node ID Register wakes up the core, the Setup1 Register should be written to before the Node ID Register. Until a non-zero value is placed into the NID Register, no microcode is executed, no tokens are passed by this node, and no reconfigurations are generated by this node. Once a non-zero value is placed in the register, the core wakes up, but the node will not attempt to join the network until the TX Enable bit of the Configuration Register is set.

Before setting the TX Enable bit, the software may make some determinations. The software may first observe the Receive Activity and the Token Seen bits of the Diagnostic Status Register to verify the health of the receiver and the network.

Next, the uniqueness of the Node ID value placed in the Node ID Register is determined. The TX Enable bit should still be a logic "0" until it is ensured that the Node ID is unique. If this node ID already exists, the Duplicate ID bit of the Diagnostic Status Register is set after a maximum of 210mS (or 420mS if the ET1 and ET2 bits are other than 1,1). To determine if another node on the network already has this ID, the COM20022I compares the value in the Node ID Register with the DID's of the token, and determines whether there is a response to it. Once the Diagnostic Status Register is read, the DUPID bit is cleared.

The user may then attempt a new ID value, wait 210mS before checking the Duplicate ID bit, and repeat the process until a unique Node ID is found. At this point, the TX Enable bit may be set to allow the node to join the network. Once the node joins the network, a reconfiguration occurs, as usual, thus setting the MYRECON bit of the Diagnostic Status Register.

The Tentative ID Register may be used to build a network map of all the nodes on the network, even once the COM20022I has joined the network. Once a value is placed in the Tentative ID Register, the COM20022I looks for a response to a token whose DID matches the Tentative ID Register. The software can record this information and continue placing Tentative ID values into the register to continue building the network map. A complete network map is only valid until nodes are added to or deleted from the network. Note that a node cannot detect the existence of the next logical node on the network when using the Tentative ID. To determine the next logical node, the software should read the Next ID Register.

6.10 Improved Diagnostics

The COM20022I allows the user to better manage the operation of the network through the use of the internal Diagnostic Status Register.

A high level on the My Reconfiguration (MYRECON) bit indicates that the Token Reception Timer of this node expired, causing a reconfiguration by this node. After the Reconfiguration (RECON) bit of the Status Register interrupts the microcontroller, the interrupt service routine will typically read the MYRECON bit of the Diagnostic Status Register. Reading the Diagnostic Status Register resets the MYRECON bit. Successive occurrences of a logic "1" on the MYRECON bit indicates that a problem exists with this node. At that point, the transmitter should be disabled so that the entire network is not held down while the node is being evaluated.

The Duplicate ID (DUPID) bit is used before the node joins the network to ensure that another node with the same ID does not exist on the network. Once it is determined that the ID in the Node ID Register is unique, the software should write a logic "1" to bit 5 of the Configuration Register to enable the basic transmit function. This allows the node to join the network.

The Receive Activity (RCVACT) bit of the Diagnostic Status Register will be set to a logic "1" whenever activity (logic "1") is detected on the RXIN pin.

The Token Seen (TOKEN) bit is set to a logic "1" whenever any token has been seen on the network (except those tokens transmitted by this node).

The RCVACT and TOKEN bits may help the user to troubleshoot the network or the node. If unusual events are occurring on the network, the user may find it valuable to use the TXEN bit of the Configuration Register to qualify events. Different combinations of the RCVACT, TOKEN, and TXEN bits, as shown indicate different situations:

6.10.1 Normal Results:

RCVACT=1, TOKEN=1, TXEN=0: The node is not part of the network. The network is operating properly without this node.

RCVACT=1, TOKEN=1, TXEN=1: The node sees receive activity and sees the token. The basic transmit function is enabled. Network and node are operating properly.

MYRECON=0, DUPID=0, RCVACT=1, TXEN=0, TOKEN=1: Single node network.

6.10.2 Abnormal Results:

RCVACT=1, TOKEN=0, TXEN=X: The node sees receive activity, but does not see the token. Either no other nodes exist on the network, some type of data corruption exists, the media driver is malfunctioning, the topology is set up incorrectly, there is noise on the network, or a reconfiguration is occurring.

RCVACT=0, TOKEN=0, TXEN=1: No receive activity is seen and the basic transmit function is enabled. The transmitter and/or receiver are not functioning properly.

RCVACT=0, TOKEN=0, TXEN=0: No receive activity and basic transmit function disabled. This node is not connected to the network.

The Excessive NAK (EXCNAK) bit is used to replace a timeout function traditionally implemented in software. This function is necessary to limit the number of times a sender issues a FBE to a node with no available buffer. When the destination node replies to 128 FBEs with 128 NAKs or 4 FBEs with 4 NAKs, the EXCNAK bit of the sender is set, generating an interrupt. At this point the software may abandon the transmission via the "Disable Transmitter" command. This sets the TA bit to logic "1" when the node next receives the token, to allow a different transmission to occur. The timeout value for the EXNACK bit (128 or 4) is determined by the FOUR-NAKS bit on the Setup1 Register.

The user may choose to wait for more NAK's before disabling the transmitter by taking advantage of the wraparound counter of the EXCNAK bit. When the EXCNAK bit goes high, indicating 128 or 4 NAKs, the "POR Clear Flags" command may be issued to reset the bit so that it will go high again after another count of 128 or 4. The software may count the number of times the EXCNAK bit goes high, and once the final count is reached, the "Disable Transmitter" command may be issued.

The New Next ID bit permits the software to detect the withdrawal or addition of nodes to the network.

The Tentative ID bit allows the user to build a network map of those nodes existing on the network. This feature is useful because it minimizes the need for human intervention. When a value placed in the Tentative ID Register matches the Node ID of another node on the network, the TENTID bit is set, telling the software that this NODE ID already exists on the network. The software should periodically place values in the Tentative ID Register and monitor the New Next ID bit to maintain an updated network map.

6.11 Oscillator

The COM20022I contains circuitry which, in conjunction with an external parallel resonant crystal or TTL clock, forms an oscillator.

If an external crystal is used, two capacitors are needed (one from each leg of the crystal to ground). No external resistor is required, since the COM20022I contains an internal resistor. The crystal must have an accuracy of 0.020% or better. The oscillation frequency range is from 10 MHz to 20 MHz.

The crystal must have an accuracy of 0.010% or better when the internal clock multiplier is turned on. The oscillation frequency must be 20MHz when the internal clock multiplier is turned on.

The XTAL2 side of the crystal may be loaded with a single 74HC-type buffer in order to generate a clock for other devices.

The user may attach an external TTL clock, rather than a crystal, to the XTAL1 signal. In this case, a 390Ω pull-up resistor is required on XTAL1, while XTAL2 should be left unconnected.

Chapter 7 Operational Description

7.1 Maximum Guaranteed Ratings*

Operating Temperature Range ..... *-40°C to +85°C*

Storage Temperature Range ..... -55°C to +150°C

Lead Temperature (soldering, 10 seconds) ..... +325 °C

Positive Voltage on any pin, with respect to ground ..... V_{DD}+0.3V

Negative Voltage on any pin, with respect to ground ..... -0.3V

Maximum V_{DD} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

7.2 DC Electrical Characteristics

V_{DD}=5.0V±10%

COM20022I: T_A=0°C to +70°C, COM20022II: T_A=-40°C to +85°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Low Input Voltage 1 (All inputs except A2, XTAL1, nRESET, nRD, nWR, nREFEX and RXIN)	V_{IL1}			0.8	V	TTL Levels
High Input Voltage 1 (All inputs except A2, XTAL1, nRESET, nRD, nWR, nREFEX and RXIN)	V_{IH1}	2.0			V	TTL Levels
Low Input Voltage 2 (XTAL1)	V_{IL2}			1.0	V	TTL Clock Input
High Input Voltage 2 (XTAL1)	V_{IH2}	4.0			V	

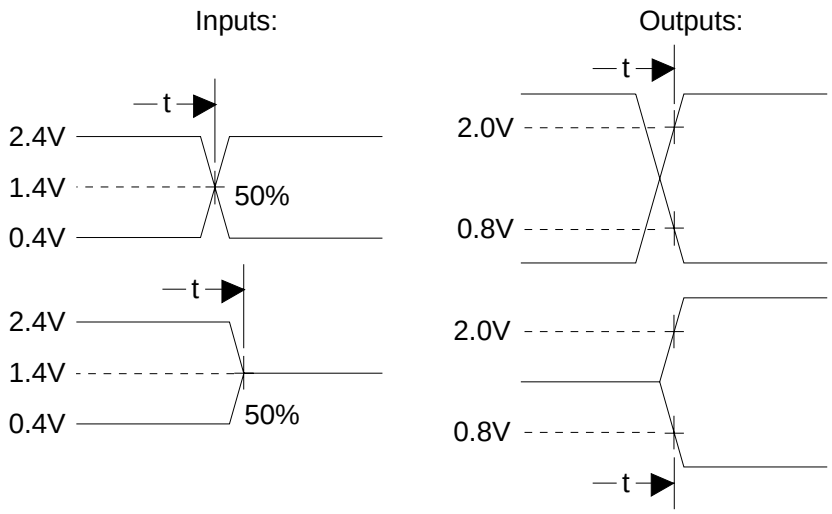
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Low to High Threshold Input Voltage (A2, nRESET, nRD, nWR, nREFEX and RXIN)	V_{ILH}		1.8		V	Schmitt Trigger, All Values at V_{DD} = 5V
High to Low Threshold Input Voltage (A2, nRESET, nRD, nWR, nREFEX and RXIN)	V_{IHL}		1.2		V	
Low Output Voltage 1 (nPULSE1 in Push/Pull Mode, nPULSE2, nTXEN, DREQ, nIOCS16)	V_{OL1}			0.4	V	I_{SINK}=4mA
High Output Voltage 1 (nPULSE1 in Push/Pull Mode, nPULSE2, nTXEN, DREQ, nIOCS16)	V_{OH1} V_{OH1C}	2.4 0.8 x V_{DD}			V	I_{SOURCE}=-2mA I_{SOURCE}=-200µA (except DREQ, nIOCS16)
Low Output Voltage 2 (D0-D15)	V_{OL2}			0.4	V	I_{SINK}=16mA
High Output Voltage 2 (D0-D15)	V_{OH2}	2.4			V	I_{SOURCE}=-12mA
Low Output Voltage 3 (nINTR)	V_{OL3}			0.8	V	I_{SINK}=24mA
High Output Voltage 3 (nINTR)	V_{OH3}	2.4			V	I_{SOURCE}=-10mA
Low Output Voltage 4 (nPULSE1 in Open-Drain Mode)	V_{OL4}			0.5	V	I_{SINK}=48mA Open Drain Driver
Dynamic V_{DD} Supply Current	I_{DD1} I_{DD2}		45 65		mA mA	5 Mbps 10 Mbps All Outputs Open
Input Pull-up Current (nPULSE1 in Open-Drain Mode, A1, AD0-AD2, D3-D15, nREFEX, (nDACK and TC in BUSTMG = H))	I_P		80	200	µA	V_{IN}=0.0V
Input Leakage Current (All inputs except A1, AD0-AD2, D3-D15, XTAL1, XTAL2, nREFEX, (nDACK and TC in BUSTMG = H))	I_L			±10	µA	$V_{SS} < V_{IN} < V_{DD}$

CAPACITANCE (T_A = 25 C; f_C = 1MHz; V_{DD} = 0V)

Output and I/O pins capacitive load specified as follows:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Input Capacitance	C_{IN}			5.0	pF	
Output Capacitance 1 (All outputs except XTAL2, nPULSE1 in Push/Pull Mode)	C_{OUT1}			45	pF	Maximum Capacitive Load which can be supported by each output.
Output Capacitance 2 (nPULSE1, in BackPlane Mode Only - Open Drain)	C_{OUT2}			400	pF	

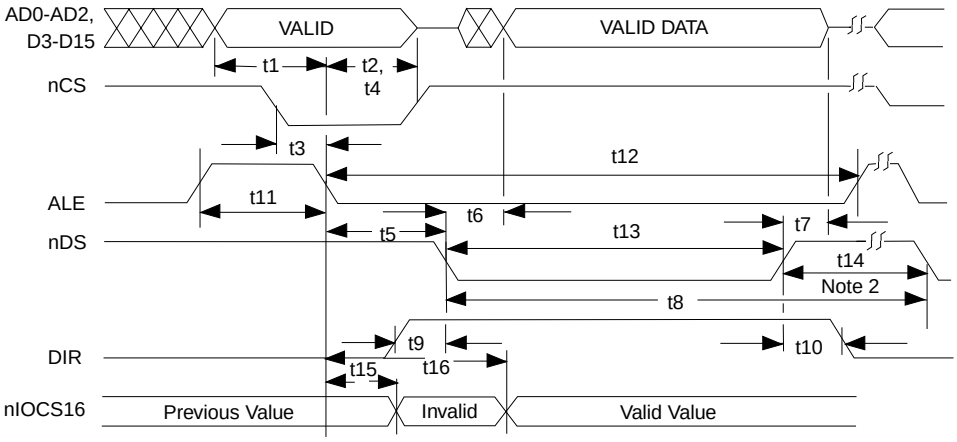
AC Measurements are taken at the following points:



Inputs are driven at 2.4V for logic "1" and 0.4 V for logic "0" except XTAL1 pin.

Outputs are measured at 2.0V min. for logic "1" and 0.8V max. for logic "0".

Chapter 8 Timing Diagrams



MUST BE: BUSTMG pin = HIGH and RBUSTMG bit = 0

	Parameter	min	max	units
t1	Address Setup to ALE Low	20		nS
t2	Address Hold from ALE Low	10		nS
t3	nCS Setup to ALE Low	10		nS
t4	nCS Hold from ALE Low	10		nS
t5	ALE Low to nDS Low	15		nS
t6	nDS Low to Valid Data		40	nS
t7	nDS High to Data High Impedance	0	20	nS
t8	Cycle Time (nDS Low to Next Time Low)	$4T_{ARB}$*		nS
t9	DIR Setup to nDS Active	10		nS
t10	DIR Hold from nDS Inactive	10		nS
t11	ALE High Width	20		nS
t12	ALE Low Width	20		nS
t13	nDS Low Width	60		nS
t14	nDS High Width	20		nS
t15	nIOCS16 Hold Delay from ALE Low	0		nS
t16	nIOCS16 Output Delay from ALE Low		40	nS

* T_{ARB} is the Arbitration Clock Period

T_{ARB} is identical to T_{opr} if SLOW ARB = 0

T_{ARB} is twice T_{opr} if SLOW ARB = 1

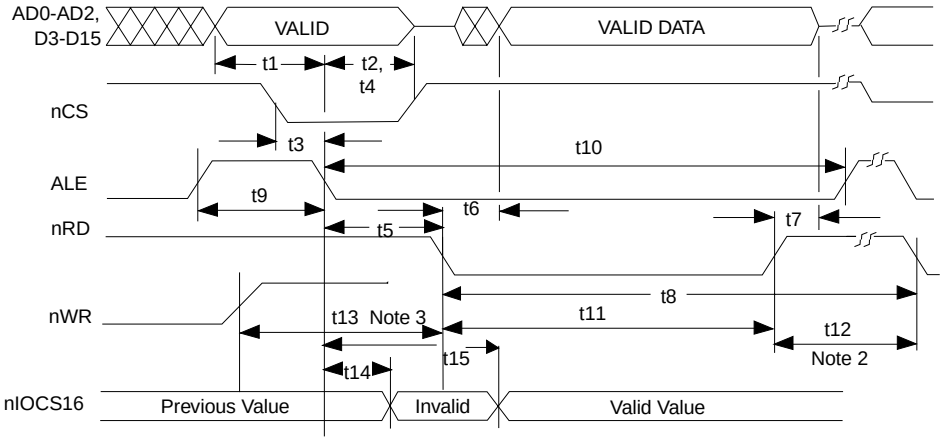
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.1 - Multiplexed Bus, 68XX-Like Control Signals; Read Cycle



MUST BE: BUSTMG pin = HIGH and RBUSTMG bit = 0

	Parameter	min	max	units
t1	Address Setup to ALE Low	20		nS
t2	Address Hold from ALE Low	10		nS
t3	nCS Setup to ALE Low	10		nS
t4	nCS Hold from ALE Low	10		nS
t5	ALE Low to nRD Low	15		nS
t6	nRD Low to Valid Data		40	nS
t7	nRD High to Data High Impedance	0	20	nS
t8	Cycle Time (nRD Low to Next Time Low)	$4T_{ARB}$*		nS
t9	ALE High Width	20		nS
t10	ALE Low Width	20		nS
t11	nRD Low Width	60		nS
t12	nRD High Width	20		nS
t13	nWR ↘ to nRD Low	20		nS
t14	nIOCS16 Hold Delay from ALE Low	0		nS
t15	nIOCS16 Output Delay from ALE Low		40	nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

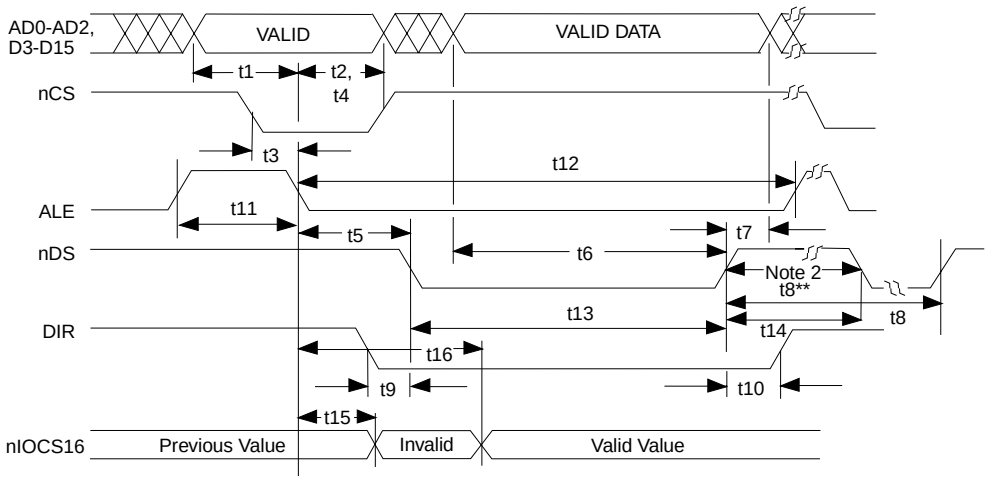
Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after a read from Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nRD to the leading edge of the next nRD.

Note 3: Read cycle for Address Pointer Low/High Registers occurring after a write to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nWR to the leading edge of nRD.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.2 - Multiplexed Bus, 80XX-Like Control Signals; Read Cycle



MUST BE: BUSTMG pin = HIGH

	Parameter	min	max	units
t1	Address Setup to ALE Low	20		nS
t2	Address Hold from ALE Low	10		nS
t3	nCS Setup to ALE Low	10		nS
t4	nCS Hold from ALE Low	10		nS
t5	ALE Low to nDS Low	15		nS
t6	Valid Data Setup to nDS High	30		nS
t7	Data Hold from nDS High	10		nS
t8	Cycle Time (nDS↓ to Next ↓)**	$4T_{ARB}$*		nS
t9	DIR Setup to nDS Active	10		nS
t10	DIR Hold from nDS Inactive	10		nS
t11	ALE High Width	20		nS
t12	ALE Low Width	20		nS
t13	nDS Low Width	20		nS
t14	nDS High Width	20		nS
t15	nIOCS16 Hold Delay from ALE Low	0		nS
t16	nIOCS16 Output Delay from ALE Low		40	nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

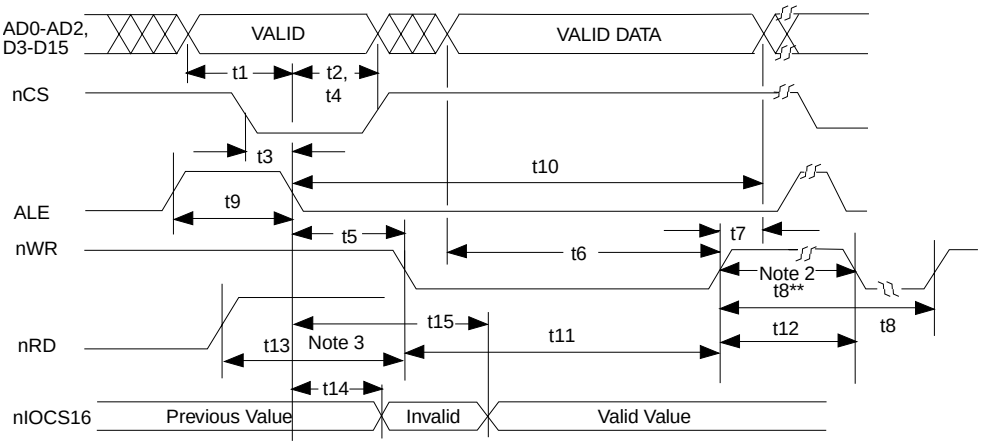
Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

** Note 2: Any cycle occurring after a write to Address Pointer Low Register requires a minimum of $4T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Write cycle for Address Pointer Low Register occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.3 - Multiplexed Bus, 68XX-Like Control Signals Write Cycle



MUST BE: BUSTMG pin = HIGH

	Parameter	min	max	units
t1	Address Setup to ALE Low	20		nS
t2	Address Hold from ALE Low	10		nS
t3	nCS Setup to ALE Low	10		nS
t4	nCS Hold from ALE Low	10		nS
t5	ALE Low to nDS Low	15		nS
t6	Valid Data Setup to nDS High	30		nS
t7	Data Hold from nDS High	10		nS
t8	Cycle Time (nWR↗ to Next ↗)**	$4T_{ARB}$*		nS
t9	ALE High Width	20		nS
t10	ALE Low Width	20		nS
t11	nWR Low Width	20		nS
t12	nWR High Width	20		nS
t13	nRD↗ to nWR Low	20		nS
t14	nIOCS16 Hold Delay from ALE Low	0		nS
t15	nIOCS16 Output Delay from ALE Low		40	nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

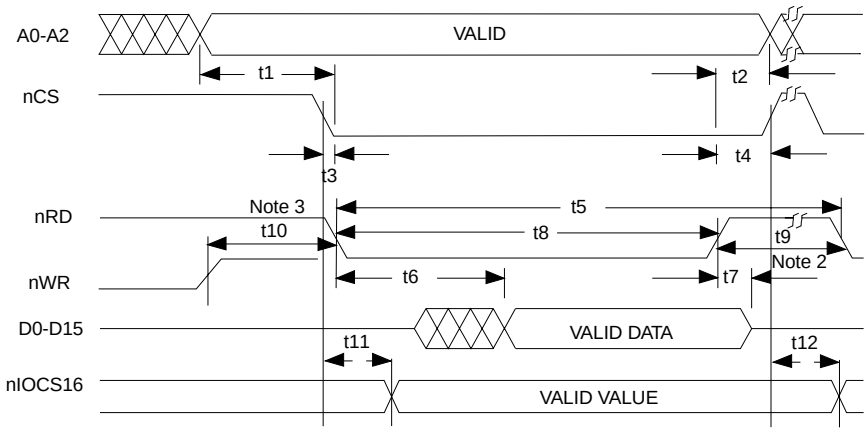
Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

** Note 2: Any cycle occurring after a write to Address Pointer Low Register requires a minimum of $4T_{ARB}$ from the trailing edge of nWR to the leading edge of the next nWR.
Write cycle for Address Pointer Low Register occurring after a write to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nWR to the leading edge of the next nWR.

Note 3: Write cycle for Address Pointer Low Register occurring after a read from Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nRD to the leading edge of nWR.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.4 - Multiplexed Bus, 80XX-Like Control Signals; Write Cycle



CASE 1: BUSTMG pin = HIGH and RBUSTMG bit = 0

	Parameter	min	max	units
t1	Address Setup to nRD Active	15		nS
t2	Address Hold from nRD Inactive	10		nS
t3	nCS Setup to nRD Active	5**		nS
t4	nCS Hold from nRD Inactive	0		nS
t5	Cycle Time (nRD Low to Next Time Low)	4T_{ARB}*		nS
t6	nRD Low to Valid Data		40**	nS
t7	nRD High to Data High Impedance	0	20	nS
t8	nRD Low Width	60		nS
t9	nRD High Width	20		nS
t10	nWR ↗ to nRD Low	20		nS
t11	nIOCS16 Output Delay from nCS Low		40***	nS
t12	nIOCS16 Hold Delay from nCS High	0****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

** nCS may become active *after* control becomes active, but the access time (t6) will now be 45nS measured from the leading edge of nCS.

*** t11 is measured from the latest active (valid) timing among nCS, A0-A2.

**** t12 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

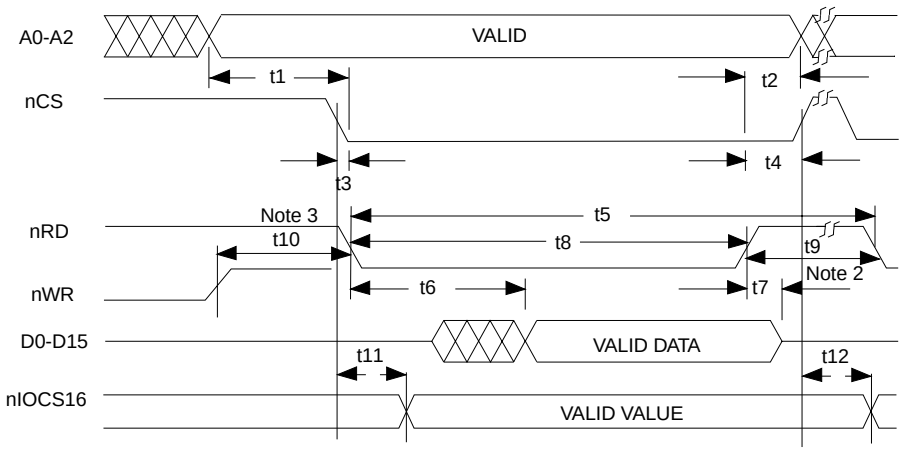
Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after a read from Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nRD to the leading edge of the next nRD.

Note 3: Read cycle for Address Pointer Low/High Registers occurring after a write to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nWR to the leading edge of nRD.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.5 - Non-Multiplexed Bus, 80XX-Like Control Signals; Read Cycle



CASE 2: BUSTMG pin = LOW or RBUSTMG bit = 1

	Parameter	min	max	units
t1	Address Setup to nRD Active	-5		nS
t2	Address Hold from nRD Inactive	0		nS
t3	nCS Setup to nRD Active	-5		nS
t4	nCS Hold from nRD Inactive	0		nS
t5	Cycle Time (nRD Low to Next Time Low)	$4T_{ARB}$*+30		nS
t6	nRD Low to Valid Data		60**	nS
t7	nRD High to Data High Impedance	0	20	nS
t8	nRD Low Width	100		nS
t9	nRD High Width	30		nS
t10	nWR ↓ to nRD Low	20		nS
t11	nIOCS16 Output Delay from nCS Low		40***	nS
t12	nIOCS16 Hold Delay from nCS High	0****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

** t6 is measured from the latest active (valid) timing among nCS, nRD, A0-A2.

*** t11 is measured from the latest active (valid) timing among nCS, A0-A2.

**** t12 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

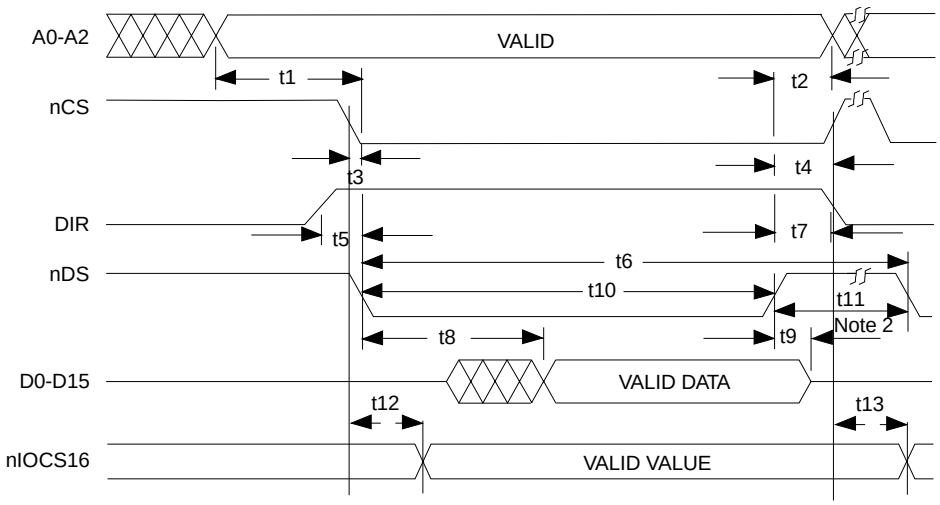
Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after a read from Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nRD to the leading edge of the next nRD.

Note 3: Read cycle for Address Pointer Low/High Registers occurring after a write to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nWR to the leading edge of nRD.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.6 - Non-Multiplexed Bus, 80XX-Like Control Signals; Read Cycle



CASE 1: BUSTMG pin = HIGH and RBUSTMG bit = 0

	Parameter	min	max	units
t1	Address Setup to nDS Active	15		nS
t2	Address Hold from nDS Inactive	10		nS
t3	nCS Setup to nDS Active	5**		nS
t4	nCS Hold from nDS Inactive	0		nS
t5	DIR Setup to nDS Active	10		nS
t6	Cycle Time (nDS Low to Next Time Low)	$4T_{ARB}$*		nS
t7	DIR Hold from nDS Inactive	10		nS
t8	nDS Low to Valid Data		40**	nS
t9	nDS High to Data High Impedence	0	20	nS
t10	nDS Low Width	60		nS
t11	nDS High Width	20		nS
t12	nIOCS16 Output Delay from nCS Low		40***	nS
t13	nIOCS16 Hold Delay from nCS High	0****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

** nCS may become active *after* control becomes active, but the access time (t8) will now be 45nS measured from the leading edge of nCS.

*** t12 is measured from the latest active (valid) timing among nCS, A0-A2.

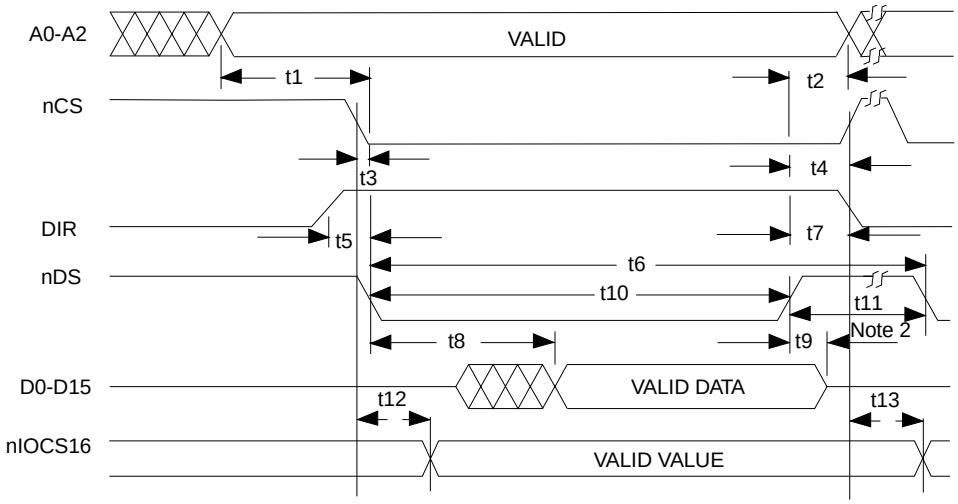
**** t13 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.7 - Non-Multiplexed Bus, 68XX-Like Control Signals; Read Cycle



CASE 2: BUSTMG pin = LOW or RBUSTMG bit = 1

	Parameter	min	max	units
t1	Address Setup to nDS Active	-5		nS
t2	Address Hold from nDS Inactive	0		nS
t3	nCS Setup to nDS Active	-5		nS
t4	nCS Hold from nDS Inactive	0		nS
t5	DIR Setup to nDS Active	10		nS
t6	Cycle Time (nDS Low to Next Time Low)	$4T_{ARB}$*+30		nS
t7	DIR Hold from nDS Inactive	10		nS
t8	nDS Low to Valid Data		60**	nS
t9	nDS High to Data High Impedence	0	20	nS
t10	nDS Low Width	100		nS
t11	nDS High Width	30		nS
t12	nIOCS16 Output Delay from nCS Low		40***	nS
t13	nIOCS16 Hold Delay from nCS High	0****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

** t8 is measured from the latest active (valid) timing among nCS, nDS, A0-A2.

*** t12 is measured from the latest active (valid) timing among nCS, A0-A2.

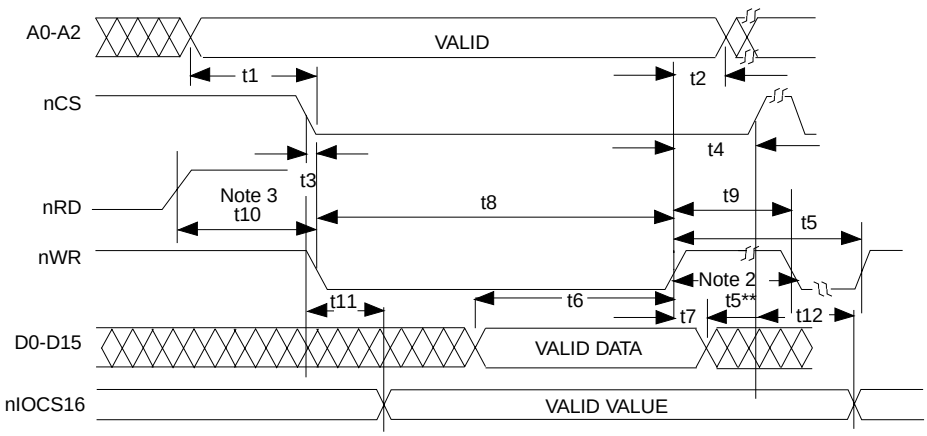
**** t13 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

Note 2: Read cycle for Address Pointer Low/High Registers occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.8 - Non-Multiplexed Bus, 68XX-Like Control Signals; Read Cycle



CASE 1: BUSTMG pin = HIGH

	Parameter	min	max	units
t1	Address Setup to nWR Active	15		nS
t2	Address Hold from nWR Inactive	10		nS
t3	nCS Setup to WR Active	5		nS
t4	nCS Hold from nWR Inactive	0		nS
t5	Cycle Time (nWR↗ to Next ↗)**	$4T_{ARB}$*		nS
t6	Valid Data Setup to nWR High	30***		nS
t7	Data Hold from nWR High	10		nS
t8	nWR Low Width	20		nS
t9	nWR High Width	20		nS
t10	nRD↗ to nWR Low	20		nS
t11	nIOCS16 Output Delay from nCS Low		40****	nS
t12	nIOCS16 Hold Delay from nCS High	0*****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

***: nCS may become active *after* control becomes active, but the data setup time will now be 30 nS measured from the later of nCS falling or Valid Data available.

**** t11 is measured from the latest active (valid) timing among nCS, A0-A2.

***** t12 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

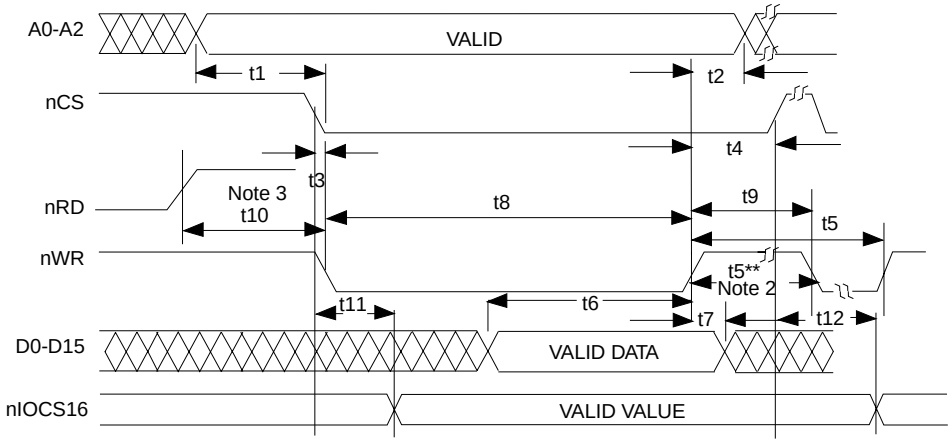
**Note 2: Any cycle occurring after a write to the Address Pointer Low Register requires a minimum of $4T_{ARB}$ from the trailing edge of nWR to the leading edge of the next nWR.

Write cycle for Address Pointer Low Register occurring after a write to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nWR to the leading edge of the next nWR.

Note 3: Write cycle for Address Pointer Low Register occurring after a read from Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nRD to the leading edge of nWR.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.9 - Non-Multiplexed Bus, 80XX-Like Control Signals; Write Cycle



CASE 2: BUSTMG pin = LOW

	Parameter	min	max	units
t1	Address Setup to nWR Active	0		nS
t2	Address Hold from nWR Inactive	0		nS
t3	nCS Setup to WR Active	0		nS
t4	nCS Hold from nWR Inactive	0		nS
t5	Cycle Time (nWR↓ to Next ↓)**	4T_{ARB}*		nS
t6	Valid Data Setup to nWR High	30		nS
t7	Data Hold from nWR High	10		nS
t8	nWR Low Width	65		nS
t9	nWR High Width	30		nS
t10	nRD↓ to nWR Low	20		nS
t11	nIOCS16 Output Delay from nCS Low		40****	nS
t12	nIOCS16 Hold Delay from nCS High	0*****		nS

* T_{ARB} is the Arbitration Clock Period

T_{ARB} is identical to T_{opr} if SLOW ARB = 0

T_{ARB} is twice T_{opr} if SLOW ARB = 1

T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

**** t11 is measured from the latest active (valid) timing among nCS, A0-A2.

***** t12 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

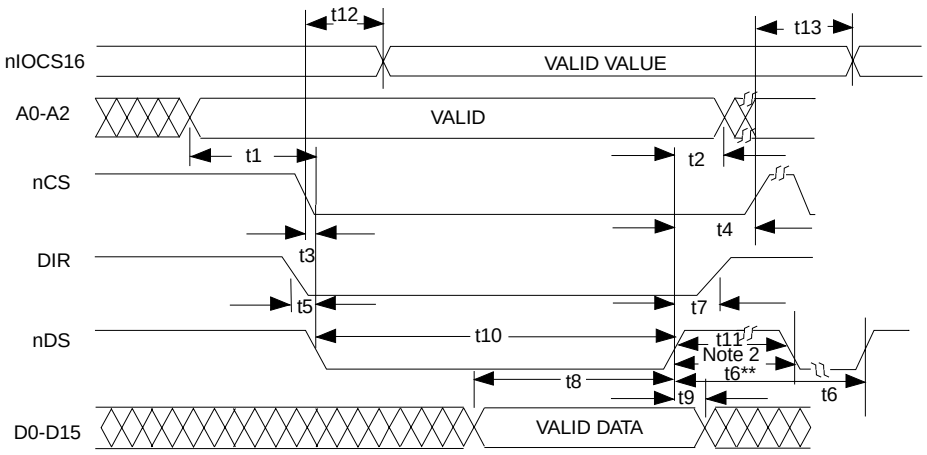
** Note 2: Any cycle occurring after a write to Address Pointer Low Register requires a minimum of 4T_{ARB} from the trailing edge of nWR to the leading edge of the next nWR.

Write cycle for Address Pointer Low Register occurring after a write to Data Register requires a minimum of 5T_{ARB} from the trailing edge of nWR to the leading edge of the next nWR.

Note 3: Write cycle for Address Pointer Low Register occurring after a read from Data Register requires a minimum of 5T_{ARB} from the trailing edge of nRD to the leading edge of nWR.

Notes 2 and 3 are applied to an access to Data Register by DMA transfer.

Figure 8.10 - Non-Multiplexed Bus, 80XX-Like Control Signals; Write Cycle



CASE 1: BUSTMG pin = HIGH

	Parameter	min	max	units
t1	Address Setup to nDS Active	15		nS
t2	Address Hold from nDS Inactive	10		nS
t3	nCS Setup to nDS Active	5		nS
t4	nCS Hold from nDS Inactive	0		nS
t5	DIR Setup to nDS Active	10		nS
t6	Cycle Time (nDS↓ to Next Time↓)**	$4T_{ARB}$*		nS
t7	DIR Hold from nDS Inactive	10		nS
t8	Valid Data Setup to nDS High	30***		nS
t9	Data Hold from nDS High	10		nS
t10	nDS Low Width	20		nS
t11	nDS High Width	20		nS
t12	nIOCS16 Output Delay from nCS Low		40****	nS
t13	nIOCS16 Hold Delay from nCS High	0*****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

***: nCS may become active *after* control becomes active, but the data setup time will now be 30 nS measured from the later of nCS falling or Valid Data available.

****: t12 is measured from the latest active (valid) timing among nCS, A0-A2.

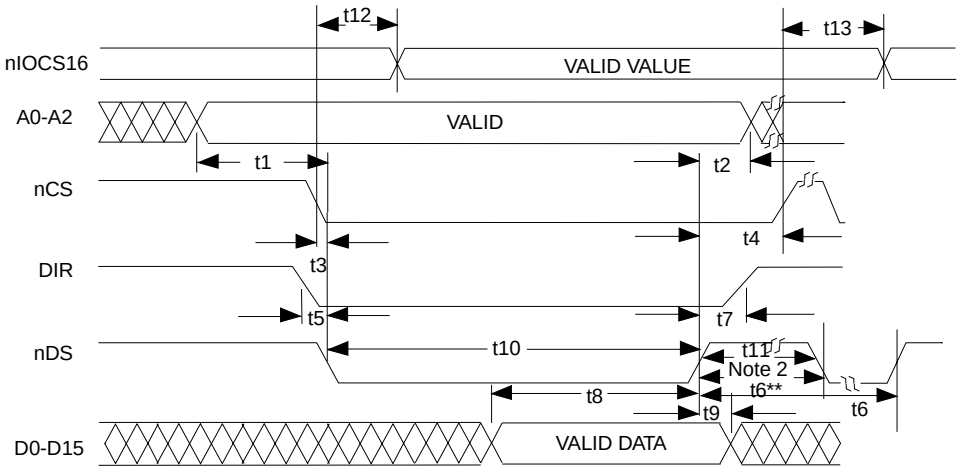
*****: t13 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

**Note 2: Any cycle occurring after a write to the Address Pointer Low Register requires a minimum of $4T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.
Write cycle for Address Pointer Low Registers occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.11 - Non-Multiplexed Bus, 68XX-Like Control Signals; Write Cycle



CASE 2: BUSTMG pin = LOW

	Parameter	min	max	units
t1	Address Setup to nDS Active	0		nS
t2	Address Hold from nDS Inactive	0		nS
t3	nCS Setup to nDS Active	0		nS
t4	nCS Hold from nDS Inactive	0		nS
t5	DIR Setup to nDS Active	10		nS
t6	Cycle Time (nDS↓ to Next ↓)**	$4T_{ARB}$*		nS
t7	DIR Hold from nDS Inactive	10		nS
t8	Valid Data Setup to nDS High	30		nS
t9	Data Hold from nDS High	10		nS
t10	nDS Low Width	65		nS
t11	nDS High Width	30		nS
t12	nIOCS16 Output Delay from nCS Low		40****	nS
t13	nIOCS16 Hold Delay from nCS High	0*****		nS

* T_{ARB} is the Arbitration Clock Period
T_{ARB} is identical to T_{opr} if SLOW ARB = 0
T_{ARB} is twice T_{opr} if SLOW ARB = 1
T_{opr} is the period of operation clock. It depends on CKUP1 and CKUP0 bits

**** t12 is measured from the latest active (valid) timing among nCS, A0-A2.

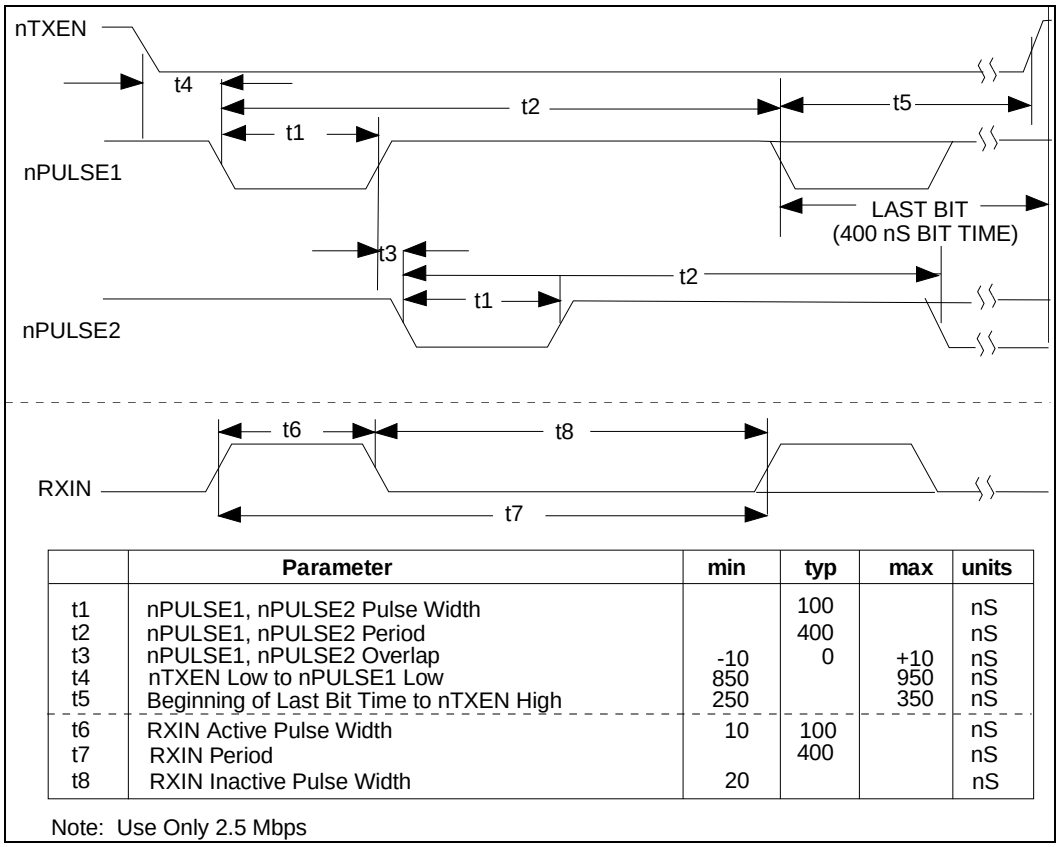
***** t13 is measured from the earliest inactive (invalid) timing among nCS, A0-A2.

Note 1: The Microcontroller typically accesses the COM20022 on every other cycle. Therefore, the cycle time specified in the microcontroller's datasheet should be doubled when considering back-to-back COM20022 cycles.

**Note 2: Any cycle occurring after a write to the Address Pointer Low Register requires a minimum of $4T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.
Write cycle for Address Pointer Low Register occurring after an access to Data Register requires a minimum of $5T_{ARB}$ from the trailing edge of nDS to the leading edge of the next nDS.

Note 2 is applied to an access to Data Register by DMA transfer.

Figure 8.12 - Non-Multiplexed Bus, 68XX-Like Control Signals; Write Cycle

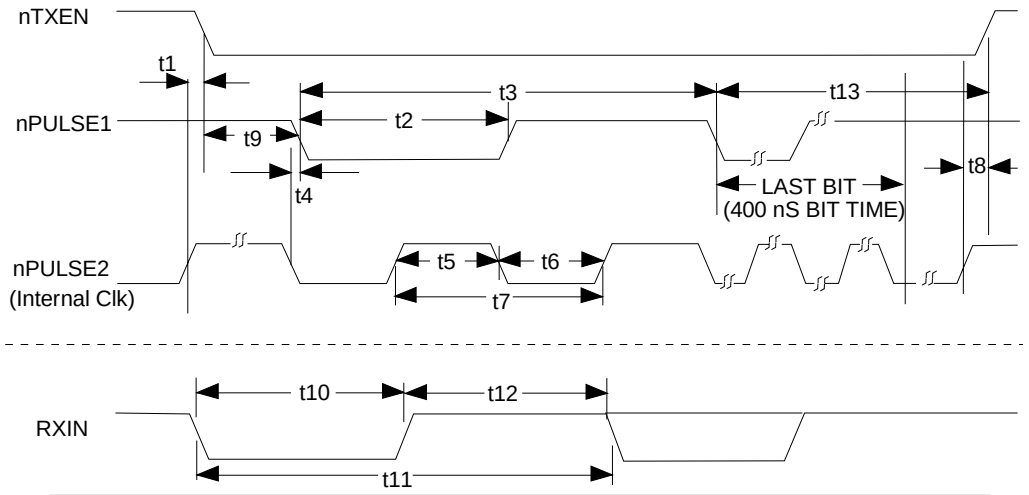


	Parameter	min	typ	max	units
t1	nPULSE1, nPULSE2 Pulse Width		100		nS
t2	nPULSE1, nPULSE2 Period		400		nS
t3	nPULSE1, nPULSE2 Overlap	-10	0	+10	nS
t4	nTXEN Low to nPULSE1 Low	850		950	nS
t5	Beginning of Last Bit Time to nTXEN High	250		350	nS
t6	RXIN Active Pulse Width	10	100		nS
t7	RXIN Period		400		nS
t8	RXIN Inactive Pulse Width	20			nS

Note: Use Only 2.5 Mbps

Figure 8.13 - Normal Mode Transmit or Receive Timing

(These signals are to and from the hybrid)



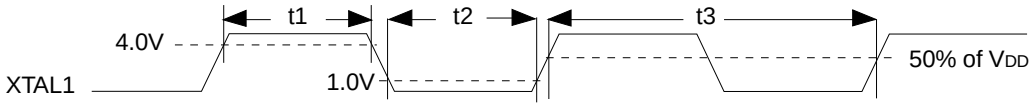
	Parameter	min	typ	max	units
t1	nPULSE2 High to nTXEN Low	-25		50	nS
t2	nPULSE1 Pulse Width		200*		nS
t3	nPULSE1 Period		400*		nS
t4	nPULSE2 Low to nPULSE1 Low	-25		50	nS
t5	nPULSE2 High Time		100*		nS
t6	nPULSE2 Low Time		100*		nS
t7	nPULSE2 Period		200*		nS
t8	nPULSE2 High to nTXEN High (First Rising Edge on nPULSE2 after Last Bit Time)	-25		50	nS
t9	nTXEN Low to first nPULSE1 Low**	650		750	nS
t13	Beginning Last Bit Time to nTXEN High**	450		550	nS
t10	RXIN Active Pulse Width	10	200*		nS
t11	RXIN Period		400*		nS
t12	RXIN Inactive Pulse Width	20			nS

Above values are for 2.5 Mbps.
Other Data Rates are shown below.

T_{DR} is the Data Rate Period
*t5, t6 = $T_{DR}/4$
*t2, t7, t10 = $T_{DR}/2$
*t3, t11 = T_{DR}
**t9 = $\frac{7}{4}$ x T_{DR} +/- 50 nS
**t13 = $\frac{5}{4}$ x T_{DR} +/- 50 nS

Figure 8.14 - Backplane Mode Transmit or Receive Timing

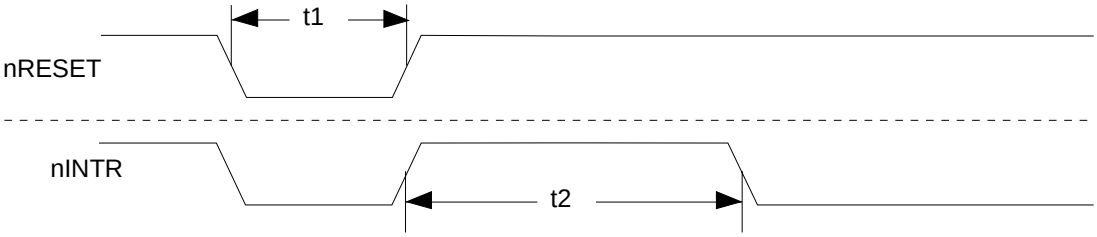
(These signals are to and from the differential driver or the cable)



	Parameter	min	typ	max	units
t1	Input Clock High Time	20			nS
t2	Input Clock Low Time	20			nS
t3	Input Clock Period*	50		100	nS
t4	Input Clock Frequency*	10		20	MHz
t5	Frequency Accuracy*	-200		200	ppm

Note*: Input clock frequency must be 20 MHz (±100ppm or better) to use the internal Clock Multiplier. t_4 and t_5 are applied to crystal oscillaton.

Figure 8.15 - TTL Input Timing on XTAL1 Pin



	Parameter		min	typ	max	units
t1	nRESET Pulse Width***		$5T_{XTL}$*			
t2	nINTR High to Next nINTR Low	EF = 0	T_{DR}**/2			
		EF = 1	$4T_{XTL}$*			

Note*: T_{XTL} is period of external XTAL oscillation frequency.
Note**: T_{DR} is period of Data Rate (i.e. at 2.5 Mbps, T_{DR} = 400 nS)
Note***: When the power is turned on, t1 is measured from stable XTAL oscillation after V_{DD} was over 4.5V.

Figure 8.16 - Reset and Interrupt Timing

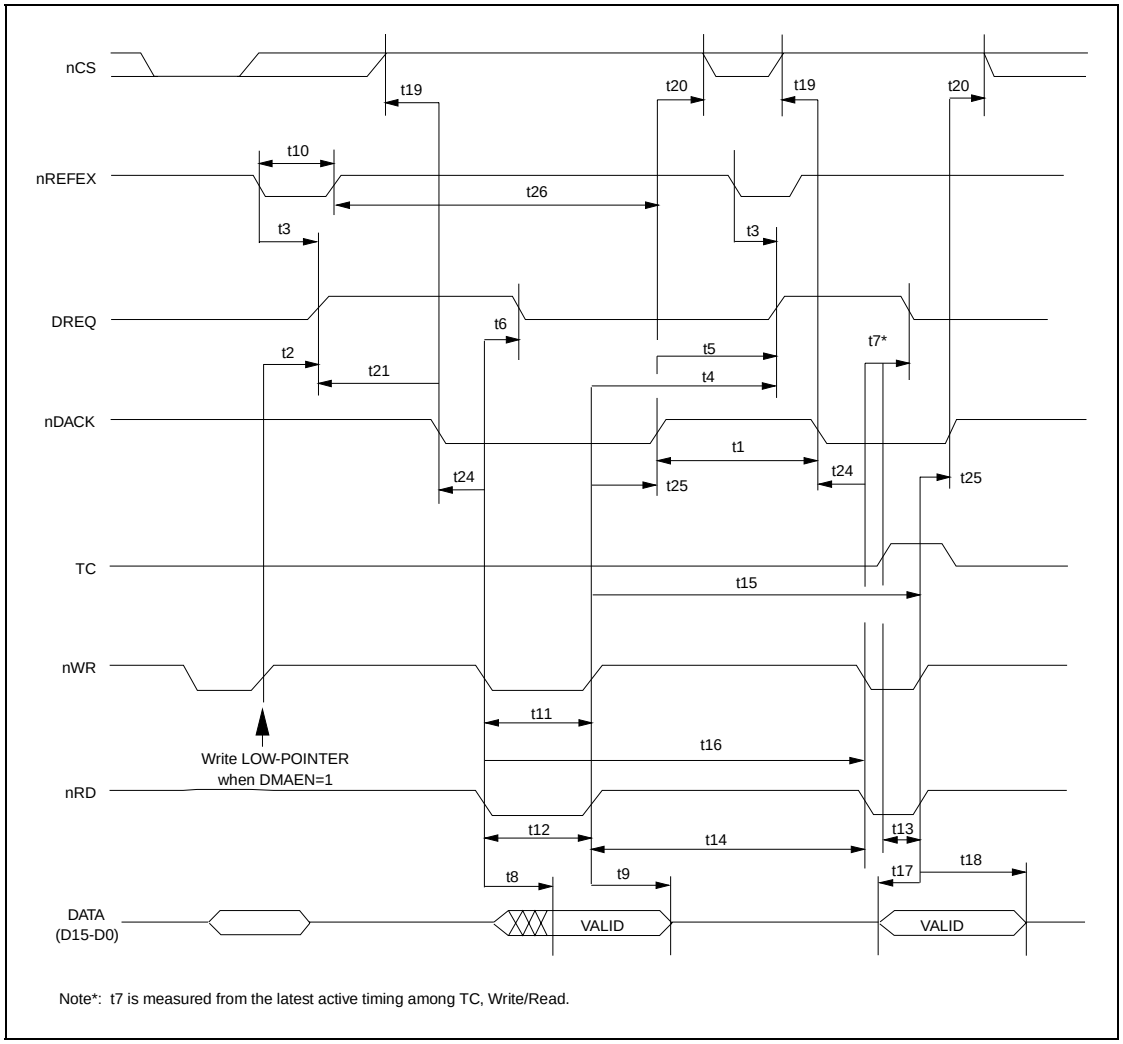


Figure 8.17 - DMA Timing (Intel Mode 80XX)

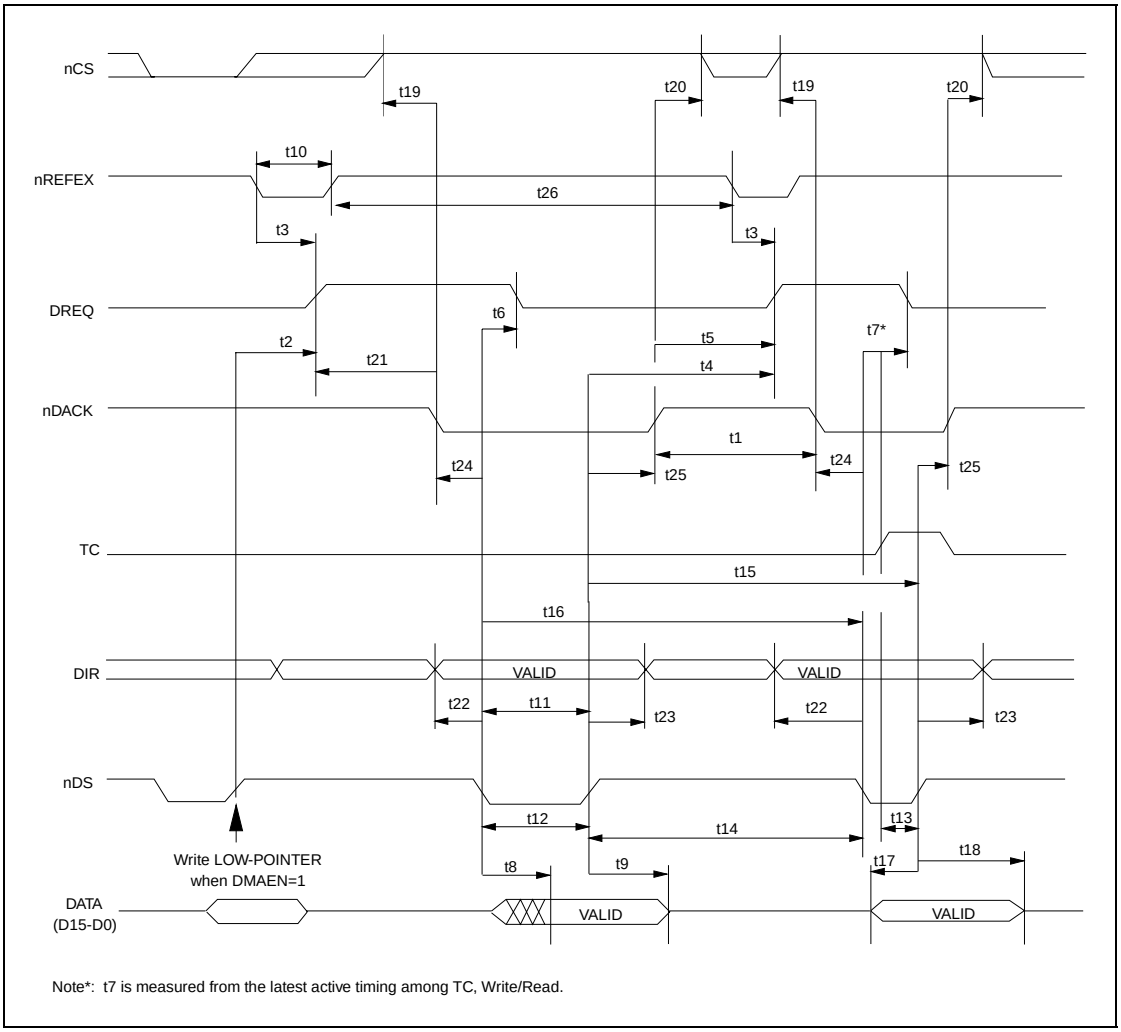


Figure 8.18 - DMA Timing (Motorola Mode 68XX)

Table 8.1 - DMA Timing

	PARAMETER		MIN	TYP	MAX	UNIT	NOTE
t1	nDACK Inactive Pulse Width				30	ns	
t2	The First DREQ Assertion Delay After Writing Low Pointer		4 Tarb	5 Tarb	5Tarb +40ns		Note 1
t3	DREQ Assert Delay from nREFEX Active at Programmable Burst Transfer Mode		0		40	ns	Note 3
t4	DREQ Assertion Delay from Write/Read Inactive at Non-Burst Transfer Mode		0		40	ns	Note 4
t5	DREQ Assertion Delay from nDACK Inactive due to Timeout of Gate Timer at Programmable Burst Transfer Mode	GTTM bit =0	7Txtl		8Txtl +40ns		Note 2
		GTTM bit=1	15Txtl		16Txtl +40ns		
t6	DREQ Negation Delay from Write/Read Active		0		40	ns	Note 4
t7	DREQ Negation Delay from TC and Write/Read Active		0		40	ns	Note 4
t8	Data Access Time from Read Active				40	ns	Note 4
t9	Data Float Delay from Read Inactive		0		20	ns	Note 4
t10	nREFEX Active Pulse Width		20			ns	
t11	Write Active Pulse Width	CASE 1W	20			ns	Note 4,5
		CASE 2W	65			ns	
t12	Read Active Pulse Width	CASE 1R	60			ns	Note 4,5
		CASE 2R	100			ns	
t13	Active Pulse Overlap Width between TC and Write/Read		20			ns	Note 4
t14	Write/Read Inactive Pulse Width	CASE1w/1R	20			ns	Note 4,5
		CASE2w/2R	30			ns	
t15	Write Cycle Interval Period		4Tarb				Note 1,4
t16	Read Cycle Interval Period	CASE1R	4Tarb				Note 1,4,5
		CASE2R	4Tarb+30nS				
t17	Data Setup to Write Inactive		30			ns	Note 4
t18	Data Hold From Write Inactive		10			ns	Note 4
t19	nCS High Setup to nDACK Active		20			ns	
t20	nCS High Hold from nDACK Inactive		20			ns	
t21	DREQ Active Setup to nDACK Active		20			ns	
t22	DIR Setup to nDS Low (Motorola mode only)		10			ns	
t23	DIR Hold from nDS High (Motorola mode only)		10			ns	
t24	nDACK Setup to Write/Read Active		30			ns	Note 4
t25	nDACK Hold After Write/Read Inactive		5			ns	Note 4
t26	nREFEX Inactive Time		3Txtl				Note 2

Notes:

1. Tarb is the ARBITRATION CLOCK PERIOD. It depends on Topr and SLOWARB bit.
   SLOWARB must set to “1” if the data rate is over 5 Mbps. (i.e. 10 Mbps)
   Tarb is Topr at SLOWARB=0 and Tarb is 2Topr at SLOWARB=1.
   Topr is the period of Operation Clock Frequency. It depends on the CKUP1 and CKUP0 bits.
2. Txtl is a period of external XTAL oscillation frequency.
3. The nREFEX pin must not be Low while nDACK is Low.

4. “Write” means write signal and “Read” means read signal. “Write/Read” means write or read signal.
   At INTEL MODE, write signal is nWR and read signal is nRD.
   At MOTOROLA MODE, write signal is nDS when DIR is Low and the read signal is nDS when DIR is High.
5. Conditions of CASE1W, CASE2W, CASE1R and CASE2R are shown below;
   CASE1W : BUSTMG pin = High
   CASE2W : BUSTMG pin = Low
   CASE1R : BUSTMG pin = High and RBUSTMG bit = 0
   CASE2R : BUSTMG pin = Low or RBUSTMG bit = 1

Chapter 9 Package Outline

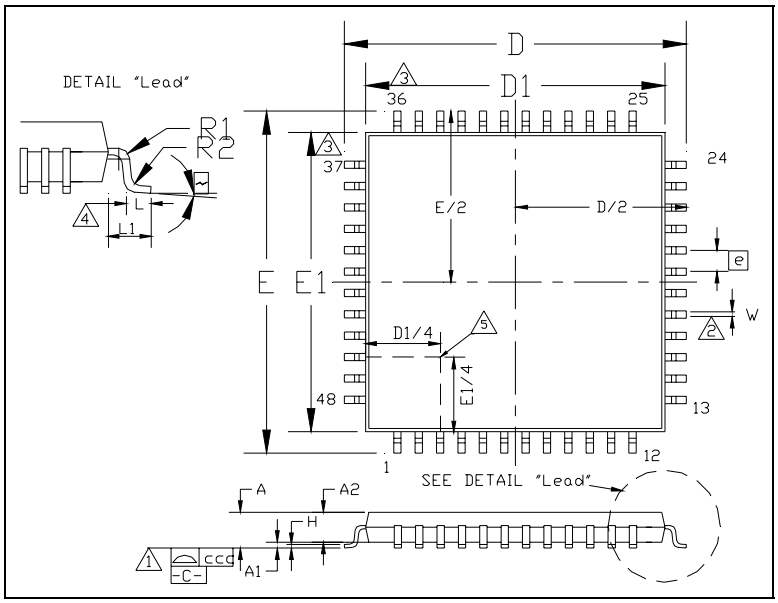


Figure 9.1 - COM20022I 48 Pin TQFP Package Outline

Table 9.1 - COM20022I 48 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.6	Overall Package Height
A1	0.05	0.10	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	8.80	9.00	9.20	X Span
D/2	4.40	4.50	4.60	$^1/_2$ X Span Measure from Centerline
D1	6.90	7.00	7.10	X body Size
E	8.80	9.00	9.10	Y Span
E/2	4.40	4.50	4.60	$^1/_2$ Y Span Measure from Centerline
E1	6.90	7.00	7.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.17	~	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity (Assemblers)
ccc	~	~	0.08	Coplanarity (Test House)

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 10 Appendix A

This appendix describes the function of the NOSYNC and EF bits.

10.1 NOSYNC Bit

The NOSYNC bit controls whether or not the RAM initialization sequence requires the line to be idle by enabling or disabling the SYNC command during initialization. It is defined as follows:

NOSYNC: Enable/Disable SYNC command during initialization. NOSYNC=0, Enable (Default): the line has to be idle for the RAM initialization sequence to be written, NOSYNC=1, Disable: the line does not have to be idle for the RAM initialization sequence to be written.

The following discussion describes the function of this bit:

During initialization, after the CPU writes the Node ID, the COM20022I will write "D1"h data to Address 000h and Node-ID to Address 001h of its internal RAM within 3uS. These values are read as part of the diagnostic test. If the D1 and Node-ID initialization sequence cannot be read, the initialization routine will report it as a device diagnostic failure. These writes are controlled by a micro-program which sometimes waits if the line is active; SYNC is the micro-program command that causes the wait. When the micro-program waits, the initial RAM write does not occur, which causes the diagnostic error. Thus in this case, if the line is not idle, the initialization sequence may not be written, which will be reported as a device diagnostic failure.

However, the initialization sequence and diagnostics of the COM20022I should be independent of the network status. This is accomplished through some additional logic to decode the program counter, enabled by the NOSYNC bit. When it finds that the micro-program is in the initialization routine, it disables the SYNC command. In this case, the initialization will not be held up by the line status.

Thus, by setting the NOSYNC bit, the line does not have to be idle for the RAM initialization sequence to be written.

10.2 EF Bit

The EF bit controls several modifications to internal operation timing and logic. It is defined as follows:

EF: Enable/Disable the new internal operation timing and logic refinements. EF=0: (Default) Disable the new internal operation timing (the timing is the same as in the COM20020 Rev. B); EF=1: Enable the new internal operation timing.

The EF bit controls the following timing/logic refinements in the COM20022I:

a) Extend Interrupt Disable Time

While the interrupt is active (nINTR pin=0), the interrupt is disabled by writing the Clear Tx/Rx interrupt and Clear Flag command and by reading the Next-ID register. This minimum disable time is changed by the Data Rate. For example, it is 200nS at 2.5Mbps and 50nS at 10Mbps. The 50nS width will be too short to for the Interrupt to be seen.

Setting the EF bit will change the minimum disable time to always be more than 200nS even if the Data Rate is 10Mbps . This is done by changing the clock which is supplied to the Interrupt Disable logic. The frequency of this clock is always 20MHz even if the data rate is 10Mbps.

b) Synchronize the Pre-Scalar Output

The Pre-Scalar is used to change the data rate. The output clock is selected by CKP3-1 bits in the Setup1 register. The CKP3-1 bits are changed by writing the Setup1 register from outside the CPU. It's not synchronized between the CPU and COM20022I. Thus, changing the CKP2-0 timing does not synchronize with the internal clocks of Pre-Scalar, and changing CKP2-0 may cause spike noise to appear on the output clock line.

Setting the EF bit will include flip-flops inserted between the Setup1 register and Pre-Scalar for synchronizing the CKP2-0 with Pre-Scalar's internal clocks.

Never change the CKP2-0 when the data rate is over 5 Mbps. They must all be zero.

c) Shorten The Write Interval Time To The Command Register

The COM20022I limits the write interval time for continuous writing to the Command register. The minimum interval time is changed by the Data Rate. It's 100 nS at the 2.5 Mbps and 1.6 μS at the 156.25 Kbps. This 1.6 μS is very long for CPU.

Setting the EF bit will change the clock source from OSCK clock (8 times frequency of data rate) to XTAL clock which is not changed by the data rate, such that the minimum interval time becomes 100 nS.

d) Eliminate The Write Prohibition Period For The Enable Tx/Rx Commands

The COM20022I has a write prohibition period for writing the Enable Transmit/Receive Commands. This period is started by the TA or RI bit (Status Reg.) returning to High. This prohibition period is caused by setting the TA/RI bit with an internal pulse signal. It is 3.2 μS at 156.25 Kbps. This period may be a problem when using interrupt processing. The interrupt occurs when the RI bit returns to High. The CPU writes the next Enable Receive Command to the other page immediately. In this case, the interval time between the interrupt and writing Command is shorter than 3.2 μS.

Setting the EF bit will cause the TA/RI bit to return to High upon release of the internal pulse signal for setting the TA/RI bit, instead of at the start of the pulse. This is illustrated in Figure 10.1 on the following page.

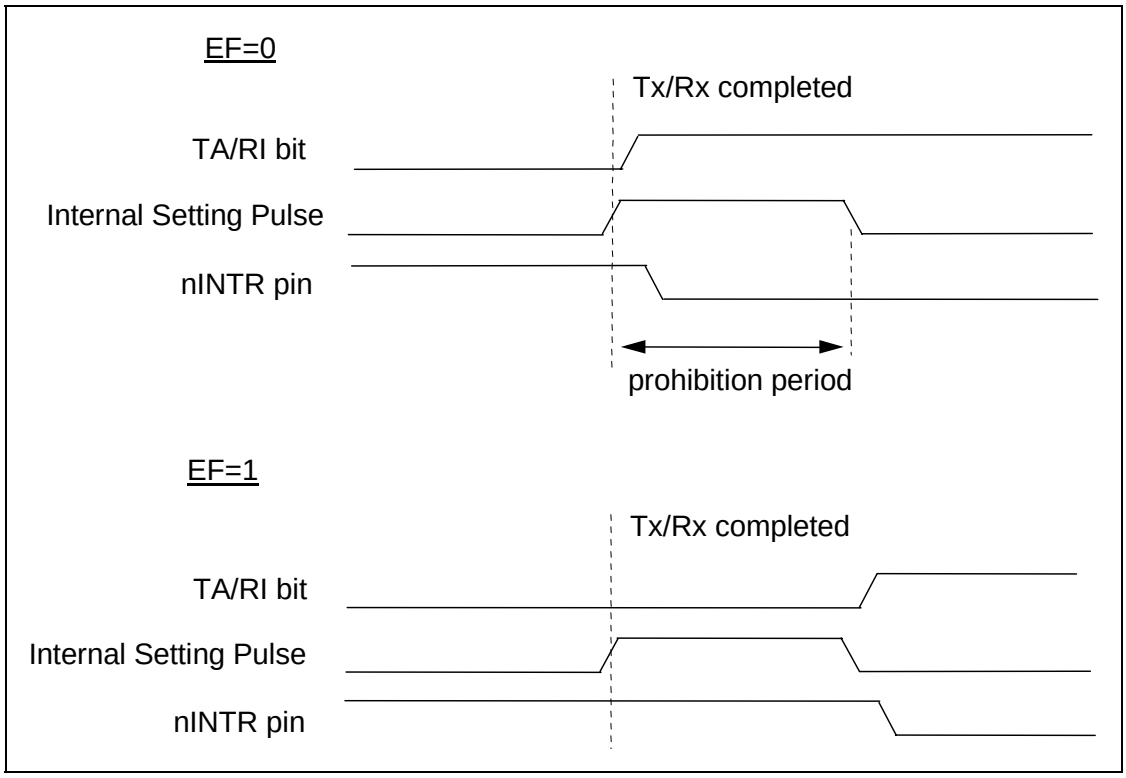


Figure 10.1 - Effect of the EF Bit on the TA/RI Bit

The EF bit also controls the resolution of the following issues from the COM20020 Rev B:

a) Network MAP Generation

Tentative ID is used for generating the Network MAP, but it sometimes detects a non-existent node. Every time the Tentative-ID register is written, the effect of the old Tentative-ID remains active for a while, which results in an incorrect network map. It can be avoided by a carefully coded software routine, but this requires the programmer to have deep knowledge of how the COM20022I works. Duplicate-ID is mainly used for generating the Network MAP. This has the same issue as Tentative-ID.

A minor logic change clears all the remaining effects of the old Tentative-ID and the old Duplicate-ID, when the COM20022I detects a write operation to Tentative-ID or Node-ID register. With this change, programmers can use the Tentative-ID or Duplicate-ID for generating the network MAP without any issues. This change is Enabled/Disabled by the EF bit.

b) Mask Register Reset

The Mask register is reset by a soft reset in the COM20020 Rev. A, but is not reset in Rev. B. The Mask register is related to the Status and Diagnostic register, so it should be reset by a soft reset. Otherwise, every time the soft reset happens, the COM20020 Rev. B generates an unnecessary interrupt since the status bits RI and TA are back to one by the soft reset.

This is resolved by changing the logic to reset the Mask register both by the hard reset and by the soft reset. The soft reset is activated by the Node-ID register going to 00h or by the RESET bit going to High in the Configuration register. This solution is Enabled/Disabled by the EF bit.

Chapter 11 Appendix B: Example of Interface Circuit Diagram to ISA Bus