LOW SKEW, 1-TO-4, CRYSTAL OSCILLATOR/LVCMOS-TO-3.3V LVPECL/LVCMOS FANOUT BUFFER

ICS8534I-13

General Description

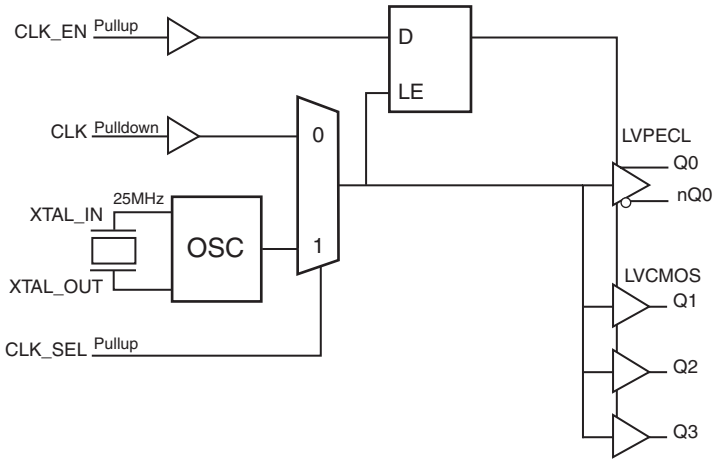
The ICS8534I-13 is a low skew, high performance 1-to-4 Crystal Oscillator/LVCMOS-to-3.3V LVPECL/LVCMOS fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8534I-13 has selectable single ended clock or crystal inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8534I-13 ideal for those applications demanding well defined performance and repeatability.

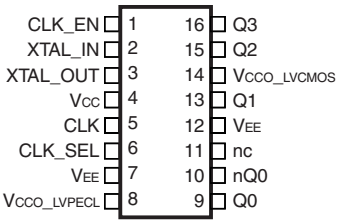
Features

- One differential 3.3V LVPECL outputs, and three single ended 2.5V LVCMOS outputs
- Selectable LVCMOS/LVTTL CLK or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Crystal frequency: 25MHz
- Maximum output frequency: 266MHz
- Output skew: 55ps (typical)
- Part-to-part skew: 800ps (typical)
- Propagation delay: 3.3ns (typical)
- Additive phase jitter, RMS: 0.16ps (typical)
- LVPECL output, 3.3V operating supply
  LVCMOS output, 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free RoHS 6) packages

Block Diagram



Pin Assignment



ICS8534I-13
16-Lead SOIC, 150MIL
3.9mm x 9.9mm x 1.375mm
package body
M Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ0 output is forced high. LVCMOS / LVTTL interface levels.
2, 3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
4	V_{CC}	Power		Positive supply pin.
5	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
6	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects XTAL inputs. When LOW, selects CLK input. LVCMOS / LVTTL interface levels.
7, 12	V_{EE}	Power		Negative supply pins.
8	V_{CCO_LVPECL}	Power		Output power supply mode for LVPECL clock outputs.
9, 10	Q0, nQ0	Output		Differential clock outputs. LVPECL interface levels.
11	nc	Unused		No connect.
13, 15, 16	Q1, Q2, Q3	Output		Single ended clock outputs. LVCMOS / LVTTL interface levels.
14	V_{CCO_LVCMOS}	Power		Output power supply mode for LVCMOS / LVTTL clock outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs		
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0**	**nQ0**	**Q1:Q3**
0	0	CLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW
0	1	XTAL_IN, XTAL_OUT	Disabled; LOW	Disabled; HIGH	Disabled; LOW
1	0	CLK	Enabled	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in *Figure* 1.
In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.

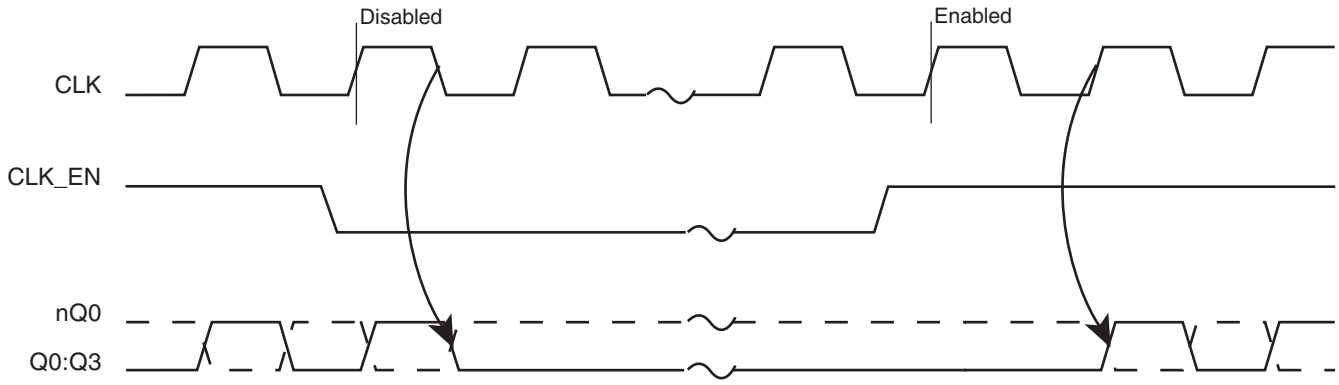


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs	Outputs		
CLK	**Q0**	**nQ0**	**Q1:Q3**
0	LOW	HIGH	LOW
1	HIGH	LOW	HIGH

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I (LVCMOS)	-0.5V to V_{CC} + 0.5 V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_LVCMOS} + 0.5V
Inputs, V_I (LVPECL)	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	90°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVPECL} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCO_LVPECL}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			60		mA
I_{CCO_LVPECL}	Power Supply Current			12		mA

Table 4B. LVCMOS Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CCO_LVCMOS}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			58		mA
I_{CCO_LVCMOS}	Power Supply Current			15		mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
V_{HYS}	Input Hysteresis	CLK_EN, CLK_SEL		100			mV
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
		CLK_EN, CLK_SEL	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN, CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVCMOS} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVCMOS} = 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVCMOS}/2. See Parameter Measurement Information Section. "LVCMOS Output Load Test circuit" diagram.

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V±5\%$, $V_{CCO\_LVPECL} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} - 2.0		V_{CCO_LVPECL} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1			1.65		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.16		ps
*t*sk(o)	Output Skew; NOTE 2, 4			55		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			800		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

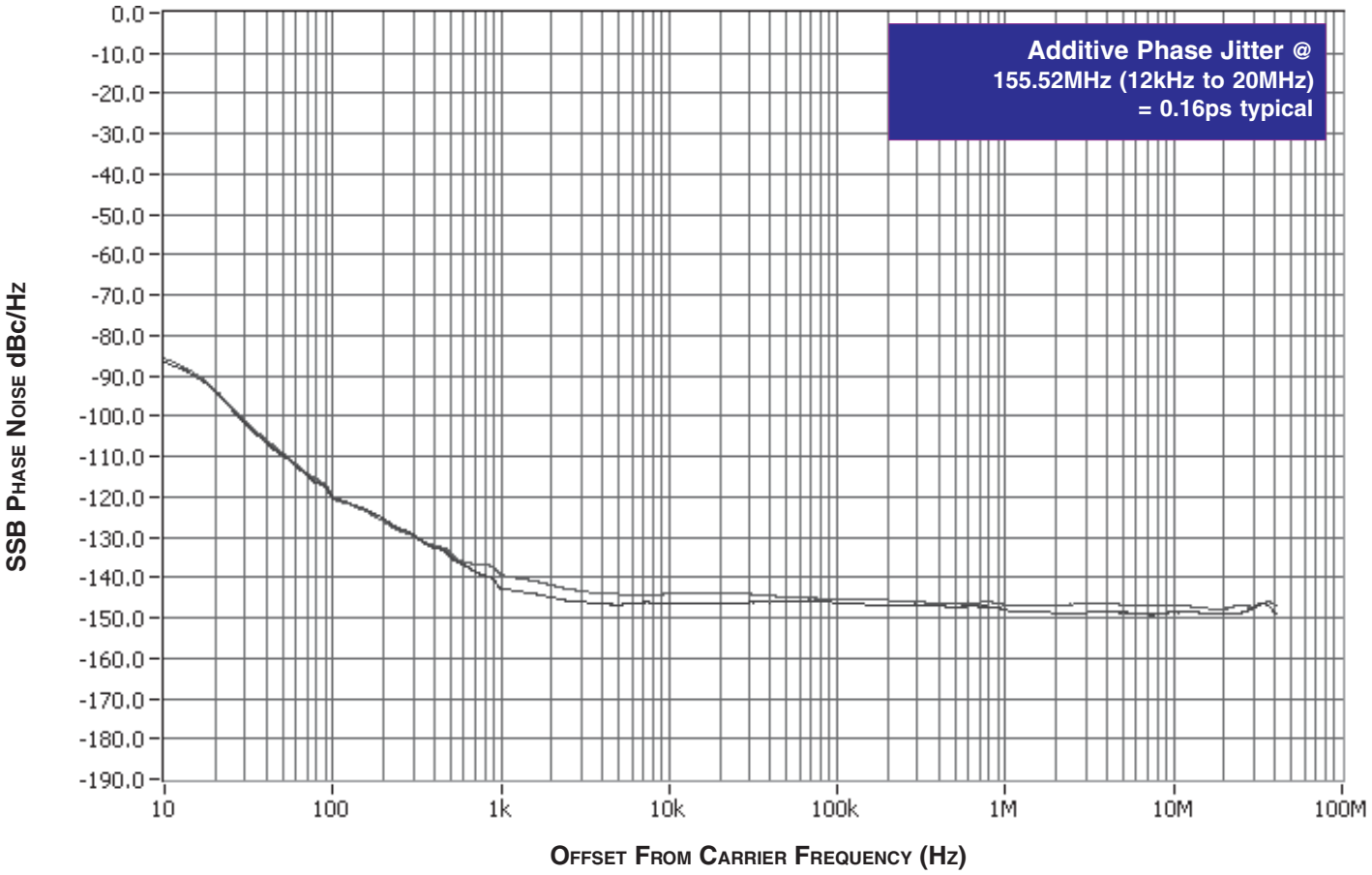
TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVCMOS} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1			3.3		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, (Integration Range: 12kHz - 20MHz)		0.21		ps
*t*sk(o)	Output Skew; NOTE 2, 4			55		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			800		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		550		ps
odc	Output Duty Cycle			50		%

All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from V_{CC} of the input to V_{CCO_LVCMOS} of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO\_LVCMOS.}$
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{CCO\_LVCMOS.}$
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

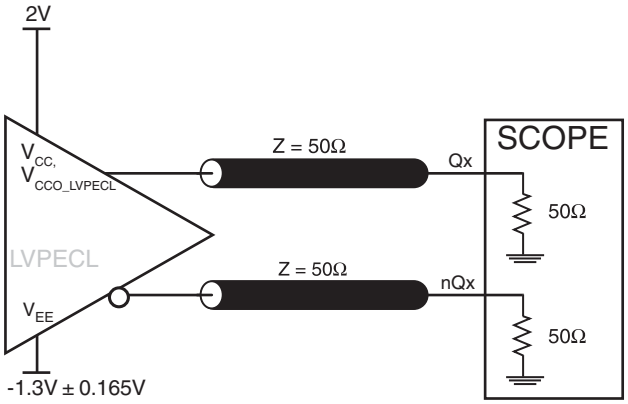
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

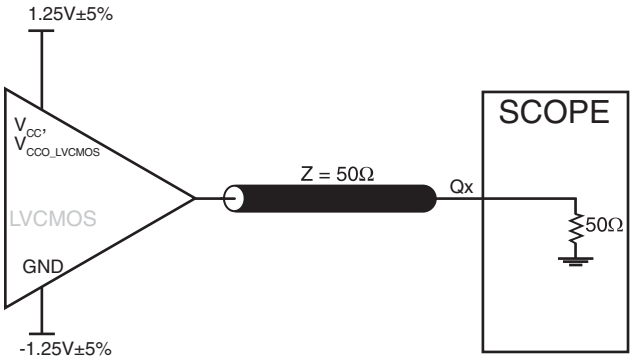


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

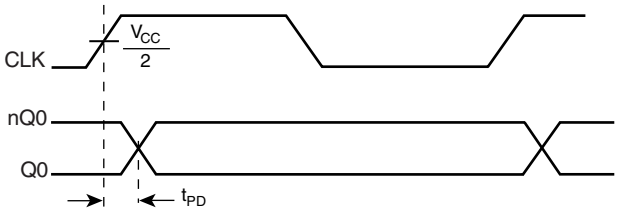
PARAMETER MEASUREMENT INFORMATION



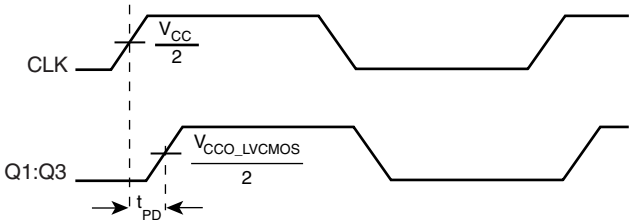
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



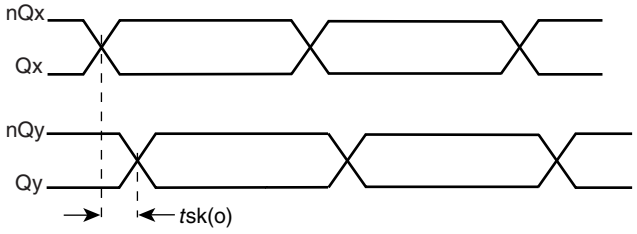
2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



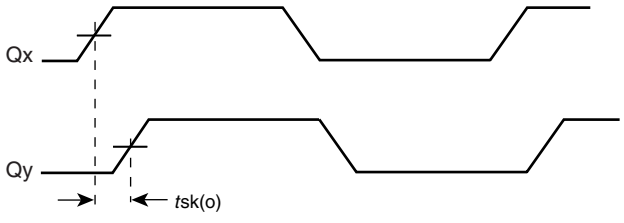
LVPECL PROPAGATION DELAY



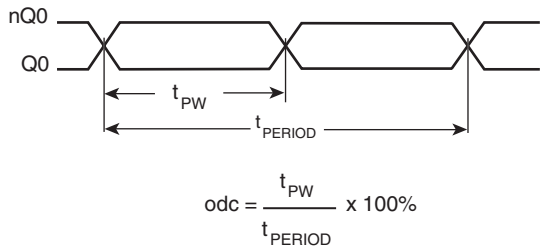
LVCMOS PROPAGATION DELAY



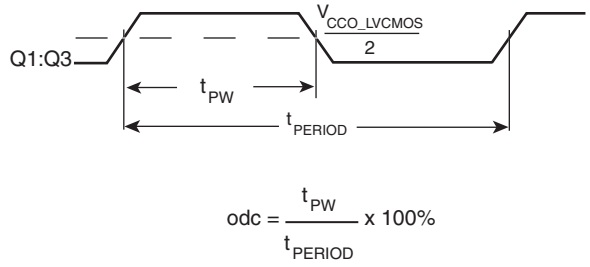
LVPECL OUTPUT SKEW



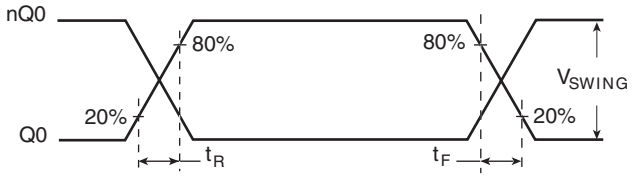
LVCMOS OUTPUT SKEW



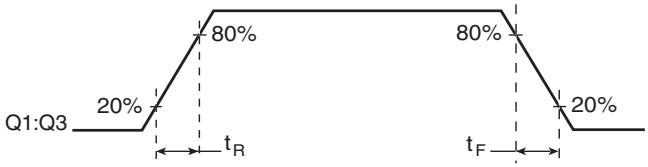
LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL OUTPUT

The unused LVPECL output can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS8534I-13 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

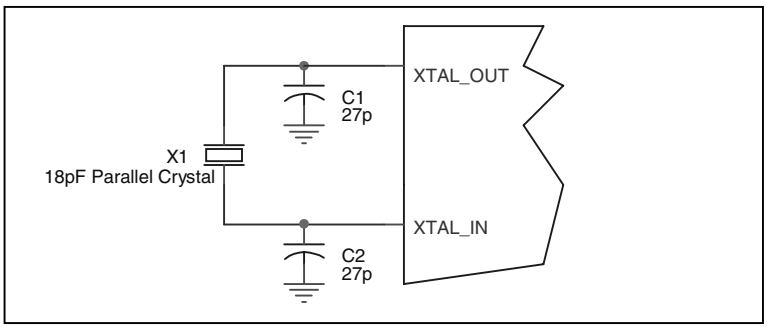


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure X.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

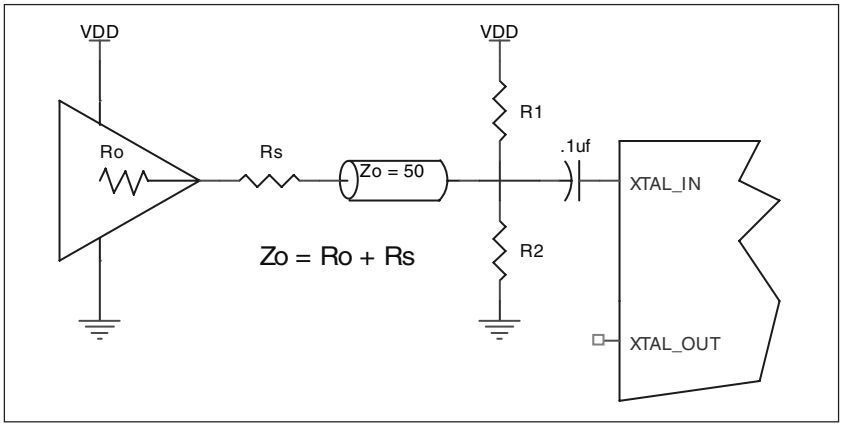


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

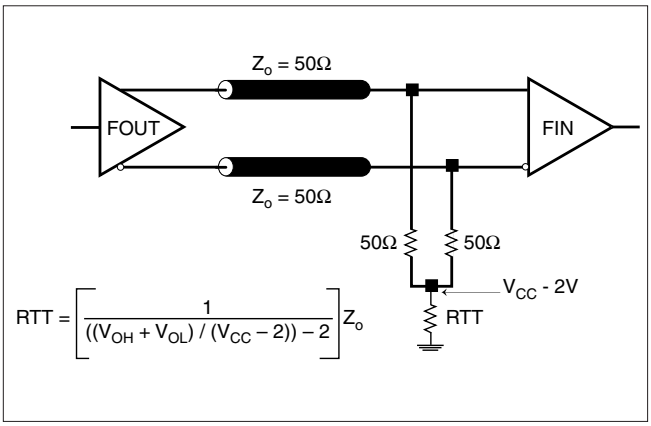


FIGURE 4A. LVPECL OUTPUT TERMINATION

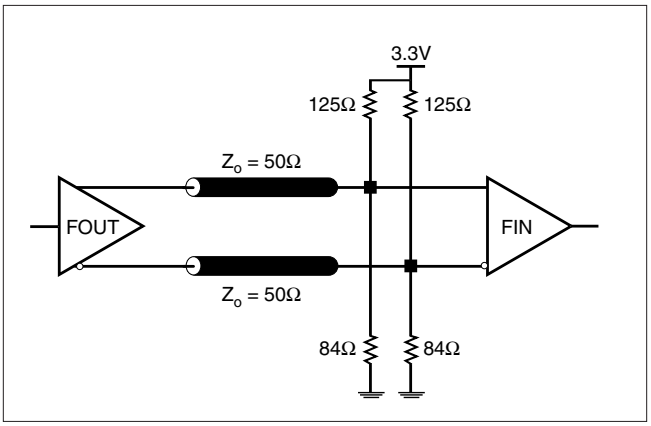


FIGURE 4B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8534I-13.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8534I-13 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVPECL Output Power Dissipation

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 60mA = **207.9mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{CCO_LVCMOS}/2

  Output Current I_{OUT} = V_{CCO_MAX} / [2 * (50Ω + R_{OUT})] = 2.625V / [2 * (50Ω + 15Ω] = **20.2mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(20.2mA)^2$ = **6.12mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 6.12mW * 3 = **18.4mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * frequency * $(V_{DDO})^2$ = 15pF * 25MHz * $(2.625V)^2$ = **2.58mW per output**
  Total Power (25MHz) = **2.58mW * 3 = 7.75mW**

Total Power Dissipation

- **Total Power**
  = Power (LVPECL) + Total Power (R_{OUT}) + Total Power (25MHz)
  = 207.9mW + 30mW + 18.4mW + 7.75mW
  = 264mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 90°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.264W * 90°C/W = 108.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 16-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	90°C/W	82°C/W	78°C/W

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	90°C/W	82°C/W	78°C/W

TRANSISTOR COUNT

The transistor count for ICS8534I-13 is: 550

Package Outline - G Suffix for 16 Lead SOIC

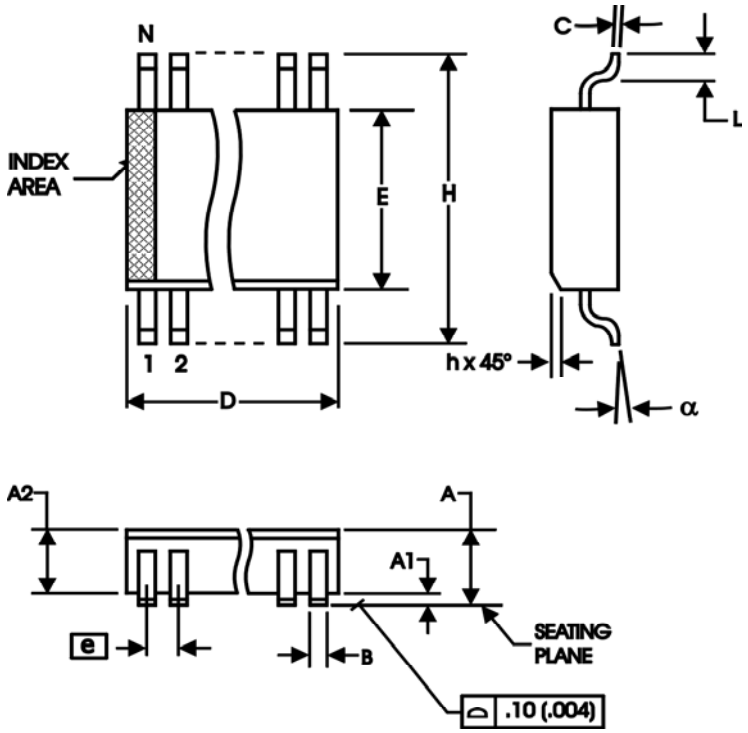


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	16	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8534BMI-13	8534BMI-13	16 lead SOIC	tube	-40°C to 85°C
ICS8534BMI-13T	8534BMI-13	16 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS8534BMI-13LF	8534BMI-13L	16 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS8534BMI-13LFT	8534BMI-13L	16 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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