

MAXIM

1MSPS, μ P-Compatible, 8-Bit ADC with 1 μ A Power-Down

MAX153

General Description

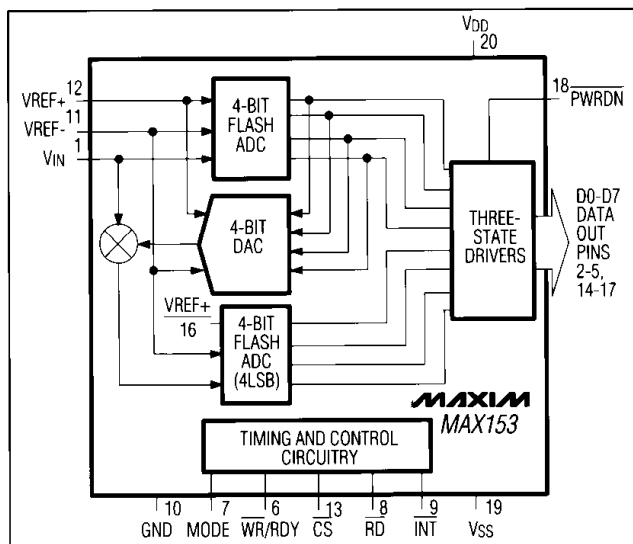
The MAX153 high-speed, microprocessor (μ P)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1M samples per second (MSPS). It operates with single +5V or dual $\pm$ 5V supplies and accepts either unipolar or bipolar inputs. A POWER-DOWN pin reduces current consumption to a typical value of 1 μ A (with 5V supply). The part returns from power-down to normal operating mode in less than 200ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX153 is DC and dynamically tested. Its μ P interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a μ P data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Applications

Cellular Telephones
Portable Radios
Battery-Powered Systems
Burst-Mode Data Acquisition
Digital-Signal Processing
Telecommunications
High-Speed Servo Loops

Functional Diagram



Features

- ◆ 660ns Conversion Time
- ◆ Power-Up/Power-Down in 200ns
- ◆ Internal Track/Hold
- ◆ 1MSPS Throughput
- ◆ Low Power: 40mW (Operating Mode)
5 μ W (Powerdown Mode)
- ◆ 1MHz Full-Power Bandwidth
- ◆ 20-Pin Narrow DIP, SO and SSOP Packages
- ◆ No External Clock Required
- ◆ Unipolar/Bipolar Inputs
- ◆ Single +5V or Dual $\pm$ 5V Supplies
- ◆ Ratiometric Reference Inputs

Ordering Information

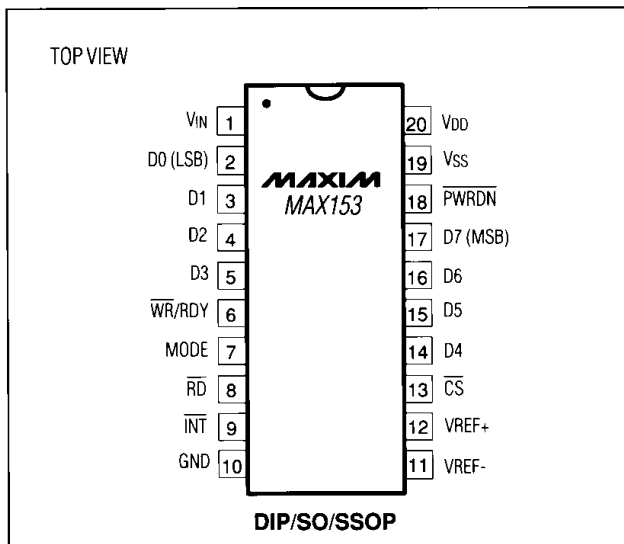
PART	TEMP. RANGE	PIN-PACKAGE
MAX153CPP	0°C to +70°C	20 Plastic DIP
MAX153CWP	0°C to +70°C	20 Wide SO
MAX153CAP	0°C to +70°C	20 SSOP***
MAX153C/D	0°C to +70°C	Dice*
MAX153EPP	-40°C to +85°C	20 Plastic DIP
MAX153EWP	-40°C to +85°C	20 Wide SO
MAX153EAP	-40°C to +85°C	20 SSOP***
MAX153MJP	-55°C to +125°C	20 Cerdip**

* Contact factory for dice specifications.

** Contact factory for availability and processing to MIL-STD-883.

*** Contact factory for availability of SSOP packages.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +7V
V _{SS} to GND	+0.3V to -7V
Digital Input Voltage to GND	+0.3V, V _{DD} + 0.3V
Digital Output Voltage to GND	-0.3V, V _{DD} + 0.3V
VREF+ to GND	V _{SS} -0.3V to V _{DD} + 0.3V
VREF- to GND	V _{SS} -0.3V to V _{DD} + 0.3V
V _{IN} to GND	V _{SS} -0.3V to V _{DD} + 0.3V

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 11.11mW/°C above +70°C)	889mW
Wide SO (derate 10.00mW/°C above +70°C)	800mW
SSOP (derate 8.00mW/°C above +70°C)	600mW
CERDIP (derate 11.11mW/°C above +70°C)	889mW

Operating Temperature Ranges:

MAX153C	0°C to +70°C
MAX153E	-40°C to +85°C
MAX153MJP	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V $\pm$ 5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V $\pm$ 5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	Unipolar range			± 1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			± 1	LSB
Zero-Code Error		Bipolar input range			± 1	LSB
Full-Scale Error		Bipolar input range			± 1	LSB
DYNAMIC PERFORMANCE (Note 1)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX153C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz MAX153M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz	45			dB
Total Harmonic Distortion	THD	MAX153C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz MAX153M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz			-50	dB
Peak Harmonic or Spurious Noise		MAX153C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz MAX153M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz			-50	dB
Conversion Time (WR-RD Mode) (Note 2)	t _{CWR}	T _A = +25°C, t _{RD} < t _{INTL} , C _L = 20pF			660	ns
Conversion Time (RD Mode)	t _{CRD}	T _A = +25°C			700	ns
		T _A = T _{MIN} to T _{MAX}	MAX153C/E		875	
			MAX153M		975	
Full-Power Input Bandwidth	*	V _{IN} = 5V _{p-p}		1		MHz
Input Slew Rate			3.14	15		V/ μ s

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V $\pm$ 5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V $\pm$ 5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range	V _{IN}		VREF-		VREF+	V
Input Leakage Current	I _{IN}	-5V $\leq$ V _{IN} $\leq$ 5V			$\pm$ 3	μ A
Input Capacitance	C _{IN}			22		pF
REFERENCE INPUT						
Reference Resistance	RREF		1	2	4	k Ω
VREF+ Input Voltage Range			VREF-		V _{DD}	V
VREF- Input Voltage Range			V _{SS}		VREF+	V
LOGIC INPUTS						
Input High Voltage	V _{INH}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{PWRDN}}$	2.4			V
		MODE	3.5			
Input Low Voltage	V _{INL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{PWRDN}}$			0.8	V
		MODE			1.5	
Input High Current	I _{INH}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{PWRDN}}$			1	μ A
		$\overline{\text{WR}}$			3	
		MODE		50	200	
Input Low Current	I _{INL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{PWRDN}}$			$\pm$ 1	μ A
Input Capacitance (Note 3)	C _{IN}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PWRDN}}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output Low Voltage	V _{OL}	I _{SINK} = 1.6mA, $\overline{\text{INT}}$, D0-D7			0.4	V
		RDY, I _{SINK} = 2.6mA			0.4	
Output High Voltage	V _{OH}	I _{SOURCE} = 360 μ A, $\overline{\text{INT}}$, D0-D7	4			V
Floating State Current	I _{LKG}	D0-D7, RDY			$\pm$ 3	μ A
Floating Capacitance (Note 3)	C _{OUT}	D7-D0, RDY		5	8	pF
POWER REQUIREMENTS						
V _{DD}	V _{DD}	$\pm$ 5% for specified accuracy		5		V
V _{SS} (Unipolar Operation)	V _{SS}			GND		V
V _{SS} (Bipolar Operation)	V _{SS}	$\pm$ 5% for specified accuracy		-5		V
V _{DD} Supply Current	I _{DD}	$\overline{\text{CS}} = \overline{\text{RD}} = 0\text{V}$, $\overline{\text{PWRDN}} = 5\text{V}$	MAX153C	8	15	mA
			MAX153E/M	8	20	
Power-Down V _{DD} Current		$\overline{\text{CS}} = \overline{\text{RD}} = 5\text{V}$, $\overline{\text{PWRDN}} = 0\text{V}$ (Note 4)		1	100	μ A
V _{SS} Supply Current	I _{SS}	$\overline{\text{CS}} = \overline{\text{RD}} = 0\text{V}$, $\overline{\text{PWRDN}} = 5\text{V}$		25	100	μ A
Power-Down V _{SS} Current		$\overline{\text{CS}} = \overline{\text{RD}} = 5\text{V}$, $\overline{\text{PWRDN}} = 0\text{V}$		12	100	μ A
Power-Supply Rejection	PSR	V _{DD} = 4.75V to 5.25V, VREF+ = 4.75V max, unipolar mode		$\pm$ 1/16	$\pm$ 1/4	LSB

Note 1: Bipolar input range, V_{IN} = $\pm$ 2.5V_{p-p}, WR-RD mode

Note 2: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.

Note 3: Guaranteed by design.

Note 4: Tested with $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{PWRDN}}$ at CMOS logic levels. Power-down current increases to several hundred μ A at TTL levels.

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TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +5V $\pm$ 5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V $\pm$ 5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{CS}}$ to $\overline{\text{RD}}/\overline{\text{WR}}$ Setup Time	t _{CSS}		0			ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}/\overline{\text{WR}}$ Hold Time	t _{CSH}		0			ns
$\overline{\text{CS}}$ to $\overline{\text{RDY}}$ Delay (Note 6)	t _{RDY}	C _L = 50pF			70	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 50pF			85	
					100	
Data-Access Time (RD Mode) (Note 2)	t _{ACC0}	C _L = 20pF			t _{CRD} +25	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF			t _{CRD} +30	
					t _{CRD} +35	
		C _L = 100pF			t _{CRD} +50	
		T _A = T _{MIN} to T _{MAX} , C _L = 100pF			t _{CRD} +65	
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ Delay (RD Mode)	t _{INTH}	C _L = 50pF		50	80	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 50pF			85	
					90	
Data-Hold Time (Note 7)	t _{DH}				60	ns
		T _A = T _{MIN} to T _{MAX}			70	
					80	
Delay Time Between Conversions (Acquisition Time)	t _p		160			ns
		T _A = T _{MIN} to T _{MAX}			185	
					260	
Write Pulse Width	t _{WR}		0.250		10	μ s
		T _A = T _{MIN} to T _{MAX}			10	
			0.280		10	
Delay Time Between WR and RD Pulses	t _{RD}		250			ns
		T _A = T _{MIN} to T _{MAX}			350	
					450	
$\overline{\text{RD}}$ Pulse Width (WR-RD Mode) Determined by t _{ACC1}	t _{READ1}	Figure 6	160			ns
		T _A = T _{MIN} to T _{MAX} , Figure 6			205	
					240	

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TIMING CHARACTERISTICS (Note 4) (continued)

(V_{DD} = +5V $\pm$ 5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V $\pm$ 5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data-Access Time (WR-RD Mode) (Note 2) t _{RD} < t _{INTL}	t _{ACC1}	C _L = 20pF, Figure 6			160	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF, Figure 6	MAX153C/E		205	
					240	
		C _L = 100pF, Figure 6			185	
					235	
					275	
RD to INT Delay	t _{RI}	T _A = T _{MIN} to T _{MAX}			150	ns
					185	
					220	
WR to INT Delay	t _{INTL}	C _L = 50pF		380	500	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 50pF	MAX153C/E		610	
			MAX153M		700	
RD Pulse Width (WR-RD Mode) Determined by t _{ACC2} t _{RD} > t _{INTL}	t _{READ2}	Figure 5		65		ns
		T _A = T _{MIN} to T _{MAX} , Figure 5	MAX153C/E	75		
			MAX153M	85		
Data-Access Time (WR-RD Mode) (Note 2) t _{RD} > t _{INTL}	t _{ACC2}	C _L = 20pF, Figure 5			65	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF, Figure 5	MAX153C/E		75	
			MAX153M		85	
		C _L = 100pF, Figure 5			90	
					110	
					130	
WR to INT Delay (Pipe-Lined Mode)	t _{IHWR}	C _L = 50pF			80	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 50pF	MAX153C/E		100	
			MAX153M		120	
Data-Access Time After INT (Note 2)	t _{ID}	C _L = 20pF			30	ns
		T _A = T _{MIN} to T _{MAX} , C _L = 20pF	MAX153C/E		35	
			MAX153M		40	
		C _L = 100pF			45	
					60	
					70	

Note 5: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of +5V and timed from a 1.6V voltage level.

Note 6: R_L = 5.1k Ω pull-up resistor.

Note 7: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

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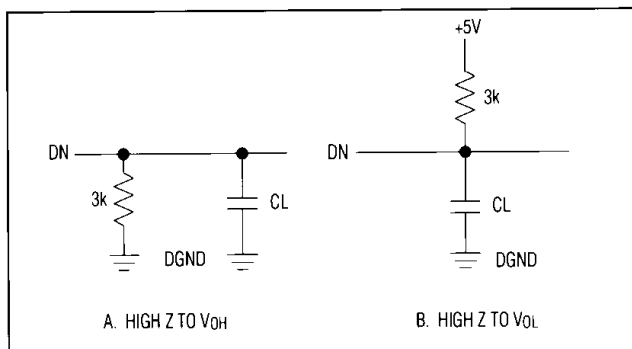


Figure 1. Load Circuits for Data-Access Time Test

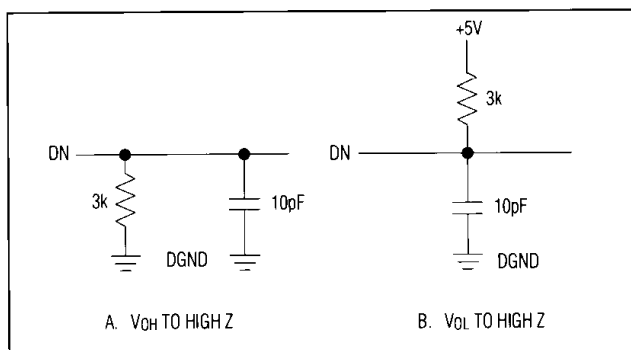
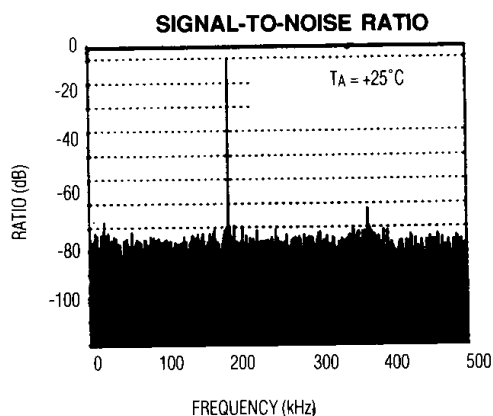
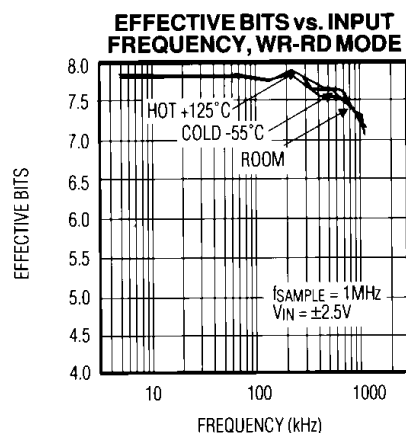
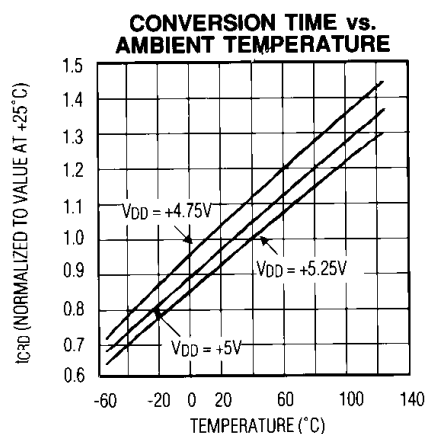
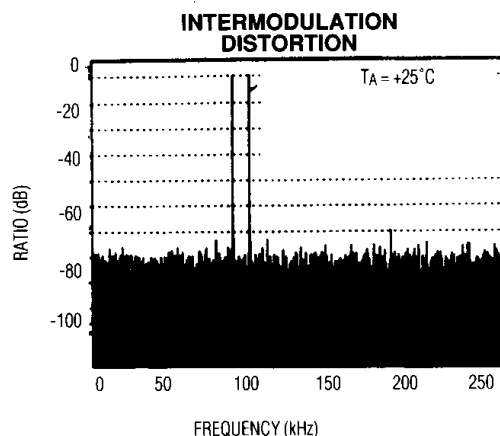


Figure 2. Load Circuits for Data-Hold Time Test

Typical Operating Characteristics



INPUT FREQUENCY = 195.8ksps ($\pm 2.5V$)
 SAMPLE FREQUENCY = 1MHz
 SNR = 49.1dB



INPUT FREQUENCY = 94.97kHz
 84.72kHz ($\pm 2.5V$)
 SAMPLE FREQUENCY = 500kHz
 IMD: 2ND-ORDER TERMS = -66.2dB
 3RD-ORDER TERMS = -60.0dB

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Pin Description

PIN	NAME	FUNCTION
1	V _{IN}	Analog Input. Range is VREF- $\leq$ V _{IN} $\leq$ VREF+.
2	D0	Three-State Data Output (LSB)
3-5	D1-D3	Three-State Data Outputs
6	WR/RDY	WRITE Control Input/READY Status Output*
7	MODE	MODE Selection Input is internally pulled low with a 50 μ A current source. MODE = 0 activates read mode. MODE = 1 activates write-read mode*
8	RD	READ Input. must be low to access data.*
9	INT	INTERRUPT Output goes low to indicate end of conversion.*
10	GND	Ground
11	VREF-	Lower limit of reference span. Sets the zero-code voltage. Range is V _{SS} $\leq$ VREF- < VREF+.
12	VREF+	Upper limit to reference span. Sets the full-scale input voltage. Range is VREF- < VREF+ $\leq$ V _{DD} .
13	CS	CHIP SELECT Input must be low for the device to recognize WR or RD inputs.
14-16	D4-D6	Three-State Data Outputs
17	D7	Three-State Data Output (MSB)
18	PWRDN	POWERDOWN Input. reduces supply current when low. CS must be high during power-down.
19	V _{SS}	Negative Supply. Unipolar: V _{SS} = 0V, Bipolar: V _{SS} = -5V
20	V _{DD}	Positive Supply, +5V

* See Digital Interface section.

Detailed Description

Converter Operation

The MAX153 uses a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper 4 data bits.

An internal digital-to-analog converter (DAC) uses the 4 most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower 4 data bits (LSBs).

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX153 can be shut down between conversions, reducing supply current to microamp levels. A TTL/CMOS logic low on the PWRDN pin shuts the device down, reducing supply current to typically 1 μ A when powered from a single 5V supply. CS must be high when power-down is used. A logic high on PWRDN wakes up the MAX153. A new conversion can be started (WR asserted low) within 360ns of the PWRDN pin being driven high (200ns to power up plus 160ns for track/hold acquisition). If power-down mode is not required, connect PWRDN to VDD.

Once the MAX153 is in power-down mode, lowest supply current is drawn with MODE low (RD mode) due to an internal 50 μ A pull-down resistor at this pin. CS must remain high during shutdown because the MAX153 may attempt to start a conversion that it cannot complete. In addition, for minimum current consumption, other digital inputs should remain stable in power-down. RDY, an open-drain output (in RD mode), will then fall and remain low throughout power-down, sinking additional supply current unless CS remains high. Refer to the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX153 has two basic interface modes set by the status of the MODE input pin. When MODE is low, the converter is in the RD mode; when MODE is high, the converter is set up for the WR-RD mode.

Read Mode (MODE = 0)

In RD mode, conversion control and data access are controlled by the RD input (Figure 4). The comparator inputs track the analog input voltage for the duration of t_p. A minimum of 160ns is required for the input to be acquired. A conversion is initiated by driving RD low. With μ Ps that can be forced into a wait state, hold RD low until output data appears. The μ P starts the conversion, waits, and then reads data with a single read instruction.

WR/RDY is configured as a status output (RDY) in RD mode, where it can drive the ready or wait input of a μ P. RDY is an open-collector output (with no internal pull-up) that goes low after the falling edge of CS and goes high at the end of the conversion. If not used, the WR/RDY pin can be left unconnected. The INT output goes low at the end of the conversion and returns high on the rising edge of CS or RD.

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Write-Read Mode (MODE = 1)

Figures 5 and 6 show the operating sequence for the write-read (WR-RD) mode. The comparator inputs track the analog input voltage for the duration of t_p . A minimum of 160ns is required for the input voltage to be acquired. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the 4 MSBs flash result is latched into the output buffers and the 4 LSBs conversion begins. $\overline{INT}$ goes low about 380ns later, indicating conversion end, and the lower 4 data bits are latched into the output buffers. The data is then accessible 65ns to 130ns after $\overline{RD}$ goes low (see *Timing Characteristics*).

If an externally controlled conversion time is required, drive $\overline{RD}$ low 250ns after $\overline{WR}$ goes high. This latches the lower 4 data bits and outputs the conversion result on

D0–D7. A minimum 160ns delay is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include the following:

Using Internal Delay

The μ P waits for the $\overline{INT}$ output to go low before reading the data (Figure 5). $\overline{INT}$ typically goes low 380ns after the rising edge of $\overline{WR}$, indicating the conversion is complete, and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 6. The internally generated delay t_{INTL}

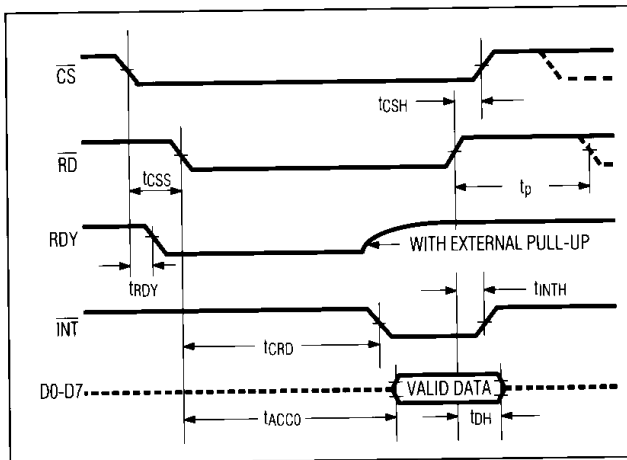


Figure 4. RD Mode Timing (MODE = 0)

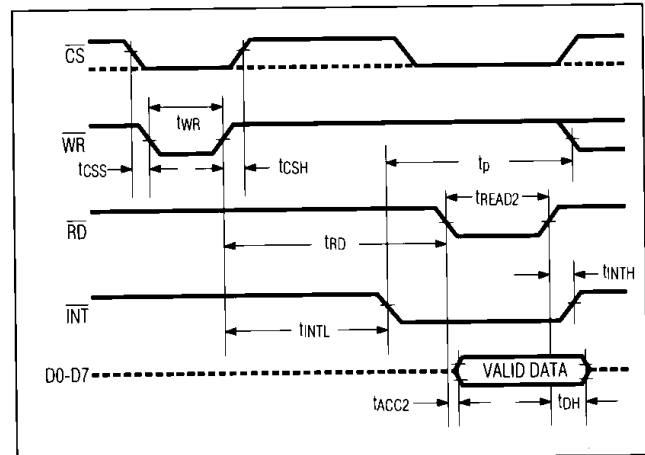


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$) (MODE = 1)

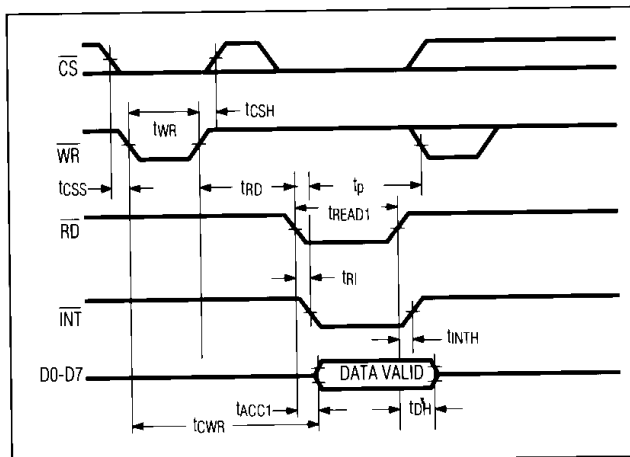


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$), Fastest Operating Mode (MODE = 1)

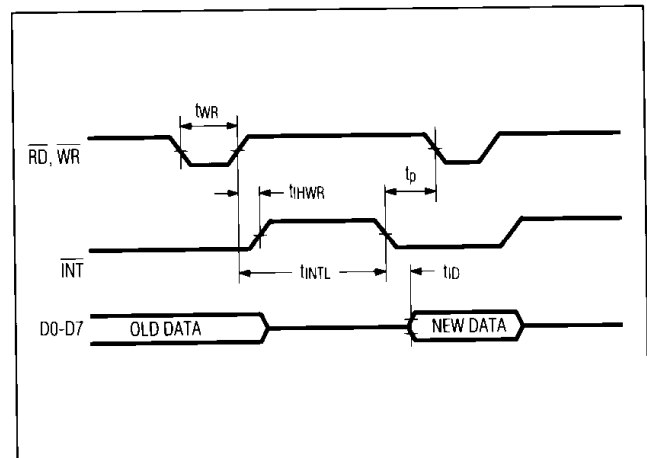


Figure 7. Pipe-Lined Mode Timing ($\overline{WR} = \overline{RD}$) (MODE = 1)

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varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{INT}$ is ignored, and $\overline{RD}$ is brought low typically 250ns after the rising edge of $\overline{WR}$. This completes the conversion and enables the output buffers (D0–D7) that contain the conversion result. $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore: $t_{CWR} = t_{WR} (250\text{ns}) + t_{CSH} (0\text{ns}) + t_{RD} (250\text{ns}) + t_{ACC1} (160\text{ns}) = 660\text{ns}$.

Pipe-Lined Operation

Besides the two standard $\overline{WR}$ - $\overline{RD}$ mode options, "pipe-lined" operation can be achieved by connecting $\overline{WR}$ and $\overline{RD}$ together (Figure 7). With $\overline{CS}$ low, driving $\overline{WR}$ and $\overline{RD}$ low initiates a conversion and reads the result of the previous conversion concurrently.

Analog Considerations

Reference

Figures 8a-8c show some reference connections. V_{REF+} and V_{REF-} inputs set the full-scale and zero-input voltages of the ADC. The voltage at V_{REF-} defines the input that produces an output code of all zeros, and the voltage at V_{REF+} defines the input that produces an output code of all ones.

The internal resistances from V_{REF+} and V_{REF-} may be as low as 1k Ω . Since current is still drawn by the reference inputs during power-down, reference supply current can be reduced during shutdown by using the circuit shown in Figure 8d. A logic-level N-channel MOSFET, connected between V_{REF-} and ground, disconnects the reference load when the ADC enters power-down.

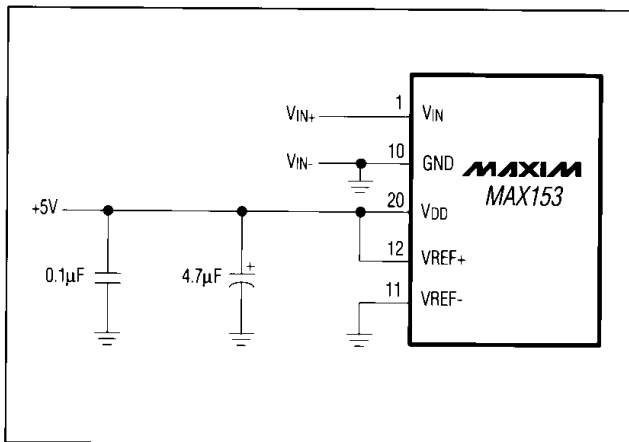


Figure 8a. Power Supply as Reference

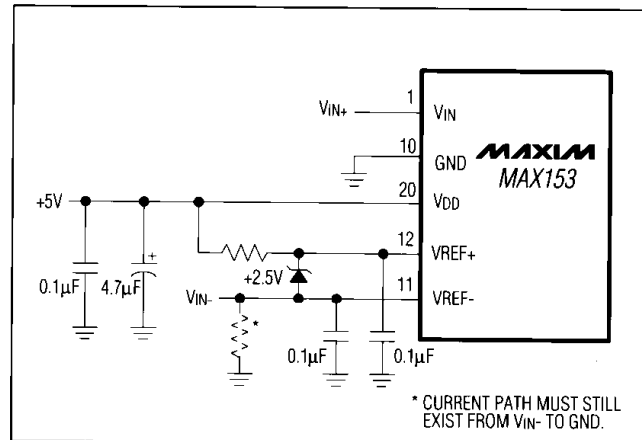


Figure 8c. Input Not Referenced to GND

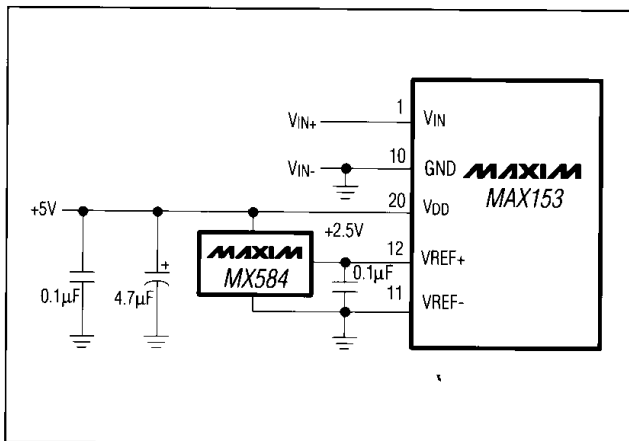


Figure 8b. External Reference, +2.5V Full Scale

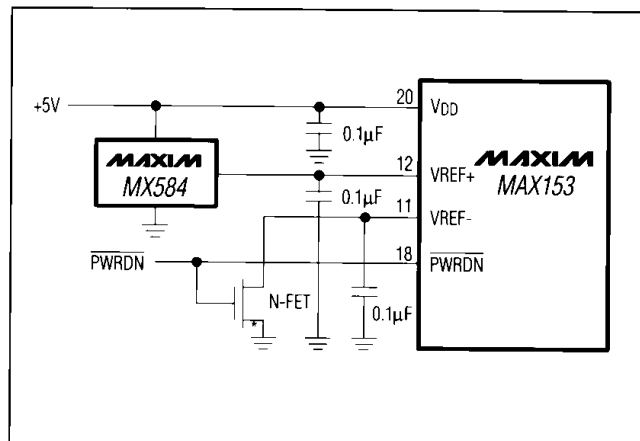


Figure 8d. An N-channel MOSFET switches off the reference load during power-down.

1MSPS, μ P-Compatible, 8-Bit ADC with 1 μ A Powerdown

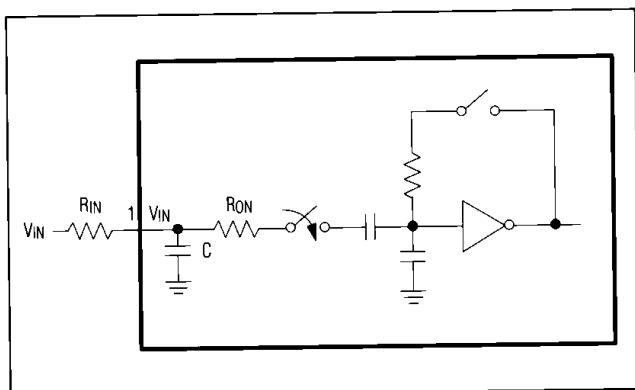


Figure 9. Equivalent Input Circuit

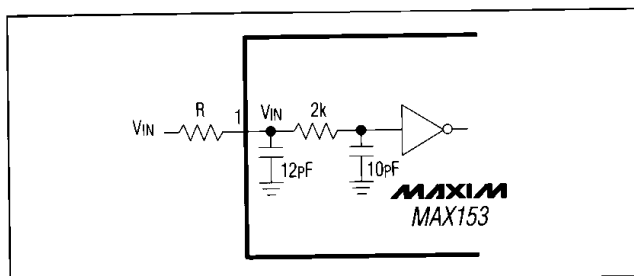


Figure 10. RC Network Equivalent Input Model

($\overline{\text{PWRDN}}$ = low). The FET should have no more than 0.5 Ω of on resistance to maintain accuracy.

Bypassing

A 4.7 μ F electrolytic in parallel with a 0.1 μ F ceramic capacitor should be used to bypass V_{DD} to GND. These capacitors should have minimal lead length.

The reference inputs should be bypassed with 0.1 μ F capacitors, as shown in Figures 8a-8c.

Input Current

Figure 9 shows the equivalent circuit of the converter input. When the conversion starts and $\overline{\text{WR}}$ is low, V_{IN} is connected to 16 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches (about 2k Ω). In addition, about 12pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 10). As source impedance increases, the capacitors take longer to charge.

The typical 22pF input capacitance allows source resistance as high as 2.2k Ω without setup problems. For

larger resistances, the acquisition time (t_p) must be increased.

Conversion Rate

The maximum sampling rate (f_{max}) for the MAX153 is achieved in the WR-RD mode ($t_{RD} < t_{INTL}$) and is calculated as follows:

$$f_{\text{max}} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_p}$$

$$f_{\text{max}} = \frac{1}{250\text{ns} + 250\text{ns} + 150\text{ns} + 160\text{ns}}$$

$$f_{\text{max}} = 1.23\text{MHz}$$

where t_{WR} = Write pulse width

t_{RD} = Delay between WR and RD pulses

t_{RI} = RD to INT delay

t_p = Delay time between conversions.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise ratio (SNR) is the ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other analog-to-digital output values. The output band is limited to one-half the A/D sample (conversion) rate. This ratio usually includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as "signal-to-noise + distortion."

The theoretical minimum A/D noise is caused by quantization error and results directly from the ADC's resolution: $\text{SNR} = (6.02N + 1.76)\text{dB}$, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT plot (*Typical Operating Characteristics*) shows the result of sampling a pure 200kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution, or "effective number of bits," the ADC provides can be measured by transposing the equation that converts resolution to SNR: $N = (\text{SNR} - 1.76)/6.02$.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \log \left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2)}}{V_1} \right]$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

1MSPS, μ P-Compatible, 8-Bit ADC with 1 μ A Power-Down

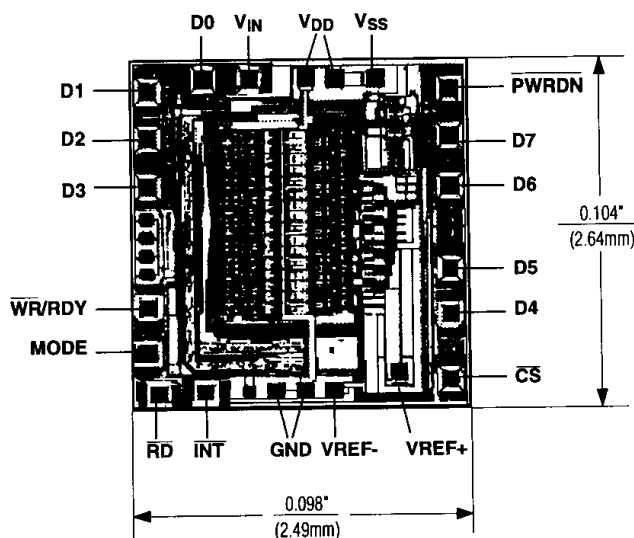
Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Intermodulation Distortion

An FFT plot of intermodulation distortion (IMD) is generated by sampling an analog input applied to the ADC. This input consists of very low distortion sine waves at two frequencies. A 2048 point plot for IMD of the MAX153 is shown in the *Typical Operating Characteristics*.

Chip Topography

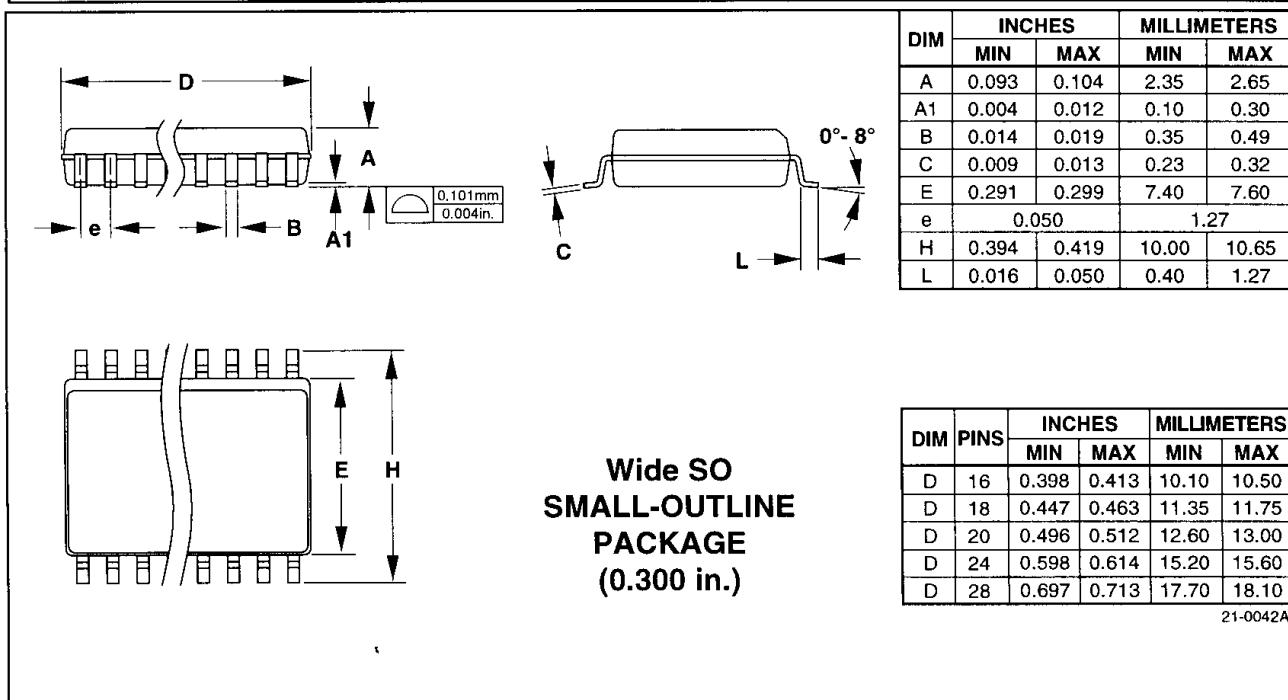
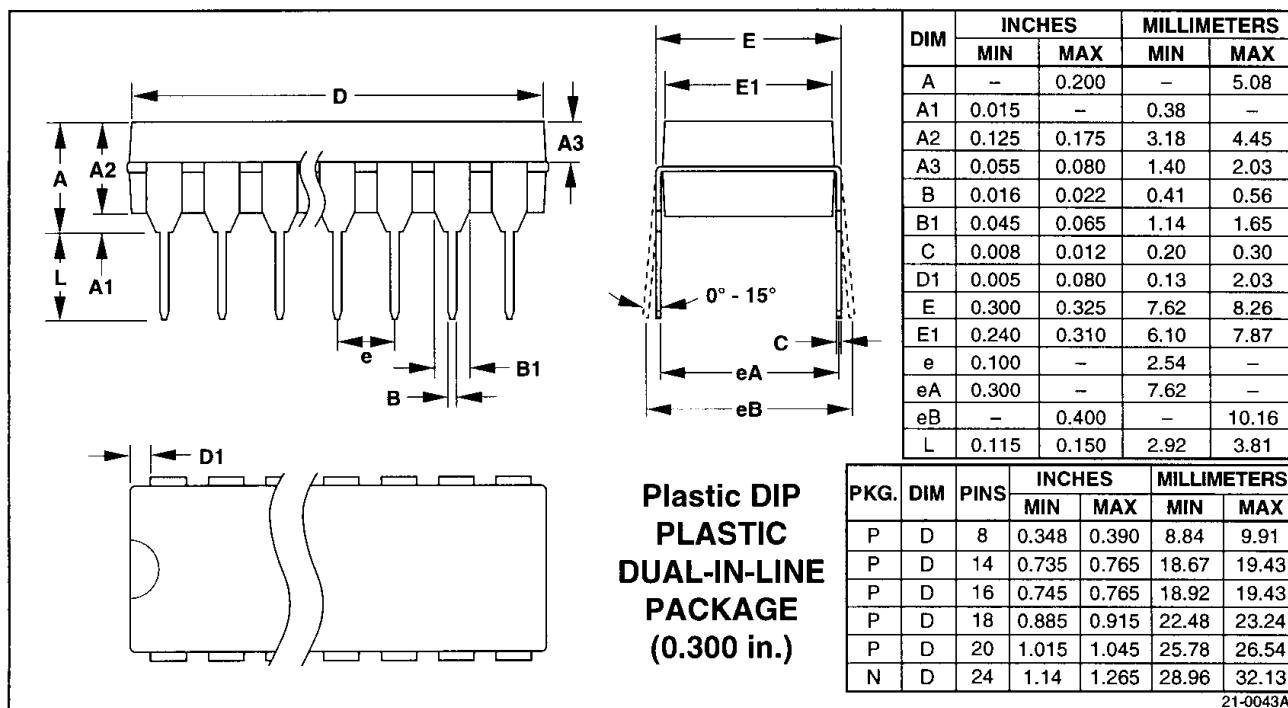


TRANSISTOR COUNT: 1856
SUBSTRATE CONNECTED TO V_{DD}

MAX153

1MSPs, μ P-Compatible, 8-Bit ADC with 1 μ A Power-Down

Package Information



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