CY22388
CY22389
CY22391

Factory Programmable Quad PLL Clock Generator with VCXO

Features

- Fully integrated phase-locked loops (PLLs)
- Small quad flat no-leads (QFN) package option
  - 40% smaller than 20-pin TSSOP
  - 22% smaller than 16-pin TSSOP
- Selectable output frequency
- Programmable output frequencies
- Output frequency range:
  - 1 MHz to 166 MHz
- Input frequency range:
  - Crystal: 10 MHz to 30 MHz
  - External reference: 1 MHz to 100 MHz
- Analog voltage-control crystal oscillator (VCXO)
- 16-/20-pin TSSOP and 32-pin QFN packages
- 3.3-V operation with 2.5-V output buffer option

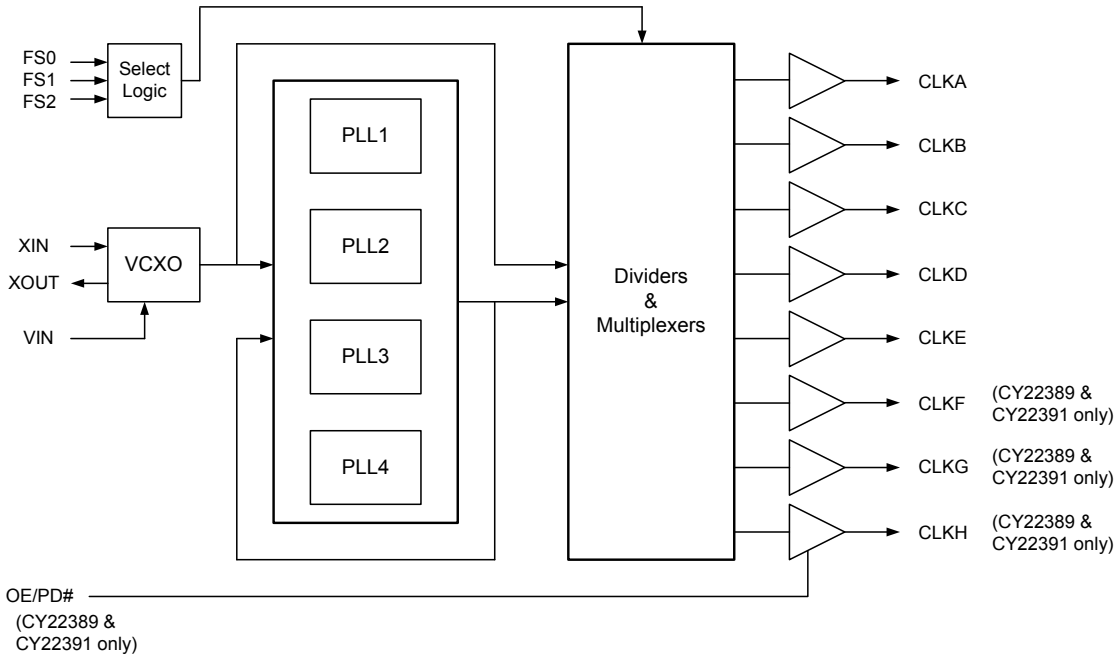
Benefits

- Meets most digital set top box, DVD recorder, and DTV application requirements
- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Integration eliminates the need for external loop filter components
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Complete VCXO solution with ±120 ppm (typical pull range)

Functional Description

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pinouts

Figure 1. 16-pin TSSOP pinout

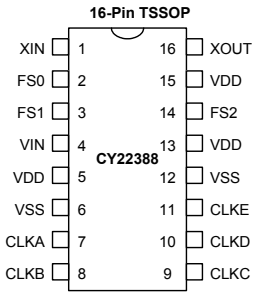


Figure 2. 20-pin TSSOP pinout

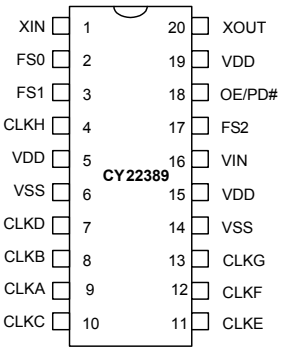
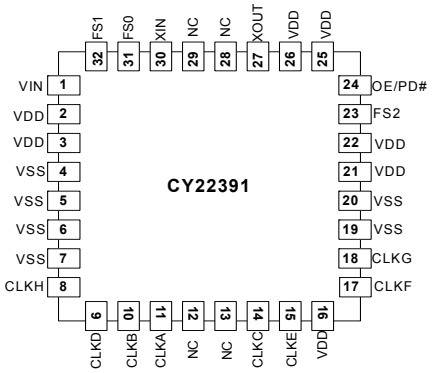


Figure 3. 32-pin QFN pinout



Pin Definitions

Pin Name	Pin Number			Pin Description
	16-pin TSSOP	20-pin TSSOP	32-pin QFN	
XIN	1	1	30	Crystal input or reference clock input
XOUT	16	20	27	Crystal output (No connect if external clock is used)
CLKA	7	9	11	Clock output
CLKB	8	8	10	Clock output
CLKC	9	10	14	Clock output
CLKD	10	7	9	Clock output
CLKE	11	11	15	Clock output
CLKF	n/a	12	17	Clock output
CLKG	n/a	13	18	Clock output
CLKH	n/a	4	8	Clock output
FS0	2	2	31	Frequency select 0
FS1	3	3	32	Frequency select 1
FS2	14	17	23	Frequency select 2
OE/PD#	n/a	18	24	Programmable control pin: Output enable (active-high) or power-down (active-low)
VIN	4	16	1	Analog control input for VCXO
VDD	5, 13, 15	5, 15, 19	2, 3, 16, 21, 22, 25, 26	Voltage supply
VSS	6, 12	6, 14	4, 5, 6, 7, 19, 20	Ground
NC	N/A	N/A	12, 13, 28, 29	No connect.

General Description

The CY22388 family of devices has an analog VCXO, four PLLs, up to eight clock outputs and frequency selection capabilities. The frequency selects do not modify any PLL frequency. Instead they allow the user to choose among eight different output divider selections depending on the clock and package configuration. This is illustrated in the Frequency Select Pin Operation tables and on page 1.

There is one programmable OE/PD#. The OE/PD# pin can be programmed as either an output enable pin or a power-down pin. The OE function can be programmed to disable a selected set of outputs when low, leaving the remaining outputs running. Full-chip power-down disables all outputs and the PLLs and most of the active circuitry when low.

Factory-Programmable CY22388/89/91

Factory programming is available for high- or low-volume manufacturing by Cypress. All requests must be submitted to the local Cypress field application engineer (FAE) or sales representative. After the request is processed, you receive a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders.

PLLs

The advantage of having four PLLs is that a single device can generate up to four independent frequencies from a single crystal. Generally a design may require up to four oscillators to accomplish what could be done with a single CY22388.

Each PLL is independent and can be configured to generate a voltage-controlled oscillator (VCO) frequency between 62.5 MHz and 250 MHz. Each PLL can then, in turn, be divided down with post dividers to generate the clock output frequency of the user's choice. The output divider allows each clock output to be divided by 1, 2, 3, 4, 5, 6, 8, 9, 10, 12 or 15. The PLL maximum is reduced to 166 MHz in 'divide by 1' mode due to output buffer limitations.

Outputs that allow frequency switching perform a glitch-free transition. A glitch is defined as a high- or low-time shorter than half the smaller of the two periods being switched between. Extended low time (even many cycles in duration) is acceptable.

Selected clock outputs are capable of being powered off a separate 2.5-V supply. This allows for driving lower voltage swing inputs. The CY22388/89/91 device still requires 3.3 V to power the oscillator and all other internal PLL circuitry. For the 2.5-V output option, refer to the CY22388 application note. Selected clocks and pinout diagrams are explained in this application note.

Clock D can obtain its output from either the reference source or PLL1/N1 with N1 being defined as the output divider for PLL1. Clock H is defined as a copy of clock D. Clock D is only available from PLL1/N1 on the 16-pin package.

For CY22388, CLKB and CLKC have related frequencies. For CY22389 and CY22391, CLKD and CLKF have related frequencies, CLKA and CLKB have related frequencies, and CLKC and CLKE have related frequencies. Related frequencies come from the same PLL but can have different divider values.

To minimize parts per million (PPM) error on the clock outputs, you must choose a crystal reference frequency that is a common multiple of the desired PLL frequencies. While this is the ideal situation, this is not always the case and the PLLs have high-resolution counters internally to help minimize frequency deviation from the desired frequency.

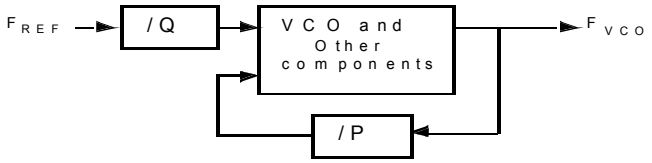
PLL VCO frequencies are generated by the following equation:

$$F_{VCO} = F_{REF} * (P / Q)$$

where F_{REF} is the reference input frequency, P is the PLL feedback divider, and Q is the reference input divider.

A PLL is a feedback system where the VCO frequency divided by P and reference frequency divided by Q are constantly being compared and the VCO frequency is adjusted to achieve a locked state. Figure 4 is a simplified drawing of a PLL.

Figure 4. PLL system



Frequency Select Pin Operation

Table 1. CY22388 16-pin TSSOP

Output Signal	Frequency Selection Lines
CLK A	FS2, FS1, FS0
CLK B	FS1, FS0
CLK C & CLK D	S0
CLK E	FIXED

Table 2. CY22389 20-pin TSSOP

Output Signal	Frequency Selection Lines
CLK A	FS2, FS1, FS0
CLK B & CLK C	FS1, FS0
CLK D, CLK E, & CLK F	FS0
CLK G	FIXED
CLK H	COPY OF CLK D

Table 3. CY22391 32-pin QFN

Output Signal	Frequency Selection Lines
CLK A	FS2, FS1, FS0
CLK B & CLK C	FS1, FS0
CLK D, CLK E, & CLK F	FS0
CLK G	FIXED
CLK H	COPY OF CLK D

Analog VCXO

There are three programmable reference operating modes for the CY22388, CY22389, and CY22391 family of devices. The first mode uses an external pullable crystal and incorporates an internal analog VCXO.

The second mode configures the internal crystal oscillator to accept an external driven reference source from 1 to 100 MHz. The input capacitance on the XIN PIN when driven in this mode is 15 pF.

The third mode disables the VCXO input control and sets the internal oscillator to a fixed frequency operation. The load capacitance seen by the external crystal when connected to PINS XIN and XOUT is equal to 12 pF.

One of the key components in the CY22388, CY22389, and CY22391 family of devices is the analog VCXO. The VCXO is used to 'pull' the reference crystal higher or lower to lock the system frequency to an external source. This is ideal for applications where the output frequency needs to track along with an external reference frequency that is constantly shifting.

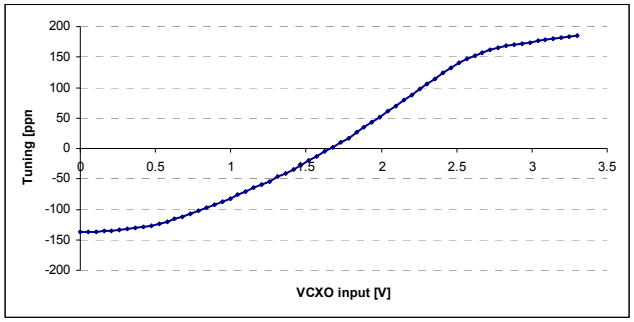
The VCXO is completely analog, so there is infinite resolution on the VCXO pull curve. The analog to digital converter steps that are normally associated with a digital VCXO input is not present in this device. A special pullable crystal must be used in order to have adequate VCXO pull range. Pullable crystal specifications are included in this datasheet.

Refer to the application note, Layout Recommendations for the CY22388, CY22389, and CY22391 Devices - ANC0001, for pullable crystal recommendations outside of the standard industry frequencies given in the Pullable Crystal specifications.

VCXO Profile

Figure 5 shows an example of what a VCXO profile looks like. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This has the effect of moving the PPM from a negative to positive offset.

Figure 5. VCXO Profile



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}/AV_{DD}/V_{DDL}$	Core supply voltage		–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-Functional	–65	125	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (human body model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability rating	V-0 at 1/8 in.	–	10	ppm
MSL	Moisture sensitivity level	All packages	3		–

Pullable Crystal Specifications

Parameter [1, 2]	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	13.5-MHz and 27-MHz crystal AT-Cut	Parallel resonance, fundamental mode	See Note 2			
C_{LNOM}	Nominal load capacitance	Order crystal at one specific C_{LNOM} 0 ppm	11.4	12	12.6	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode (CL = Series)	–	–	40	Ω
DL	Crystal drive level	Nominal V_{DD} at 25 °C over ±120 ppm pull range	–	–	300	µW
C_0[3]	Crystal shunt capacitance		1.5	3	4.0	pF
C_1[3]	Crystal motional capacitance		12	14	16.8	fF
F_{3SEPHI}[2]	Third overtone separation from 3 × F_{NOM}	Mechanical third (high side of 3 × F_{NOM})	240	–	–	ppm
F_{3SEPLO}[2]	Third overtone separation from 3 × F_{NOM}	Mechanical third (low side of 3 × F_{NOM})	–	–	–120	ppm

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
$V_{DD}/AV_{DD}/V_{DDL}$	Operating voltage	3.0	3.3	3.6	V
T_A	Ambient temperature	–10	–	70	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD}s reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Notes
1. Device operates to the following specs, which are guaranteed by design.
2. Refer to CY22388 Application Note and online software for a list of approved crystal specifications.
3. Increased tolerance available from pull range less than ±120 ppm.

DC Parameters

Parameter [4]	Description	Conditions	Min	Typ	Max	Unit
I_{OH}[5]	Output high current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{OL}[5]	Output low current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{IH}	Input high current	$V_{IH} = V_{DD}$, excluding Vin, Xin	–	5	10	µA
I_{IL}	Input low current	$V_{IL} = 0$ V, excluding Vin, Xin	–	5	10	µA
V_{IH}	Input high voltage	FS0/1/2 OE input CMOS levels	0.7 × A_{VDD}	–	–	V
V_{IL}	Input low voltage	FS0/1/2 OE input CMOS levels	–	–	0.3 × A_{VDD}	V
V_{VCXO}	VIN input range		0	–	A_{VDD}	V
C_{IN}	Input capacitance	FS0/1/2 and OE pins only	–	–	7	pF
I_{VDD}	Supply current	$V_{DD}/AV_{DD}/V_{DDL}$ current	–	60	–	mA
C_{INXIN}	Input capacitance at XIN	VCXO disabled external reference	–	15	–	pF
C_{INXTAL}	Input capacitance at crystal	VCXO disabled fixed frequency oscillator	–	12	–	pF

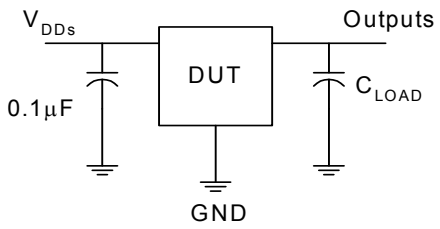
Notes
4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
5. Custom drive level is available upon request.

AC Parameters

Parameter [4]	Description	Conditions	Min	Typ	Max	Units
1/t1	Output frequency	PLL $_{minmax}$/Divider$_{maximum}$	4.2	–	166	MHz
DC1	Output duty cycle (excluding REFOUT)	Duty cycle is defined in Figure 7; t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is ≤ 125 MHz)	45	50	55	%
DC2	Output duty cycle	Duty cycle is defined in Figure 7; t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is > 125 MHz)	40	50	60	%
DC_{REFOUT}	Output duty cycle	Duty cycle is defined in Figure 7; t_2/t_1, 50% of V_{DD} (XIN Duty Cycle = 45/55%)	40	50	60	%
ER	Rising edge rate	Output clock edge rate. Measured from 20% to 80% of V_{DD}. C_{LOAD} = 15 pF. See Figure 8.	0.75	1.2	–	V/ns
EF	Falling edge rate	Output clock edge rate. Measured from 80% to 20% of V_{DD}. C_{LOAD} = 15 pF. See Figure 8.	0.75	1.2	–	V/ns
T_9	Clock jitter	Period jitter	–	±250	–	ps
T_{10}	PLL lock time		–	1	5	ms
$f_{\Delta XO}$	VCXO crystal pull range	Using non-SMD-49 crystal specified in CY22388 application note, *ANC0002"* Nominal crystal frequency input assumed (0 ppm) at 25 °C and 3.3 V	±110	±120	–	ppm
		Using SMD-49 crystal specified in CY22388 application note, *ANC0002"* Nominal crystal frequency input assumed (0 ppm) at 25 °C and 3.3 V	±105	±120	–	ppm

Test and Measurement

Figure 6. Test and Measurement



Voltage and Timing Definitions

Figure 7. Duty Cycle Definition

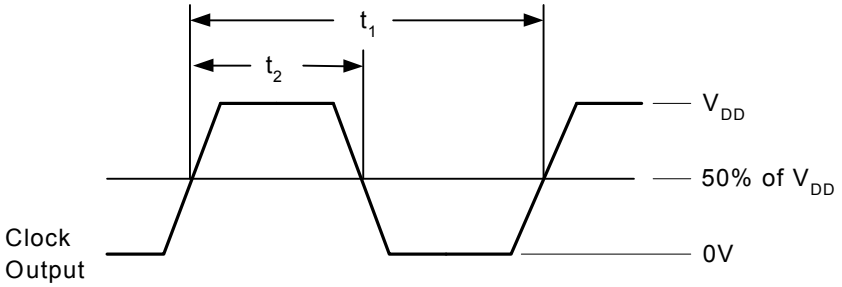


Figure 8. ER = (0.6 × V_{DD})/t_3, EF = (0.6 × V_{DD})/t_4

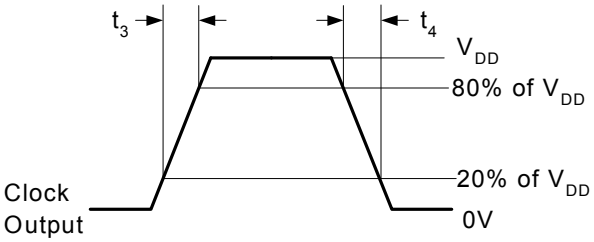
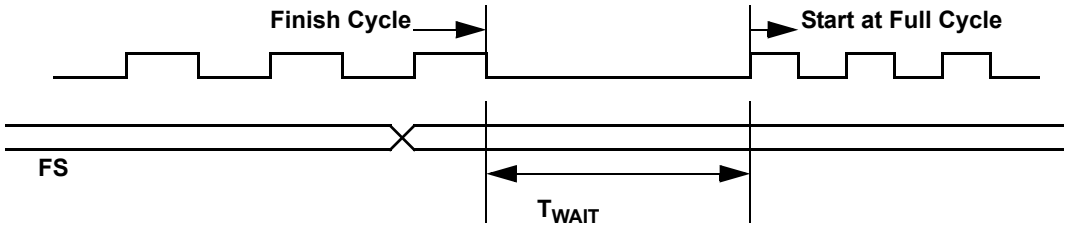


Figure 9. FS Controlled Clock Output



Ordering Information

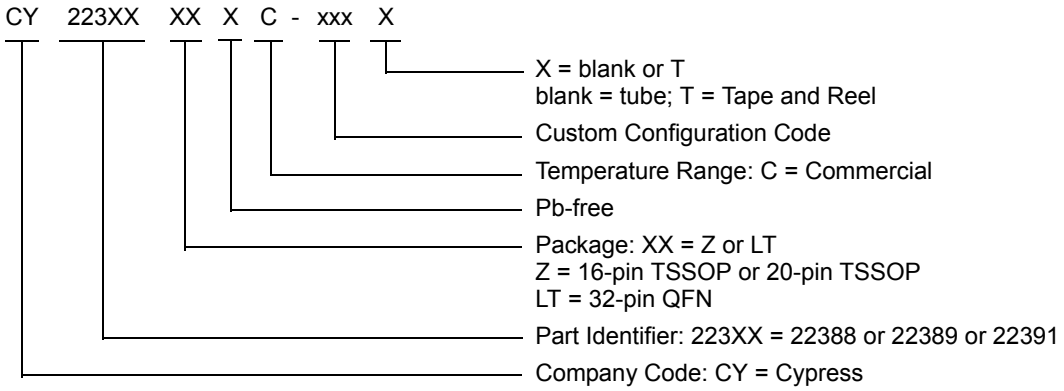
All product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Part Number	Package	Type	Production Flow
Pb-free			
CY22388FZXC	ZZ16	16-pin TSSOP	Commercial, 0 °C to +70 °C
CY22388FZXCT	ZZ16	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to +70 °C

Possible Configurations

Part Number [6]	Package	Type	Production Flow
Pb-free			
CY22388ZXC-xxx	ZZ16	16-pin TSSOP	Commercial, 0 °C to +70 °C
CY22388ZXC-xxxT	ZZ16	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to +70 °C
CY22389ZXC-xxx	ZZ20	20-pin TSSOP	Commercial, 0 °C to +70 °C
CY22389ZXC-xxxT	ZZ20	20-pin TSSOP – Tape and Reel	Commercial, 0 °C to +70 °C
CY22391LTXC-xxx	LT32	32-pin QFN (Sawn)	Commercial, 0 °C to +70 °C
CY22391LTXC-xxxT	LT32	32-pin QFN (Sawn) – Tape and Reel	Commercial, 0 °C to +70 °C

Ordering Code Definitions



Notes
6. The CY22388ZXC-xxx, CY22389ZXC-xxx, and CY22391LTXC-xxx are factory-programmed configurations. For more details, contact your local Cypress FAE or sales representative.

Package Drawing and Dimensions

Figure 10. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091

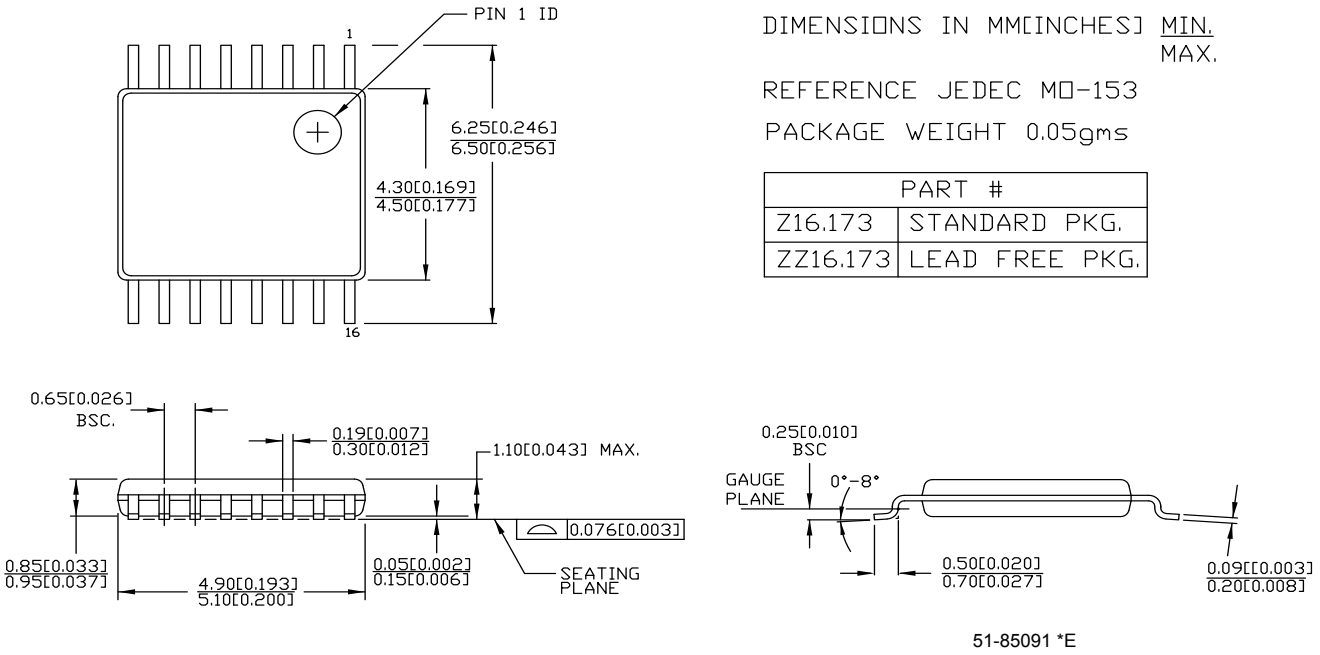
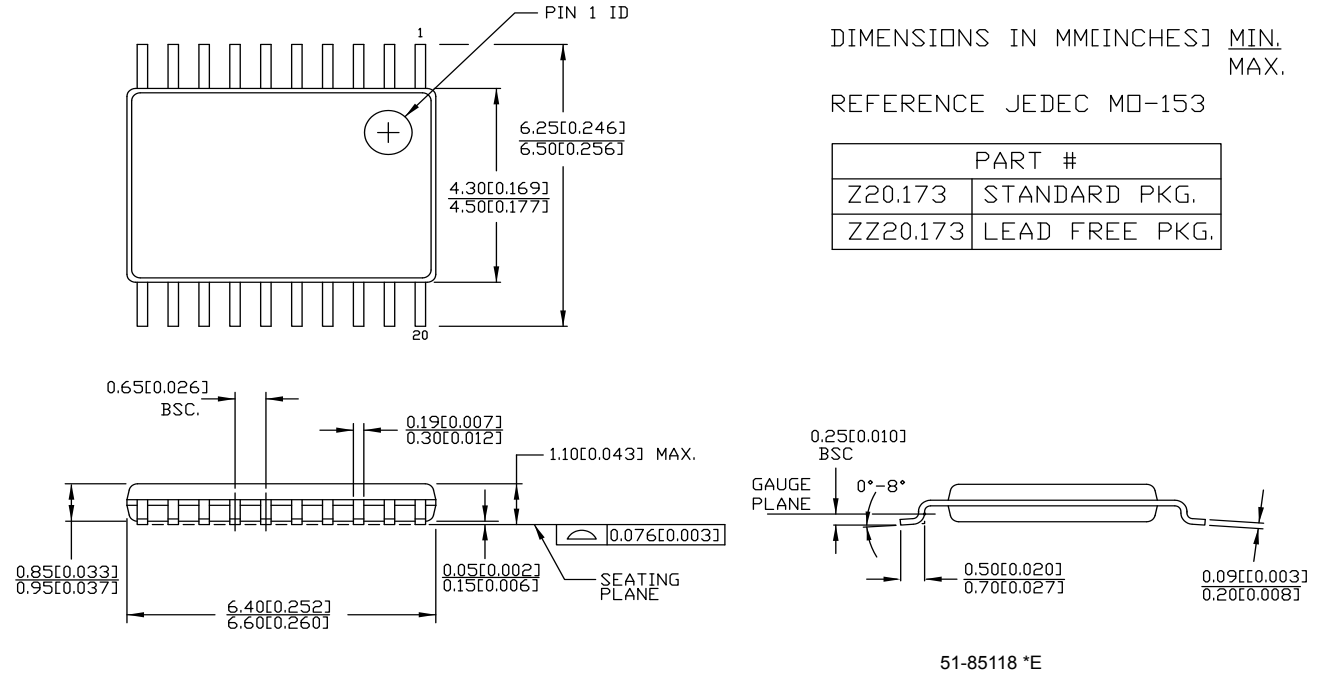
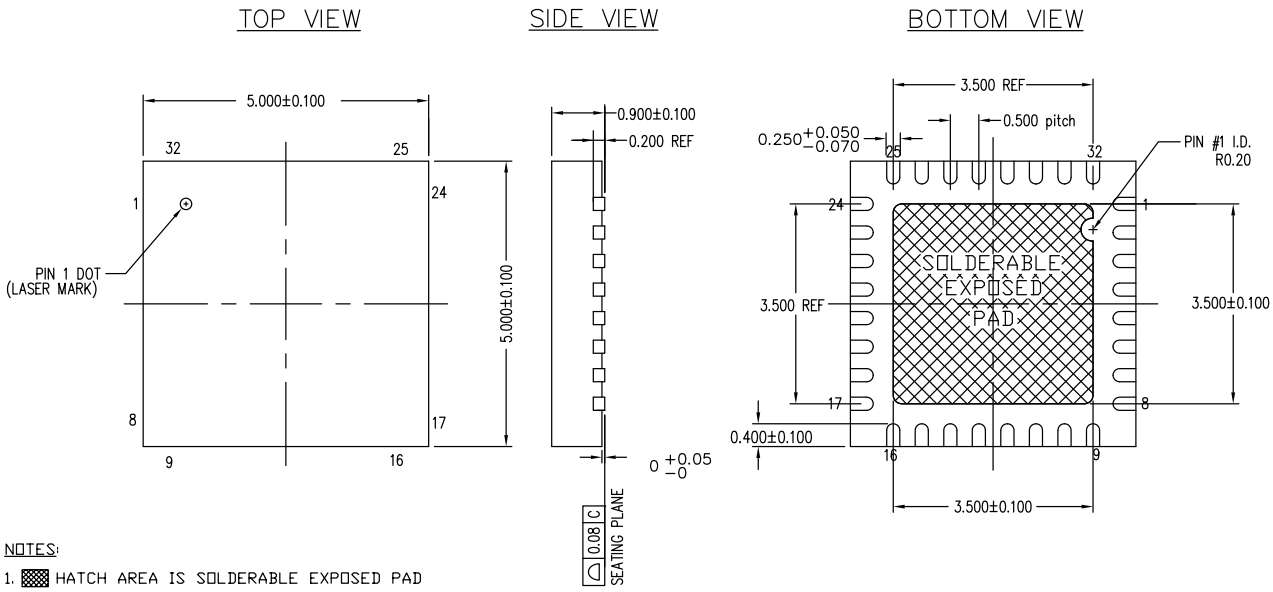


Figure 11. 20-pin TSSOP (4.40 mm Body) Z20.173/ZZ20.173 Package Outline, 51-85118



Package Drawing and Dimensions (continued)

Figure 12. 32-pin QFN (5 × 5 × 1.0 mm) LT32B 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-30999



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: SEE CYPRESS PACKAGE MATERIAL DECLARATION DATASHEET (PMDD) POSTED ON THE CYPRESS WEB

001-30999 *D

Acronyms

Acronym	Description
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FAE	Field Application Engineer
FS	Frequency Select
PJ	Period Jitter
PLL	Phase-Locked Loop
QFN	Quad Flat No-leads
TSSOP	Thin Shrunk Small Outline Package
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
fF	femtofarad
KΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
PPM	parts per million
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY22388/CY22389/CY22391, Factory Programmable Quad PLL Clock Generator with VCXO Document Number: 38-07734				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	320458	RGL	03/07/05	New data sheet Internal setting in VCXO are XOB/A=110, Offset=1110, Gain=101
*A	389649	RGL	08/02/05	Changed R1 value to max. 40Ω Changed DL comments and max. value to 300µW Changed $f_{\Delta XO}$ min. value to ±110ppm and typ. value to ±120ppm
*B	523597	RGL	11/12/06	Specified a non-SMD-49 and SMD-49 crystal specs in the VCXO Pull Range Parameter
*C	2632357	KVM	01/13/09	Changed document title to spell out each part number in full. Updated Ordering Information table to add tape & reel part numbers. Added LT32 (saw) QFN package for CY22391, including package drawing. LY32 (punch) QFN package “not recommended for new designs” Added Package column to Ordering Information table and cleaned up package references in captions of the package drawings. Clarified that Power Down (PD#) is active-low: in block diagram, CY22389 pinout and in pin description table. Replaced PDWN and PD with PD#. Updated Package Drawing and Dimensions: spec 51-85188 – Changed revision from *A to *B. Updated to new template.
*D	2897246	KVM	03/22/10	Updated Ordering Information: Added description (Regarding Possible Configurations). Updated Possible Configurations: Updated part numbers. Updated Note 6. Removed Note “Not recommended for new designs. The LY32 QFN package transitions to the LT32 QFN.”. Updated Package Drawing and Dimensions: 51-85091 – Changed revision from *A to *B. 51-85118 – Changed revision from *A to *B. 001-30999 – Changed revision from *A to *C. Removed spec 51-85188 *B.
*E	3030336	CXQ	09/14/10	Fixed various typos. Updated Features: Fixed formatting. Updated Absolute Maximum Conditions: Updated value of MSL parameter as 3 for all packages. Updated Operating Conditions: Removed “Recommended” from heading. Added Ordering Code Definitions under Ordering Information. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *B to *C. spec 51-85118 – Changed revision from *B to *C. Added Acronyms, and Units of Measure. Updated Sales, Solutions, and Legal Information.
*F	3786734	PURU	10/29/2012	Updated Pinouts: Updated Figure 3 (Updated caption only). Updated Ordering Information: Updated part numbers (Added two part numbers (CY22388FZXC and CY22388FZXCT)). Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *C to *D. spec 51-85118 – Changed revision from *C to *D. spec 001-30999 – Changed revision from *C to *D.

Document History Page (continued)

Document Title: CY22388/CY22389/CY22391, Factory Programmable Quad PLL Clock Generator with VCXO Document Number: 38-07734				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	4142797	CINM	10/01/2013	Updated to new template. Completing Sunset Review.
*H	4576237	CINM	11/21/2014	Updated Features: Updated output frequency range as 1 MHz to 166 MHz. Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *D to *E. spec 51-85118 – Changed revision from *D to *E.
*I	5475432	XHT	10/14/2016	Updated to new template. Completing Sunset Review.
*J	5995535	AESATMP8	12/15/2017	Updated logo and Copyright.

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