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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK3349

Silicon N Channel MOS FET
High Speed Switching

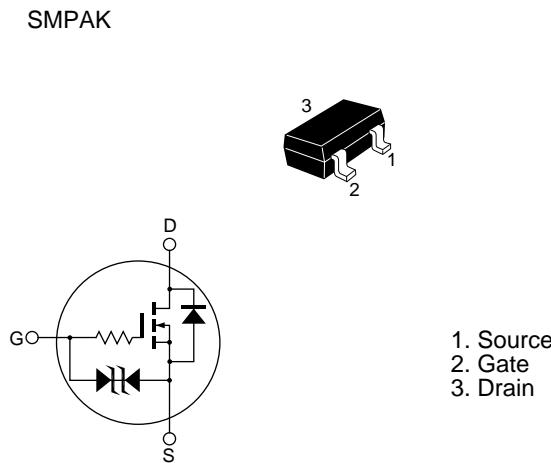
RENESAS

ADE-208-804 (Z)
1st.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 2.8 \Omega$ typ. (at $V_{GS} = 4$ V, $I_D = 25$ mA)
 $R_{DS} = 4.8 \Omega$ typ. (at $V_{GS} = 2.5$ V, $I_D = 10$ mA)
- 2.5 V gate drive device
- Small package (SMPAK)

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	20	V
Gate to source voltage	V _{GSS}	±10	V
Drain current	I _D	50	mA
Drain peak current	I _{D(pulse)} ^{Note1}	200	mA
Body-drain diode reverse drain current	I _{DR}	50	mA
Channel dissipation	P _{ch} ^{Note 2}	100	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value on the alumina ceramic board (12.5x20x0.7 mm)

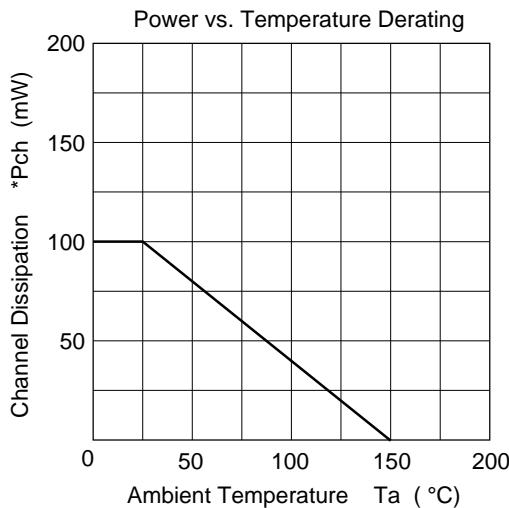
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	20	—	—	V	I _D = 100 μA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±10	—	—	V	I _G = ±100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±5	μA	V _{GS} = ±8 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 20 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	0.8	—	1.8	V	I _D = 10 μA, V _{DS} = 5 V
Static drain to source on state resistance	R _{DS(on)}	—	2.8	3.6	Ω	I _D = 25 mA, V _{GS} = 4 V ^{Note 3}
	R _{DS(on)}	—	4.8	7.2	Ω	I _D = 10 mA, V _{GS} = 2.5 V ^{Note 3}
Forward transfer admittance	y _{fs}	56	85	—	mS	I _D = 25 mA, V _{DS} = 10 V ^{Note 3}
Input capacitance	C _{iss}	—	6	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	7	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	1.2	—	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	—	120	—	ns	I _D = 25 mA, V _{GS} = 4 V
Rise time	t _r	—	450	—	ns	R _L = 400 Ω
Turn-off delay time	t _{d(off)}	—	480	—	ns	
Fall time	t _f	—	500	—	ns	

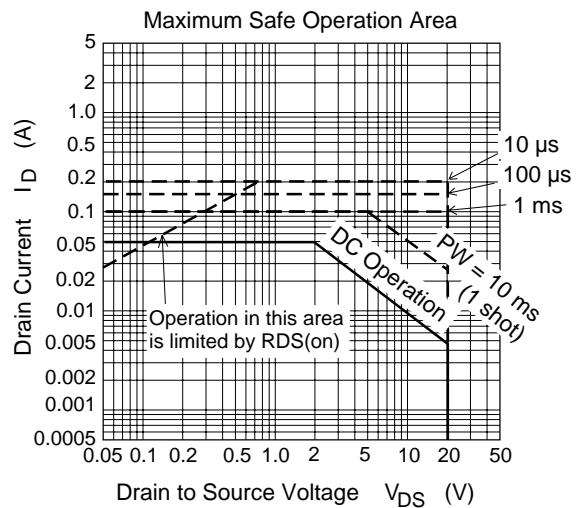
Note: 3. Pulse test

4. Marking is DN

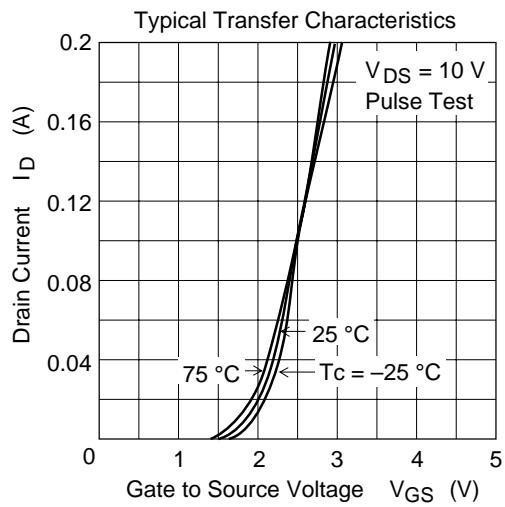
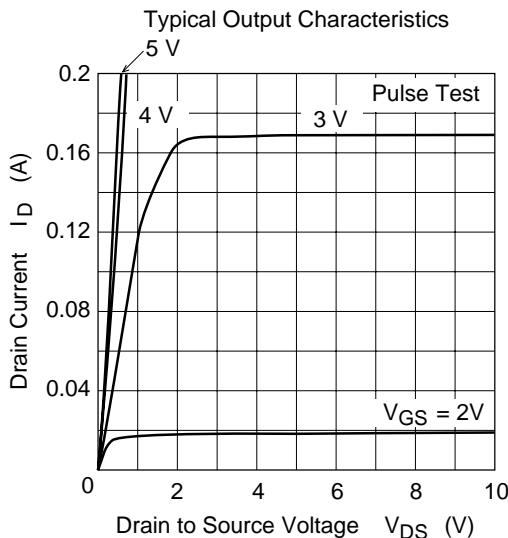
Main Characteristics

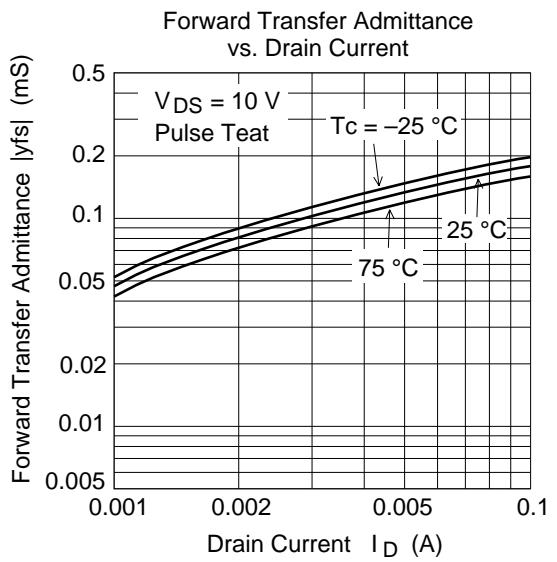
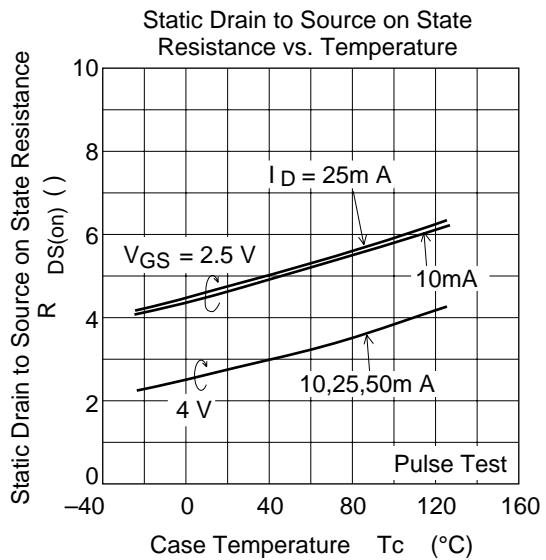
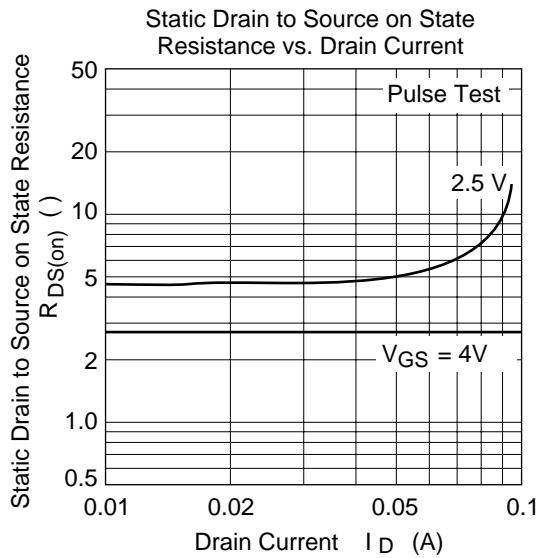
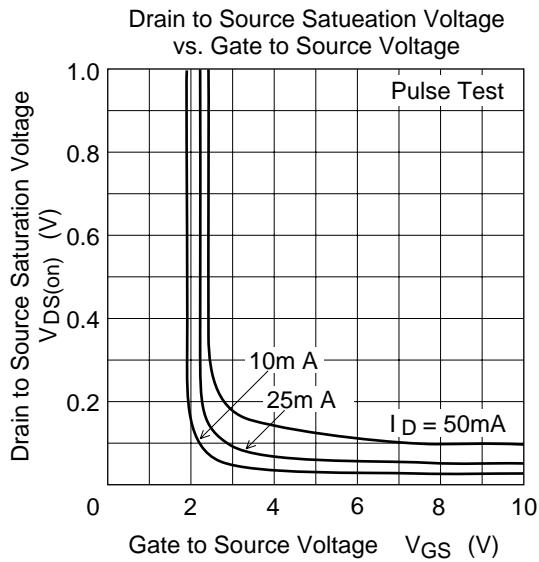


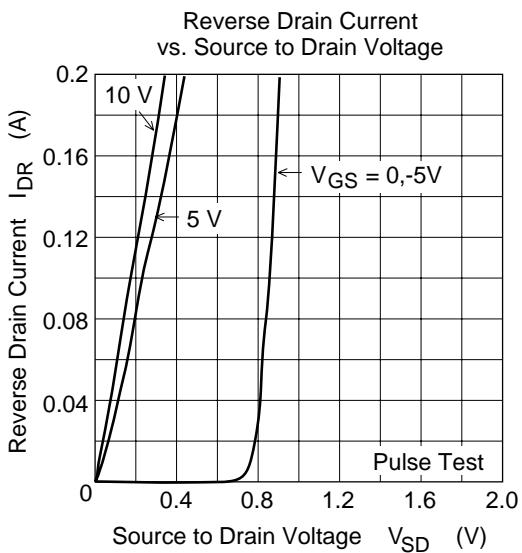
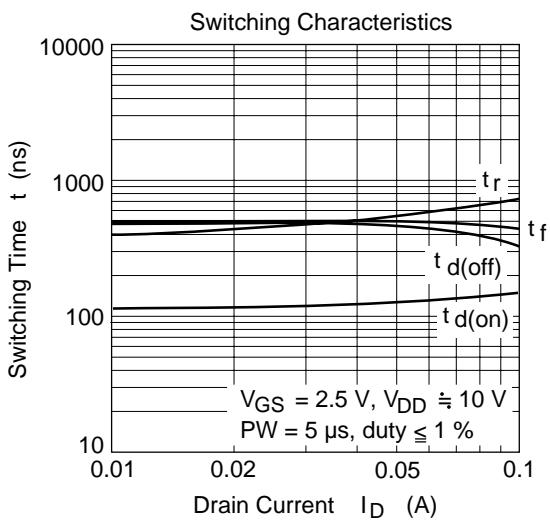
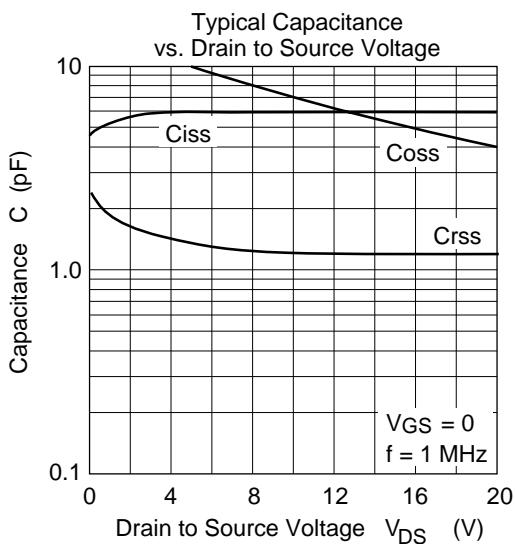
*Value on the alumina ceramic boad.(12.5x20x0.7mm)



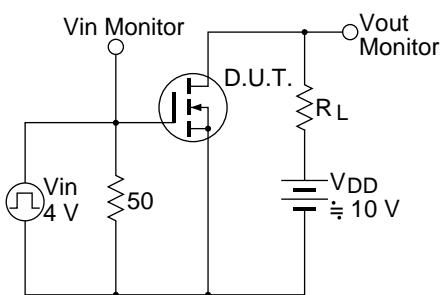
Value on the alumina ceramic boad.(12.5x20x0.7mm)



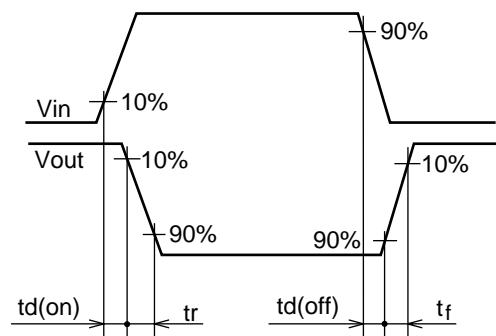




Switching Time Test Circuit



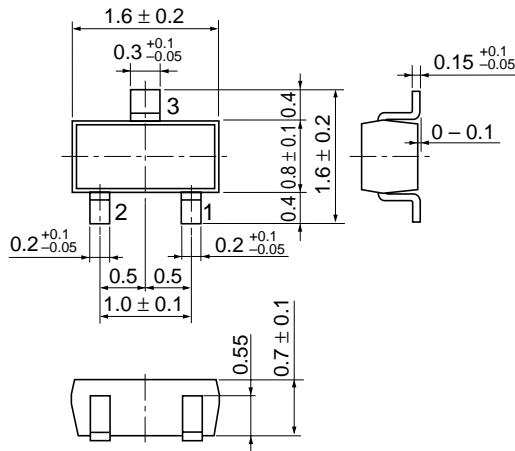
Waveforms



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SMPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.003 g

Cautions

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