TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M H 2 5 7 F K

Quad 2-Channel Multiplexer (3-State)

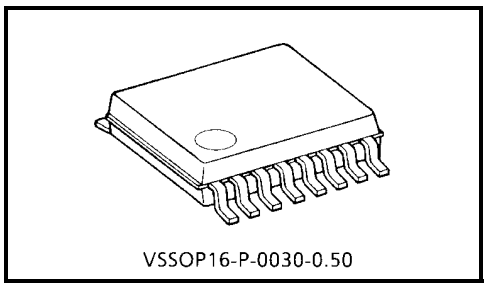
The TC7MH257FK is an advanced high speed CMOS multiplexer fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

It is composed of four independent 2-channel multiplexers with common SELECT and $\overline{\text{OUTPUTENABLE}}$ ($\overline{\text{OE}}$).

If $\overline{\text{OE}}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.



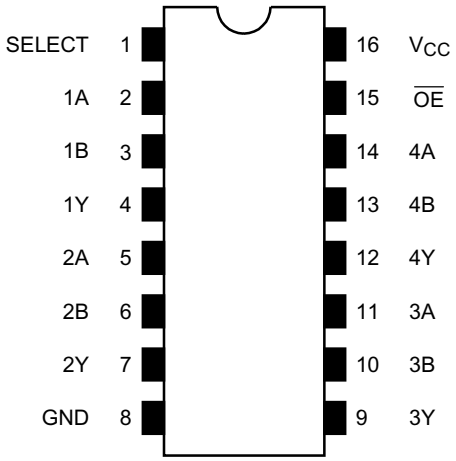
Weight: 0.02 g (typ.)

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

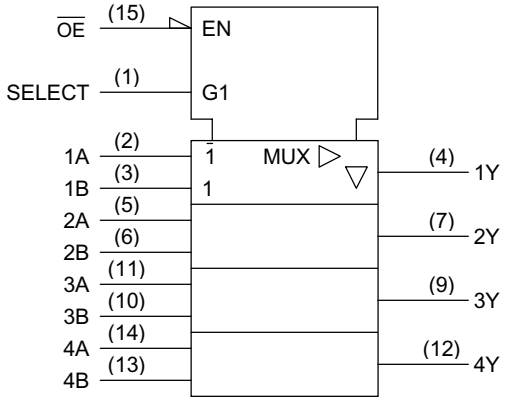
Features

- High speed: t_{pd} = 3.6 ns (typ.) (V_{CC} = 5 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2~5.5 V
- Low noise: V_{OLP} = 0.8 V (max)
- Pin and function compatible with 74ALS257

Pin Assignment (top view)



IEC Logic Symbol



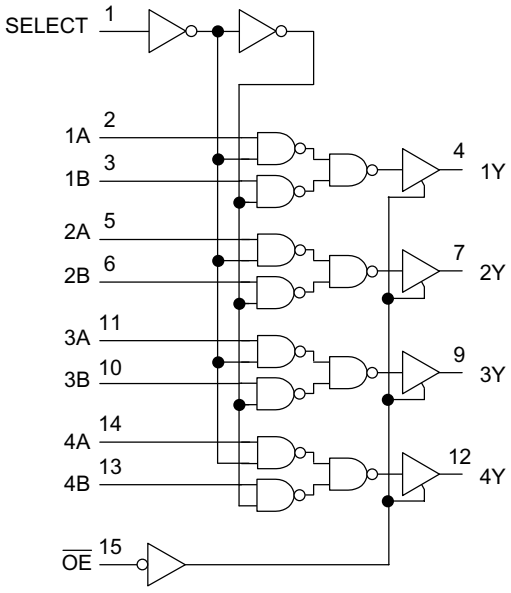
Truth Table

Inputs				Outputs
$\overline{OE}$	Select	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don’t care

Z: High impedance

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~7.0	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3 V)	ns/V
		0~20 (V_{CC} = 5 ± 0.5 V)	

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
					V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
					3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—	
	Low level	V_{IL}	—		2.0	—	—	0.50	—	0.50	
					3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$	
Output voltage	High level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				$I_{OH} = -4$ mA	3.0	2.58	—	—	2.48	—	
				$I_{OH} = -8$ mA	4.5	3.94	—	—	3.80	—	
	Low level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				$I_{OL} = 4$ mA	3.0	—	—	0.36	—	0.44	
				$I_{OL} = 8$ mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current		I_{IN}	$V_{IN} = 5.5$ V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (Input: $t_r = t_f = 3$ ns)

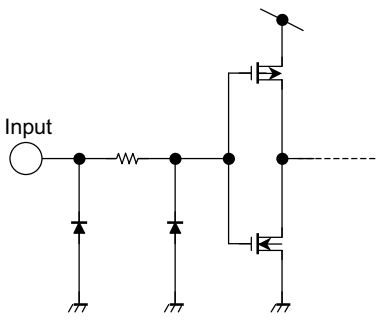
Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (A, B-Y)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	5.8	9.3	1.0	11.0	ns
				50	—	8.3	12.8	1.0	14.5	
			5.0 ± 0.5	15	—	3.6	5.9	1.0	7.0	
				50	—	5.1	7.9	1.0	9.0	
Propagation delay time (SELECT-Y)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.0	11.0	1.0	13.0	ns
				50	—	9.5	14.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.0	6.8	1.0	8.0	
				50	—	5.5	8.8	1.0	10.0	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	3.3 ± 0.3	15	—	6.7	10.5	1.0	12.5	ns
				50	—	9.2	14.0	1.0	16.0	
			5.0 ± 0.5	15	—	3.6	6.8	1.0	8.0	
				50	—	5.1	8.8	1.0	10.0	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	3.3 ± 0.3	50	—	8.6	12.0	1.0	13.5	ns
			5.0 ± 0.5	50	—	5.7	7.9	1.0	9.0	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	6	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note)			—	23	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per bit)

Noise Characteristics (Input: $t_r = t_f = 3$ ns)

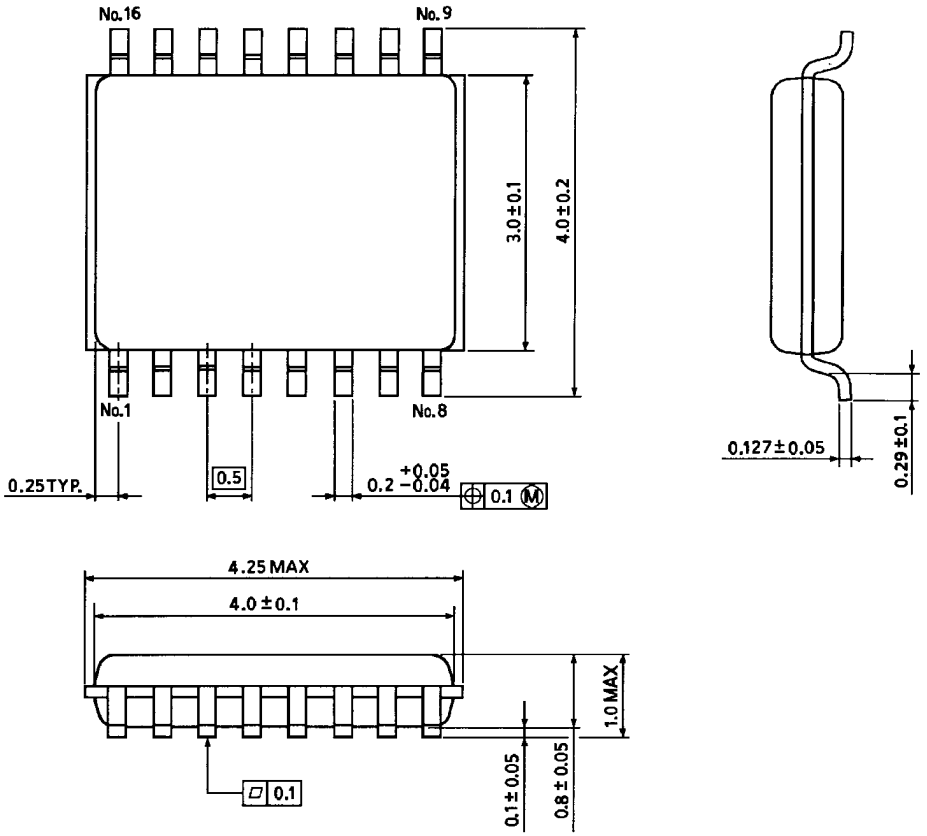
Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.3	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.3	−0.8	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit



Package Dimensions

VSSOP16-P-0030-0.50 Unit : mm



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