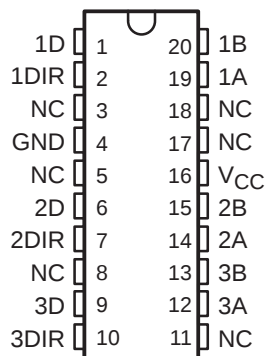


SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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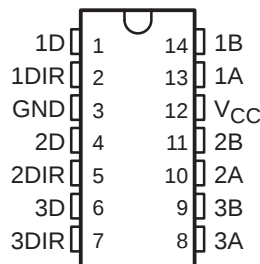
- Three Bidirectional Transceivers
- Driver Meets or Exceeds ANSI Standard EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . . 12 k Ω Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operate From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Feature Independent Direction Controls for Each Channel

DW PACKAGE
(TOP VIEW)



NC – No internal connection

J PACKAGE
(TOP VIEW)



description

The SN75ALS170 and SN75ALS170A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the driver and receiver meet ITU Recommendation V.11. The SN75ALS170A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS170 and SN75ALS170A operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 and the SN75ALS170A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SKEW LIMIT	PART NUMBER	
10 ns	SN75ALS170DW	SN75ALS170J
5 ns	SN75ALS170ADW	



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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Function Tables

EACH DRIVER

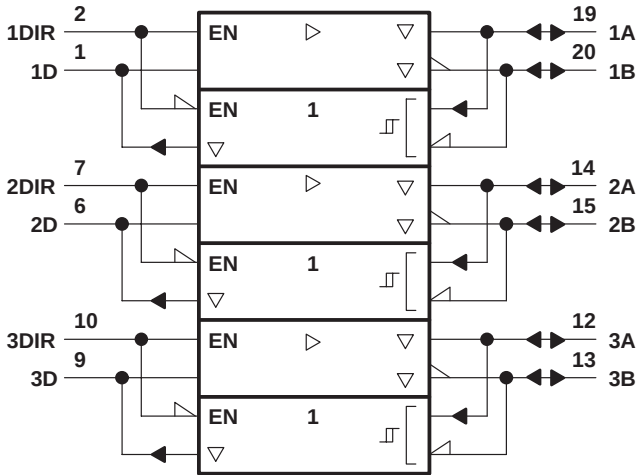
INPUT D	DIR	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3\text{ V}$	L	H
$-0.3\text{ V} < V_{ID} < 0.3\text{ V}$	L	?
$V_{ID} \leq -0.3\text{ V}$	L	L
X	H	Z
Open	L	H

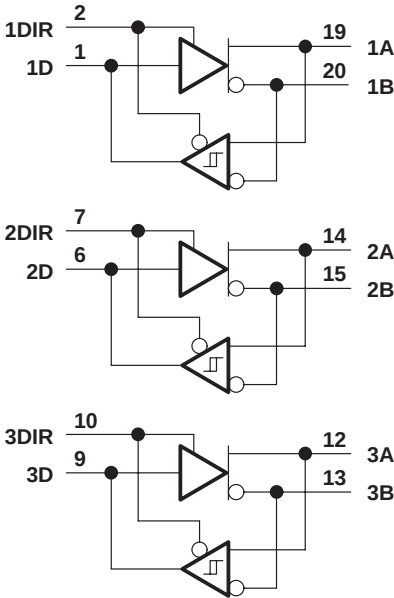
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

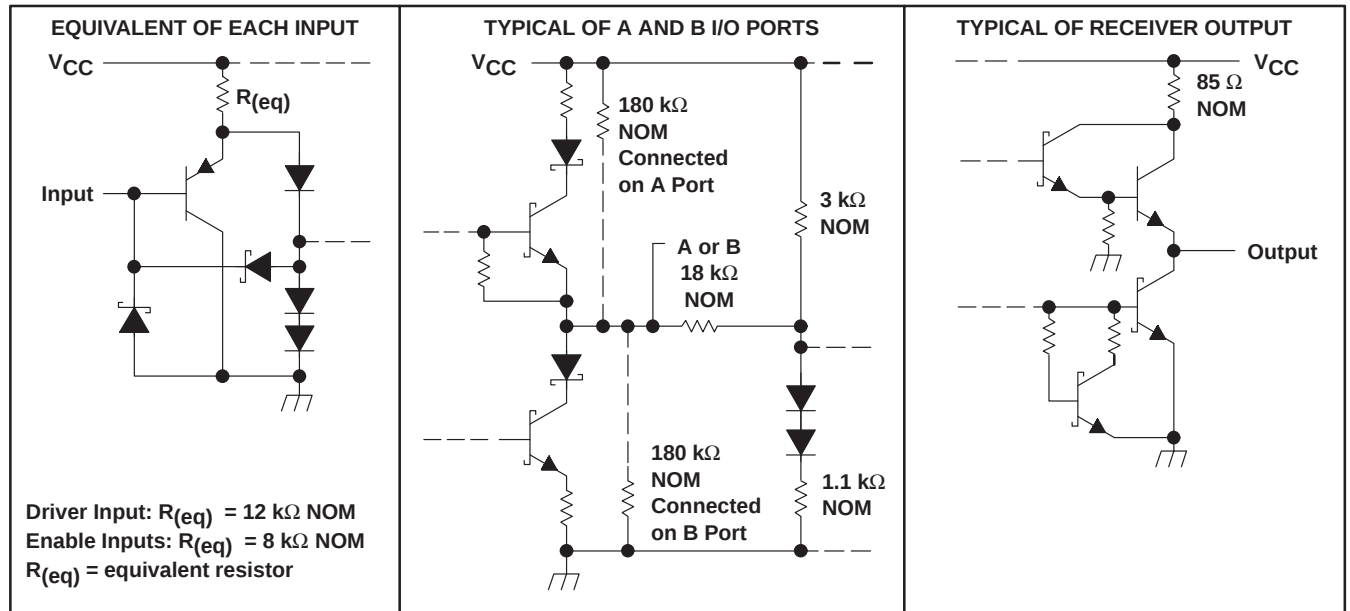


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–7 V to 12 V
Enable input voltage, V_I	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

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recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V _I or V _{IC}		12			V
		−7			
High-level input voltage, V _{IH}	D, DIR	2			V
Low-level input voltage, V _{IL}	D, DIR	0.8			V
Differential input voltage, V _{ID} (see Note 2)		±12			V
High-level output current, I _{OH}	Driver	−60			mA
	Receiver	−400			μA
Low-level output current, I _{OL}	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T _A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = −19 mA				−1.5	V
V _O	Output voltage	I _O = 0		0		6	V
V _{OH}	High-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = −55 mA	2.7			V
V _{OL}	Low-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 55 mA			1.7	V
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 1	1/2V _{OD1} or 2 ^S			V
		R _L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V _{OD3}	Differential output voltage	V _{test} = −7 V to 12 V, See Figure 2		1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 540 Ω or 100 Ω, See Figure 1				±0.2	V
V _{OC}	Common-mode output voltage					3	V
						−1	
Δ V _{OC}	Change in magnitude of common-mode output voltage¶						
I _O	Output current	Output disabled, See Note 3	V _O = 12 V			1	mA
			V _O = −7 V			−0.8	
I _{IH}	High-level input current	V _I = 2.4 V				20	μA
I _{IL}	Low-level input current	V _I = 0.4 V				−400	μA
I _{OS}	Short-circuit output current	V _O = −6 V				−250	mA
		V _O = 0				−150	
		V _O = V _{CC}				250	
		V _O = 8 V				250	
I _{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

¶ $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT	
t _d (OD)	Differential output delay time	ALS170	R _L = 54 Ω, T _A =25°C, C _L = 50 pF, See Figure 3	3	8	13	ns	
	ALS170A	5.5		8	10.5			
	ALS170	R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF, See Figure 4	R _{L2} = 75 Ω, T _A =25°C,	3	8	13		
	ALS170A			5.5	8	10.5		
t _{sk} (p)	Pulse skew [‡]	R _L = 54 Ω, See Figure 3		C _L = 50 pF,	1	5	ns	
		R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF,		R _{L2} = 75 Ω, See Figure 4	1	5	ns	
t _{sk} (lim)	Skew limit [§]	ALS170	R _L = 54 Ω, See Figure 3	C _L = 50 pF,	10		ns	
		ALS170A			5			
		ALS170	R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF,	R _{L2} = 75 Ω, See Figure 4	10			
		ALS170A			5			
t _t (OD)	Differential-output transition time	R _L = 54 Ω, See Figure 3		C _L = 50 pF,	3	8	13	ns
		R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF,		R _{L2} = 75 Ω, See Figure 4	3	8	13	

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

[‡] Pulse skew is defined as the $|t_{d(ODH)} - t_{d(ODL)}|$ of each channel.

[§] Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{0a}, V_{0b}	V_{0a}, V_{0b}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7$ V,	$I_O = -0.4$ mA			0.3	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5$ V,	$I_O = 8$ mA	$-0.3^{\ddagger}$			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA				-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 300$ mV, See Figure 5	$I_{OH} = -400$ μ A,	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -300$ mV, See Figure 5	$I_{OL} = 8$ mA,			0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 2.4$ V				20	align="center"> μ A
		$V_O = 0.4$ V				-400	
I_I	Line input current	Other input = 0, See Note 4	$V_I = 12$ V			1	align="center">mA
			$V_I = -7$ V			-0.8	
I_{IH}	High-level enable-input current	$V_{IH} = 2.7$ V				20	μ A
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4$ V				-100	μ A
r_I	Input resistance			12			k Ω
I_{OS}	Short-circuit output current	$V_{ID} = 300$ mV,	$V_O = 0$	-15		-85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	align="center">mA
			Outputs disabled		57	78	

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ALS170	$V_{ID} = -1.5$ V to 1.5 V, $C_L = 15$ pF, $T_A = 25^\circ\text{C}$, See Figure 6	9		19	align="center">ns
		ALS170A		11.5		16.5	
t_{PHL}	Propagation delay time, high-to-low-level output	ALS170		9		19	align="center">ns
		ALS170A		11.5		16.5	
$t_{sk(p)}$	Pulse skew [§]	ALS170	$V_{ID} = -1.5$ V to 1.5 V, $C_L = 15$ pF, $T_A = 25^\circ\text{C}$, See Figure 6		2	6	align="center">ns
		ALS170A				5	
$t_{sk(lim)}$	Skew limit [¶]	ALS170				10	align="center">ns
		ALS170A				5	

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

[§] Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

[¶] Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION

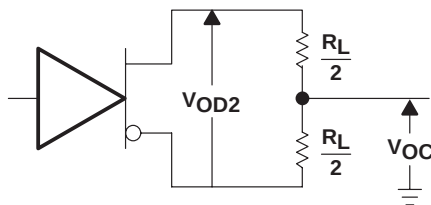


Figure 1. Driver V_{OD} and V_{OC}

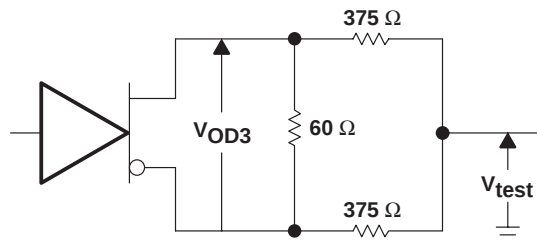
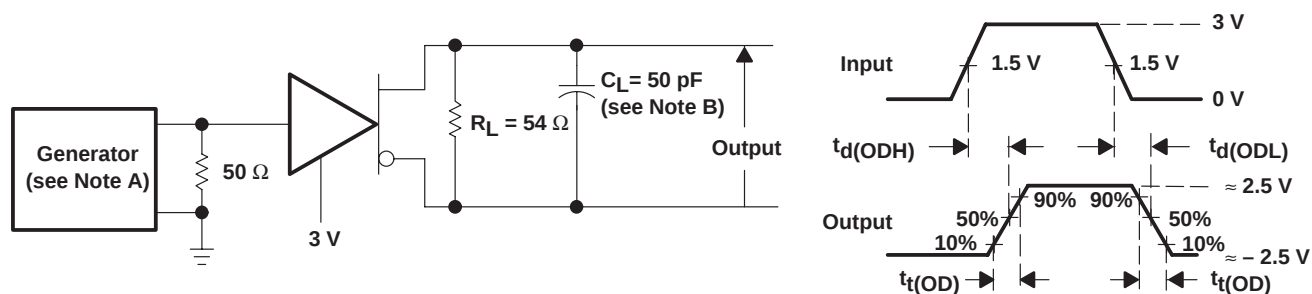


Figure 2. Driver V_{OD3}



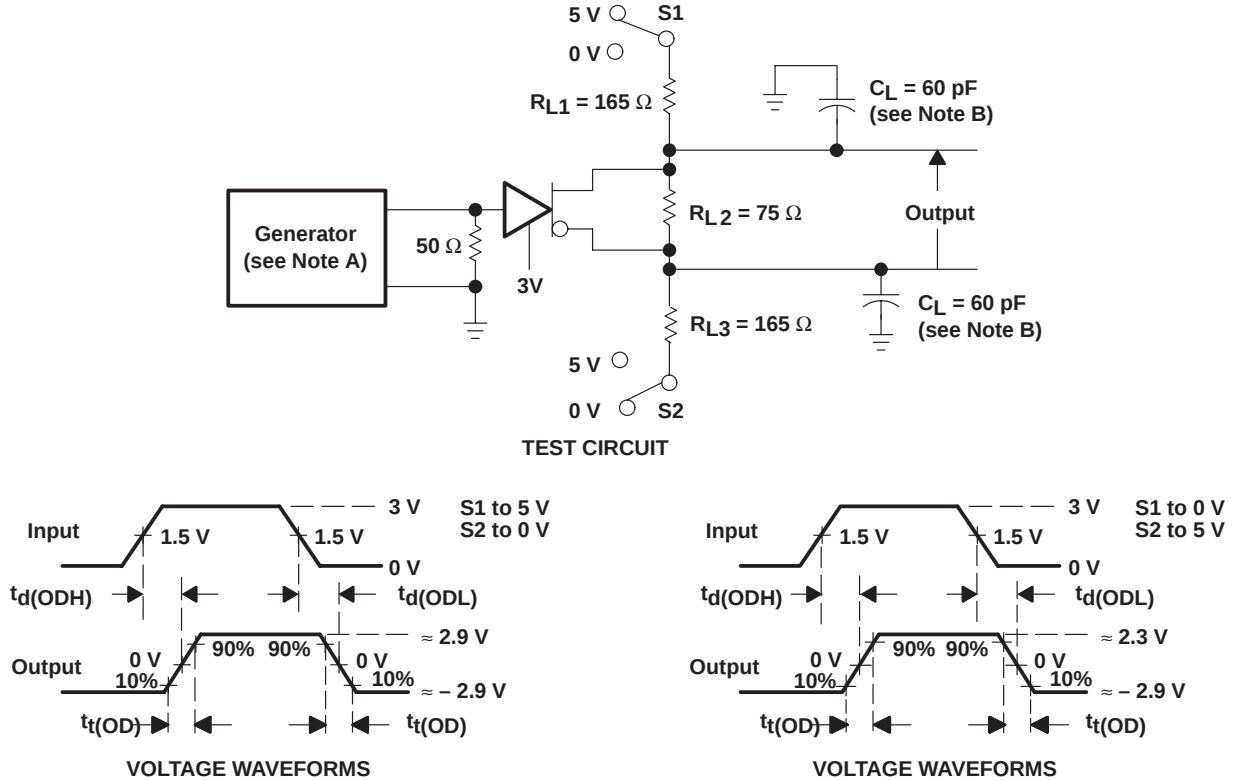
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

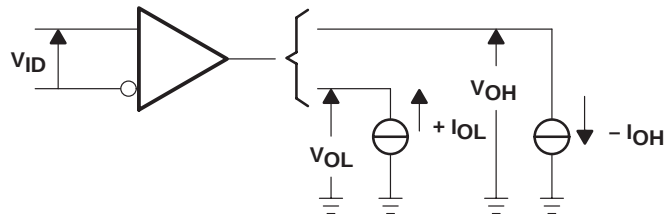
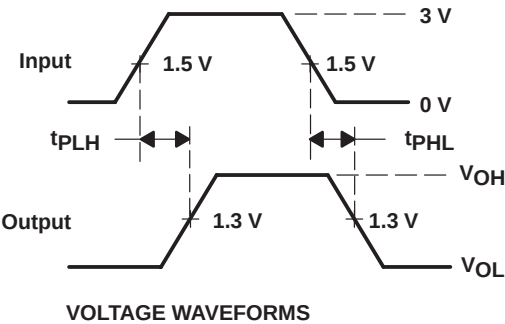
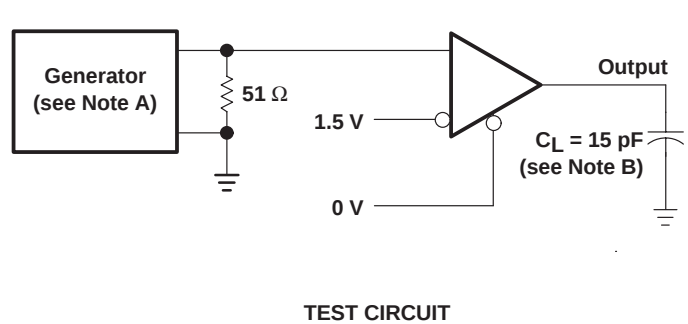


Figure 5. Receiver V_{OH} and V_{OL}

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

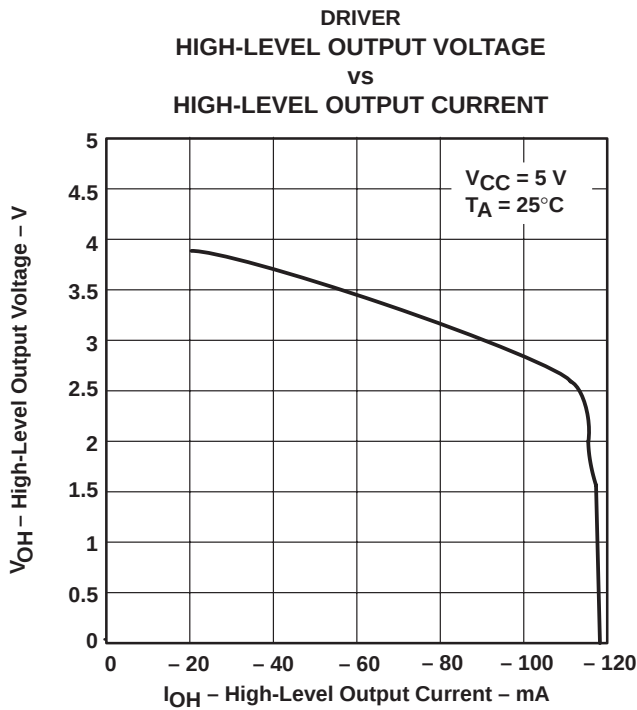


Figure 7

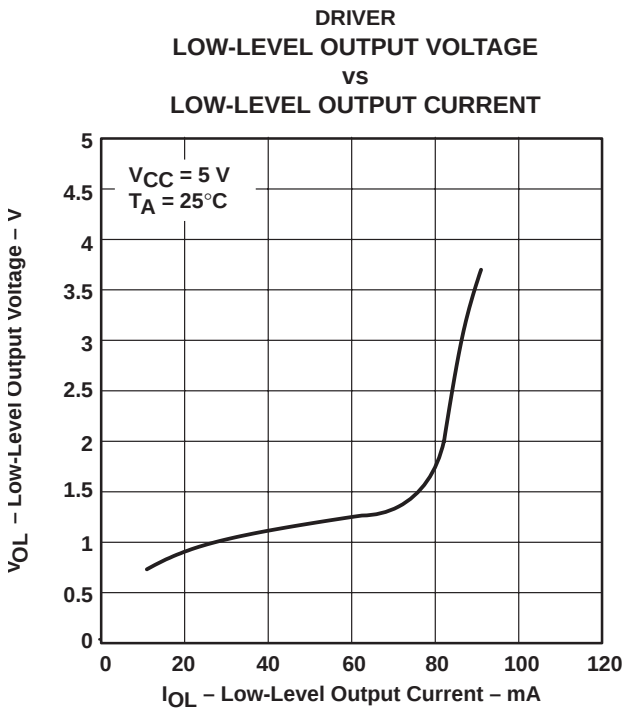


Figure 8

TYPICAL CHARACTERISTICS

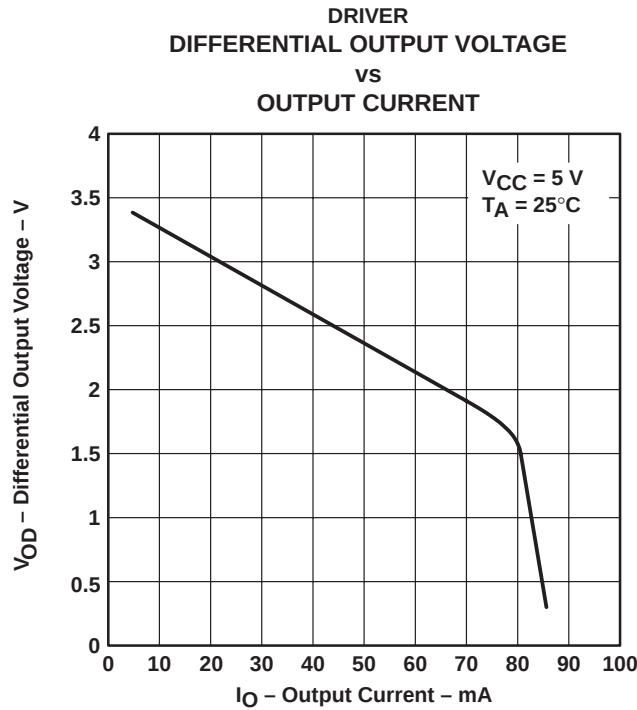


Figure 9

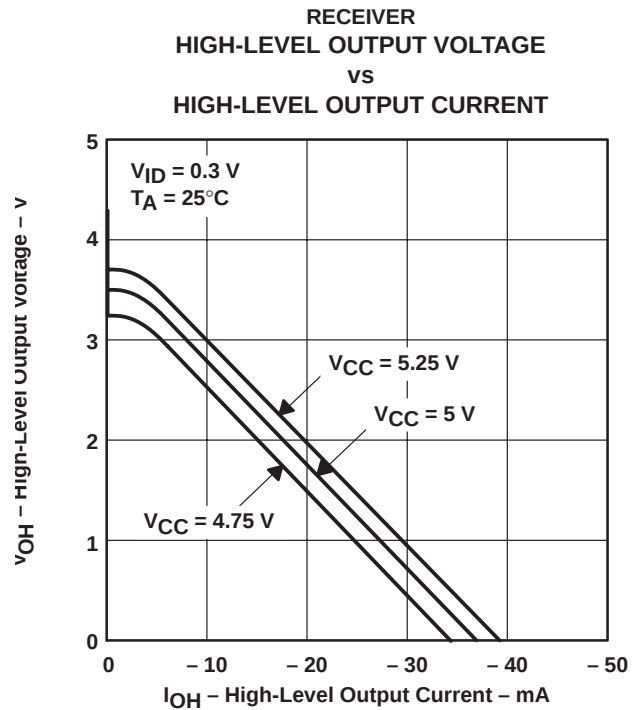


Figure 10

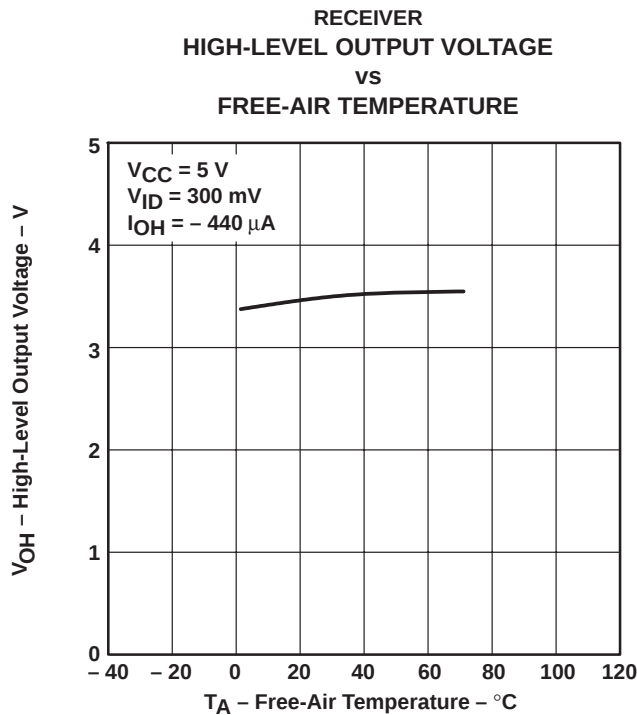


Figure 11

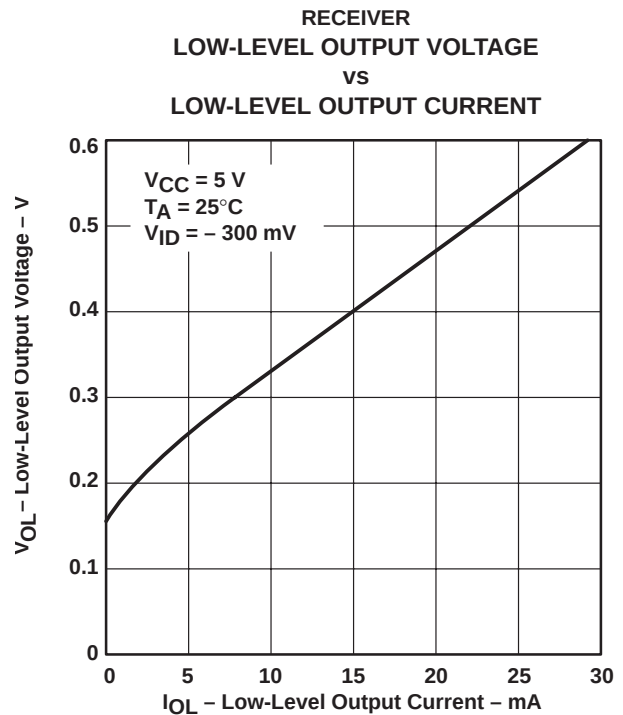


Figure 12

SN75ALS170, SN75ALS170A
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TYPICAL CHARACTERISTICS

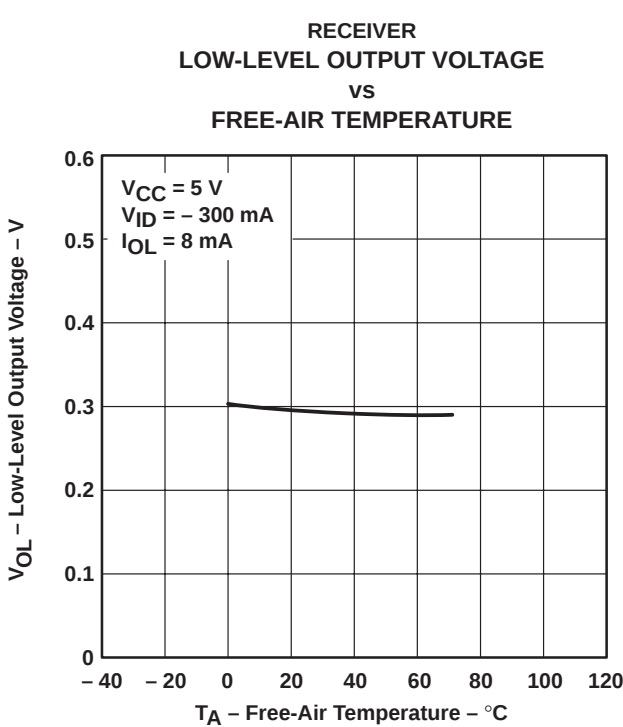


Figure 13

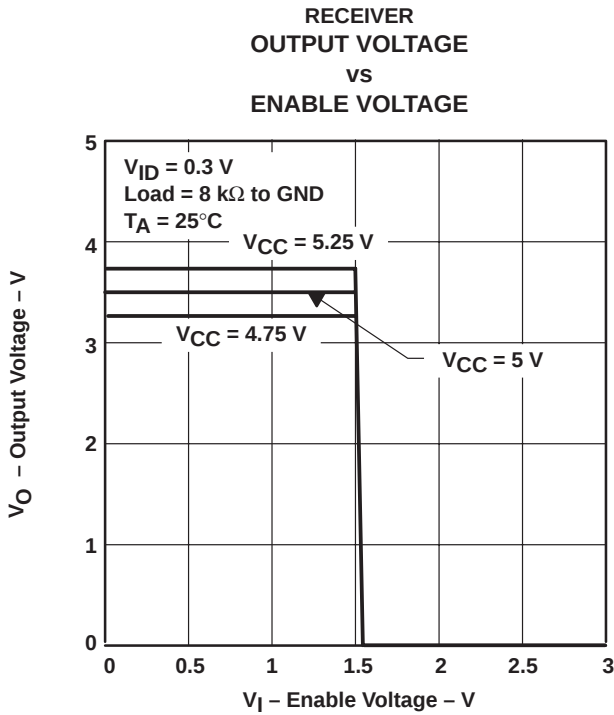


Figure 14

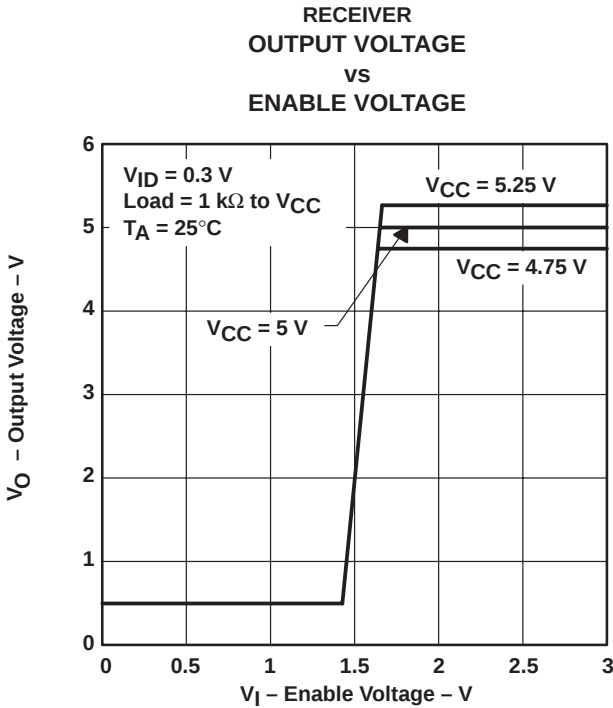
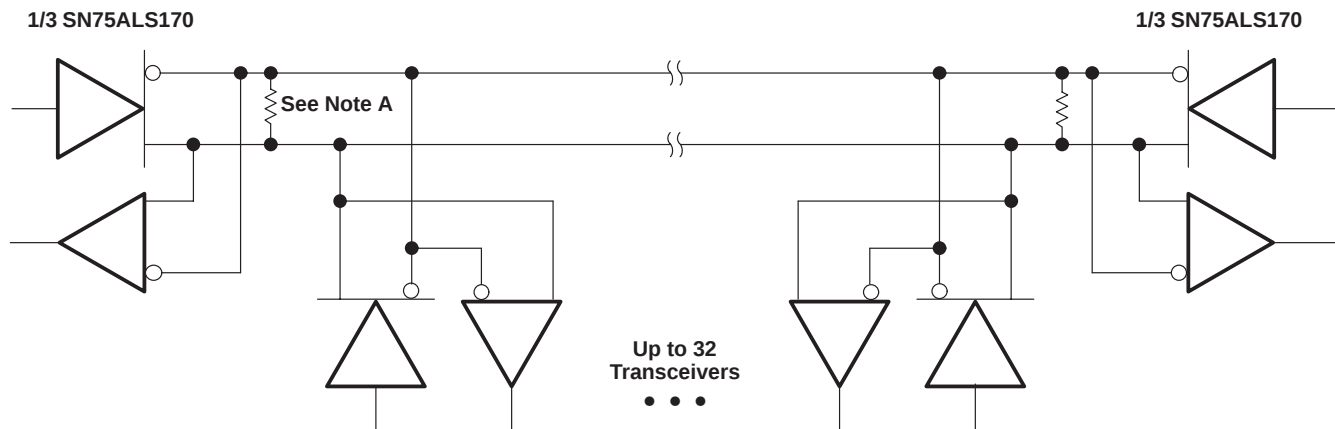


Figure 15

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

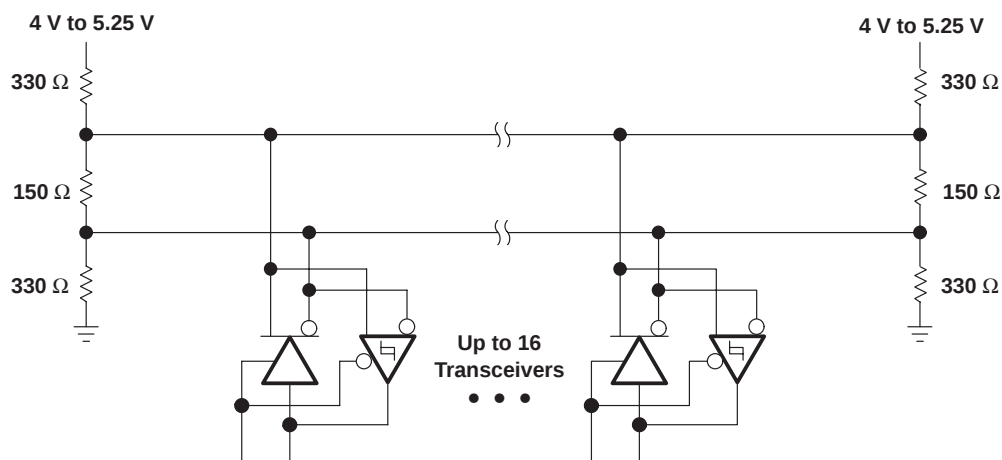


Figure 17. Typical Differential SCSI Application Circuit

SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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APPLICATION INFORMATION

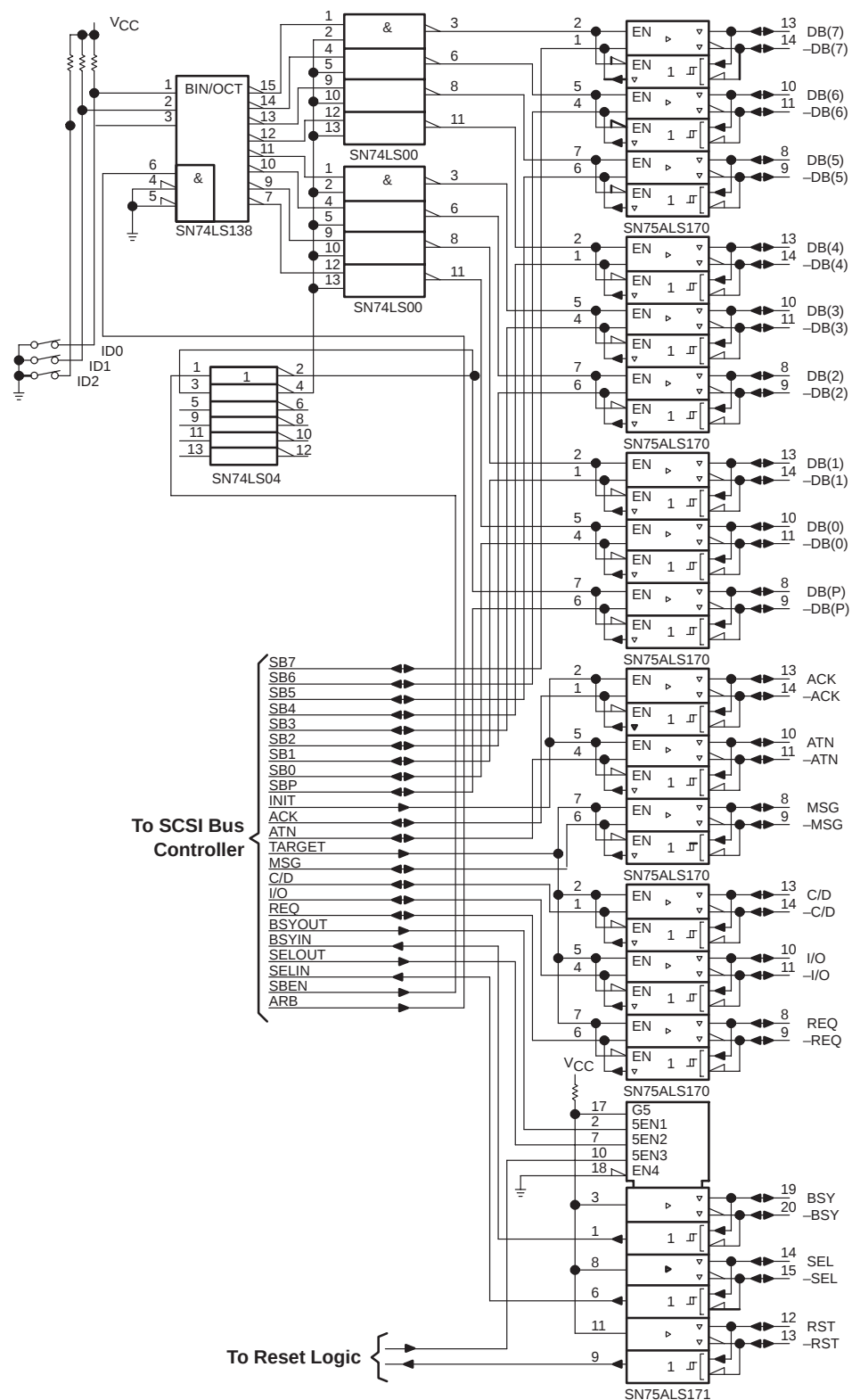


Figure 18. Typical Differential SCSI Bus Interface Implementation

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS170ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A
SN75ALS170ADW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A
SN75ALS170ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A
SN75ALS170ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A
SN75ALS170DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170
SN75ALS170DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170
SN75ALS170DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170
SN75ALS170DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS170ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS170DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS170ADWR	SOIC	DW	20	2000	350.0	350.0	43.0
SN75ALS170DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

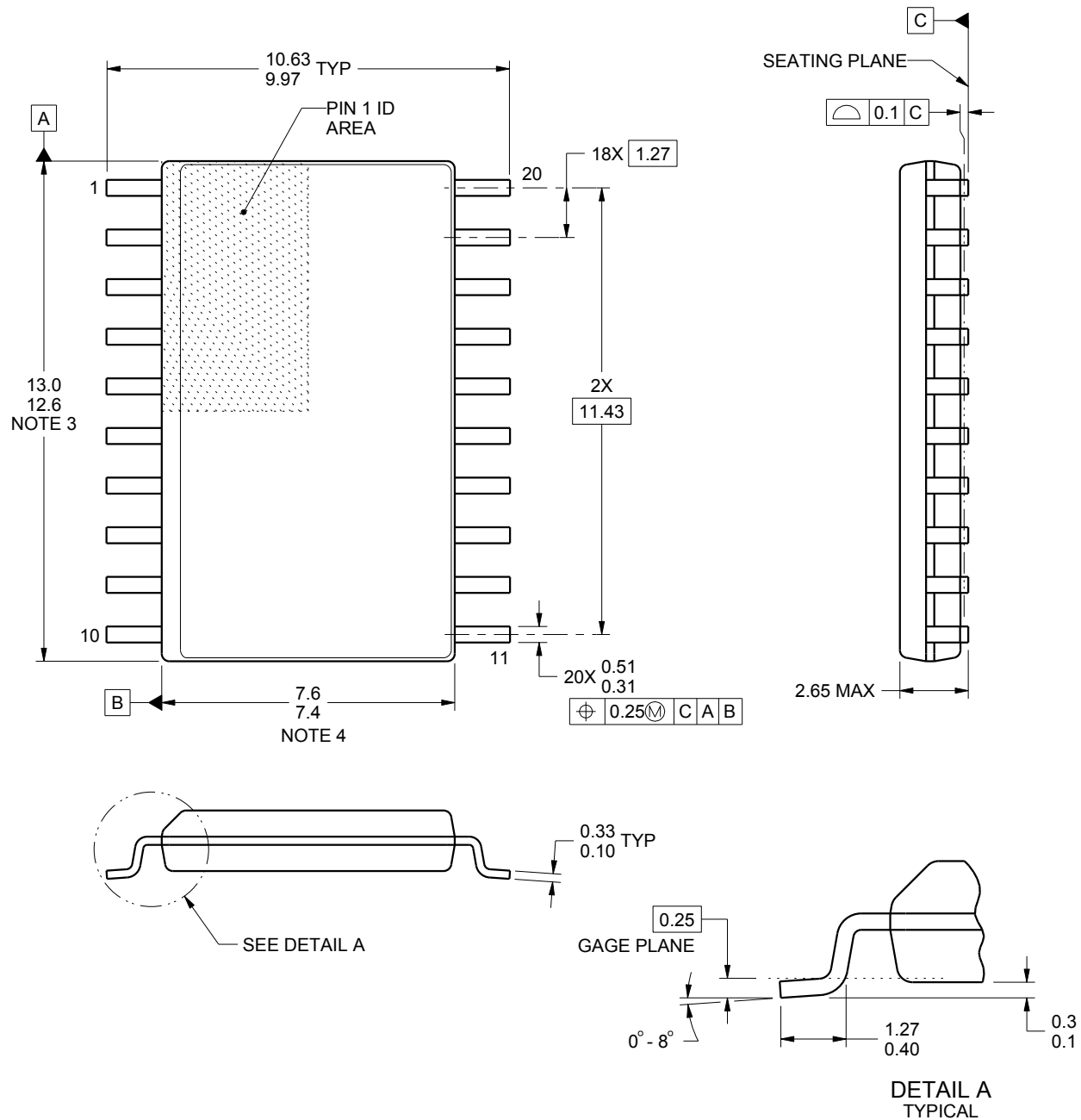
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS170ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS170ADW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS170DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS170DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

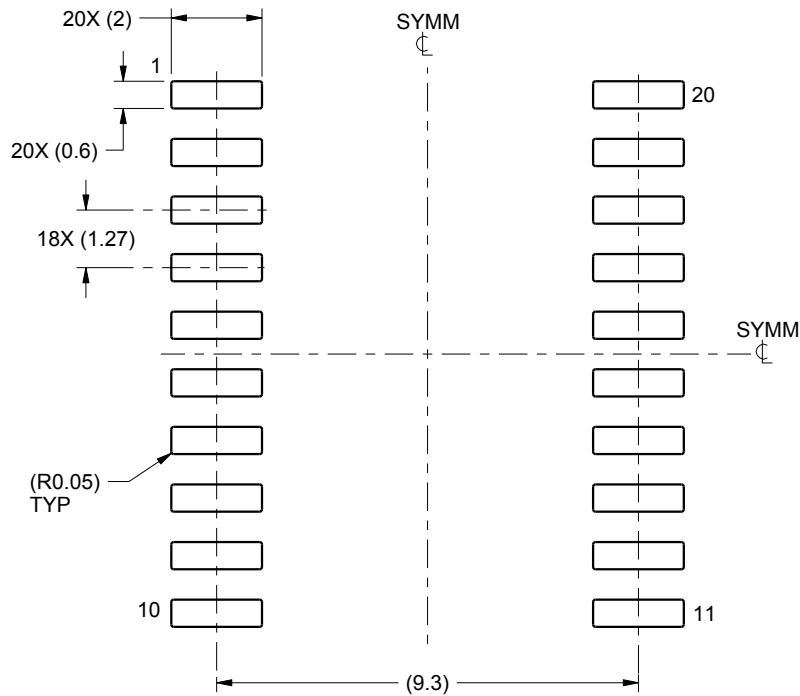
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

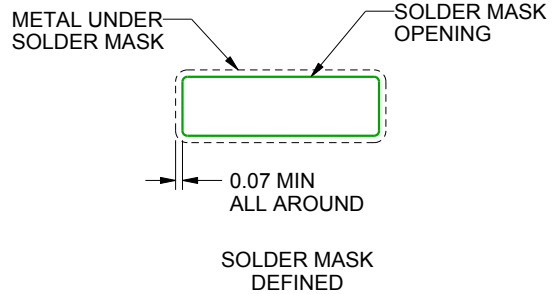
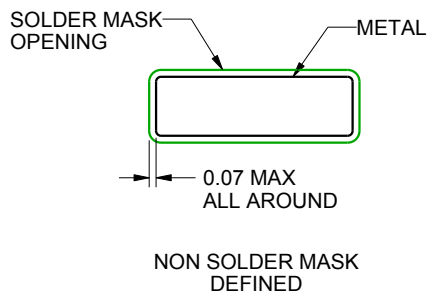
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

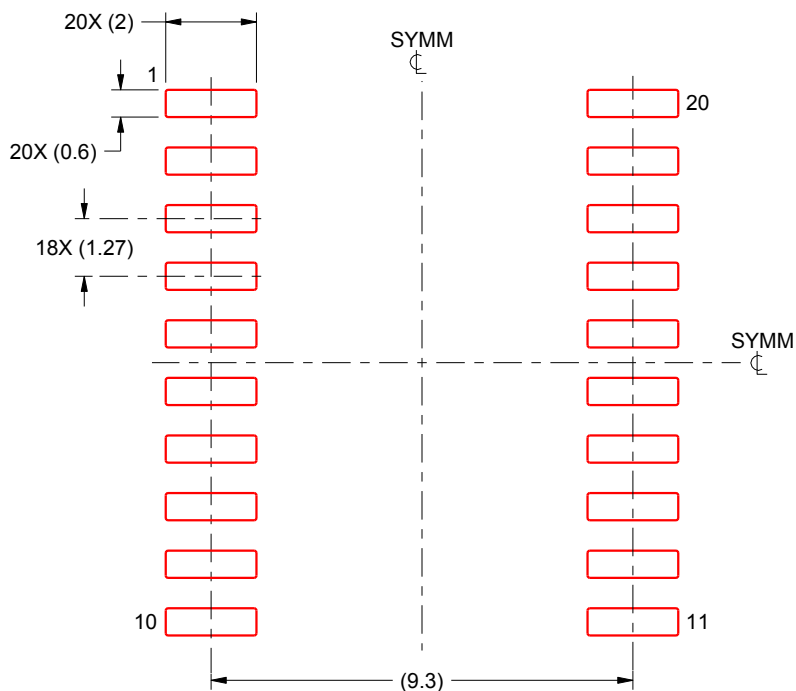
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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