NBSG16

2.5V/3.3V SiGe Differential Receiver/Driver with RSECL* Outputs

*Reduced Swing ECL

The SG16 is a Silicon Germanium differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), HSTL, GTL, TTL, CMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used for single–ended NECL or PECL inputs and the V_{MM} pin is used for CMOS inputs. For all single–ended input conditions, the unused differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Frequency > 12 GHz Typical
- 120 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.465 V
- RSECL Output Level (400 mV Peak–to–Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- V_{BB} and V_{MM} Reference Voltage Output

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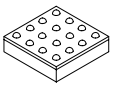
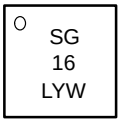


FCBGA–16
BA SUFFIX
CASE 489

MARKING DIAGRAM*



L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG16BA	4x4 mm FCBGA–16	810 Units/Tray
NBSG16BAR2	4x4 mm FCBGA–16	2500/Tape & Reel
NBSG16BA100	4x4 mm FCBGA–16	100 Units/Tray
NBSG16BA500R2	4x4 mm FCBGA–16	500/Tape & Reel

Board	Description
SG16EVB	NBSG16BA Evaluation Board

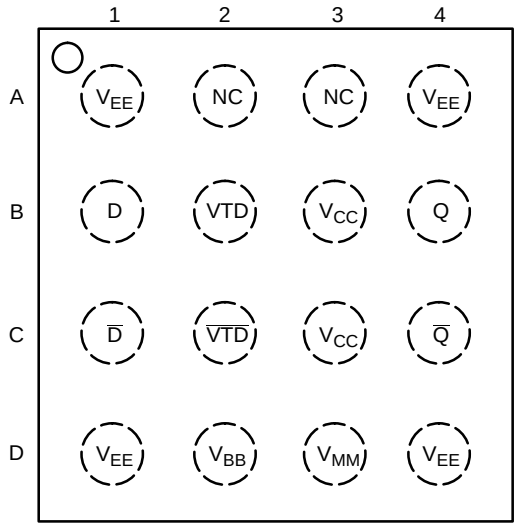


Figure 1. Pinout (Top View)

NOTE: The NC pins are electrically connected to the die and MUST be left open or both pins can be tied to V_{CC}.

PIN DESCRIPTION

PIN	FUNCTION
D*, $\overline{D}$**	ECL, HSTL, GTL, TTL, CMOS. CML, LVDS compatible inputs
Q, $\overline{Q}$	RSECL Data Outputs
VTD, $\overline{VTD}$	50 Ω Internal Input Termination Resistor
V_{MM}	CMOS Reference Voltage Output, (V_{CC}–V_{EE})/2
V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* Pin will default low when left open.
** Pin will default to a slightly higher potential than D when both are left open.

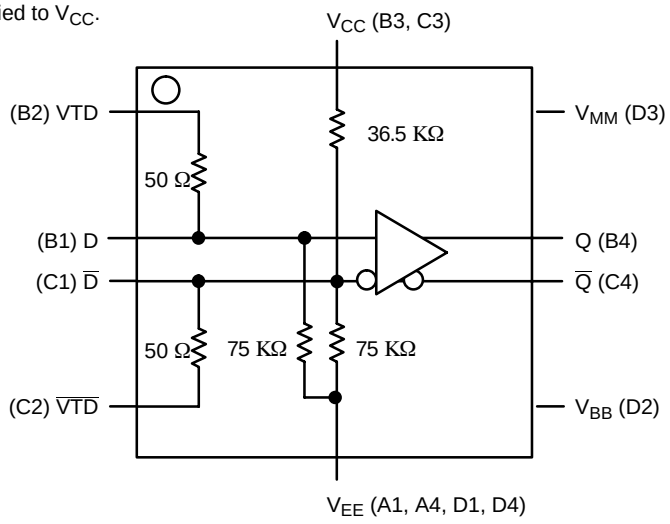


Figure 2. Logic Diagram

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ together
AC–COUPLED	Bias VTD and $\overline{VTD}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (D, $\overline{D}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating		UL 94 V–0 @ 0.125 in
Oxygen Index		28 to 34
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		–3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 –3.6	V V
I_{out}	Output Current	Continuous Surge		25 50	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	1S2P (Note 3)	16 FCBGA	5	°C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard multilayer board – 1S2P (1 signal, 2 power)

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V_{OH}	Output HIGH Voltage (Note 5)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V_{PP}	Output P–P Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 6)	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 6)	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	CMOS Output Voltage Reference $V_{CC}/2$	1200	1250	1400	1200	1250	1400	1200	1250	1400	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –0.965 V.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 8)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V_{OH}	Output HIGH Voltage (Note 9)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V_{PP}	Output P–P Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 10)	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 10)	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	CMOS Output Voltage Reference $V_{CC}/2$	1600	1650	1800	1600	1650	1800	1600	1650	1800	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.
9. All loading with 50 ohms to V_{CC}–2.0 volts.
10. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 12)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V_{OH}	Output HIGH Voltage (Note 13)	–1050	–970	–925	–975	–935	–900	–950	–910	–875	mV
V_{PP}	Output P–P Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 14)	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} – 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 14)	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V_{EE}	V_{CC} – 1.4*	V_{THR} – 75 mV	V
V_{BB}	NECL Output Voltage Reference	–1420	–1360	–1300	–1420	–1360	–1300	–1420	–1360	–1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 15)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
V_{MM}	CMOS Output Voltage Reference (Note 16)	V_{MMT} – 50	V_{MMT}	V_{MMT} + 150	V_{MMT} – 50	V_{MMT}	V_{MMT} + 150	V_{MMT} – 50	V_{MMT}	V_{MMT} + 150	mV
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC}.
13. All loading with 50 ohms to V_{CC} –2.0 volts.
14. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
15. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
16. V_{MM} typical = $|V_{CC} – V_{EE}|/2 + V_{EE} = V_{MMT}$

*Typicals used for testing purposes.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3. F_{max}/JITTER) (Note 17)	10.709	> 12		10.709	> 12		10.709	> 12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	130	100	120	140	105	125	145	ps
t_{SKEW}	Duty Cycle Skew (Note 18)		3	15		3	15		3	15	ps
t_{JITTER}	Cycle–to–Cycle Jitter (RMS) (See Figure 3. F_{max}/JITTER) (Note 17)		0.3	< 1		0.3	< 1		0.3	< 1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 19)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	30	45	75	20	40	65	20	40	65	ps

17. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.
18. See Figure 5. $t_{skew} = |t_{PLH} – t_{PHL}|$ for a nominal 50% differential clock input waveform.
19. $V_{INPP(max)}$ cannot exceed $V_{CC} – V_{EE}$

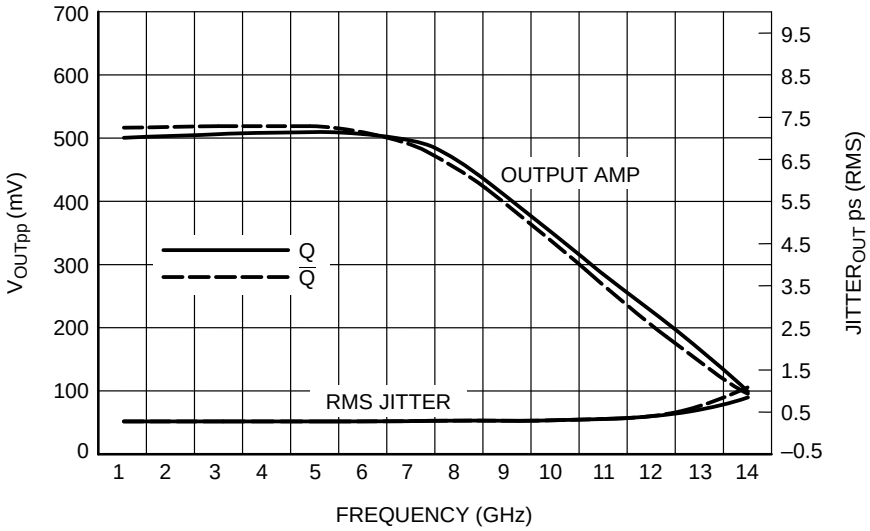
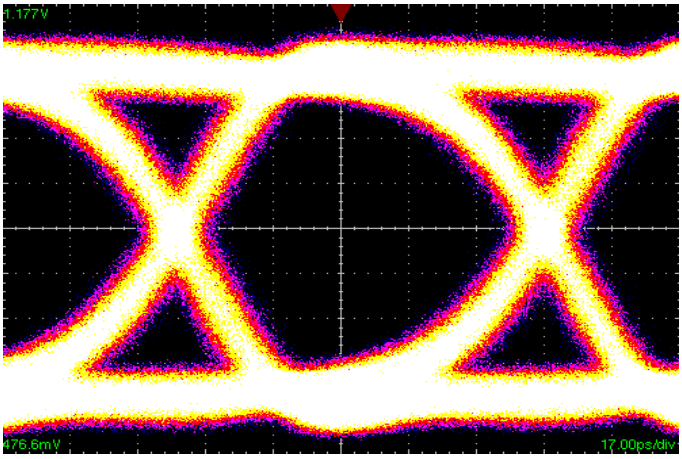


Figure 3. F_{max}/Jitter



X = 17ps/Div Y = 70 mV/Div

Figure 4. 10.709 Gb/s Diagram (3.0 V, 25°C)

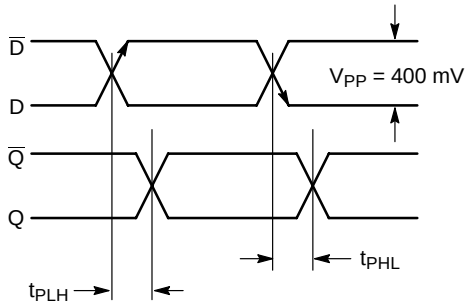


Figure 5. AC Reference Measurement

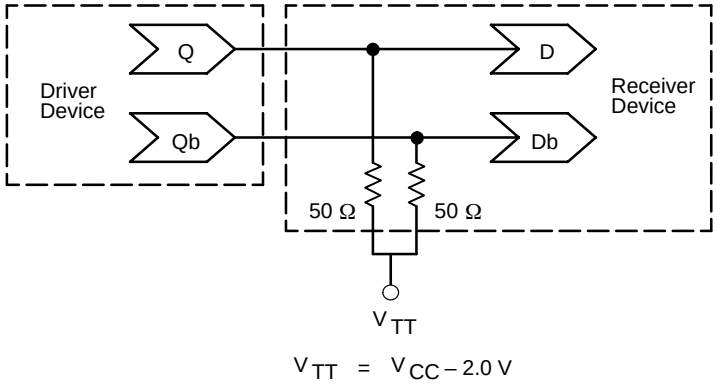
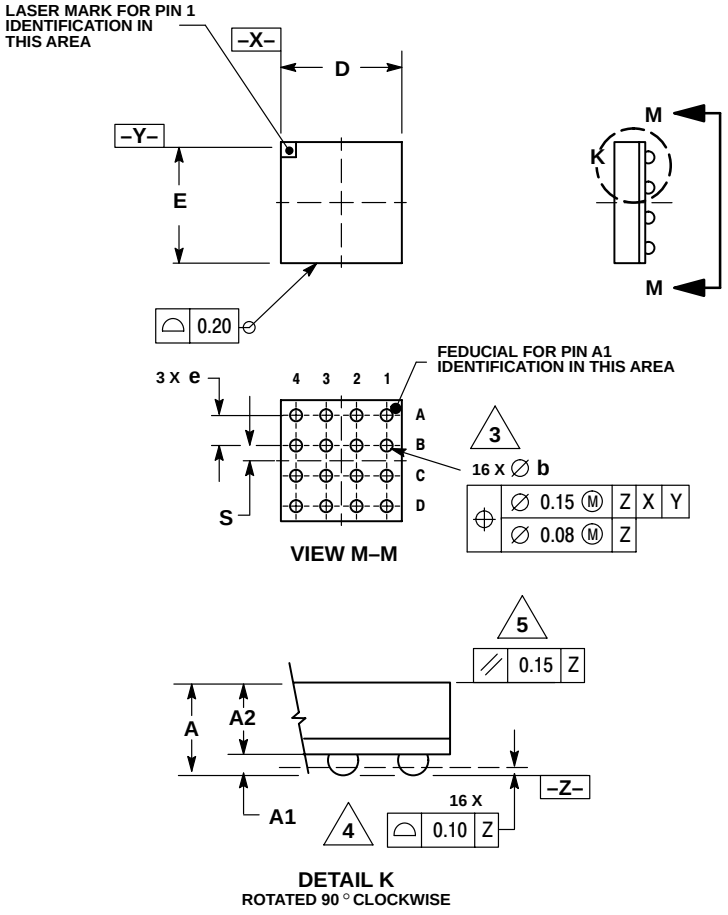


Figure 6. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA–16
BA SUFFIX
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

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