

### FEATURES

- Fixed Output Voltages:  $-3V$ ,  $-5V$  or Low Noise  $V_{IN}$  to  $-V_{IN}$  Inverted Output
- $\pm 4\%$  Output Voltage Accuracy
- Low Quiescent Current:  $25\mu A$
- 100mA Output Current Capability
- 3V to 5.5V Operating Voltage Range (LTC1983-3)
- 2.3V to 5.5V Operating Voltage Range (LTC1983-5)
- Internal 900kHz Oscillator
- "Zero Current" Shutdown
- Short-Circuit and Over-Temperature Protected
- Low Profile (1mm) ThinSOT™ Package

### APPLICATIONS

- $-3V$  Generation in Single-Supply Systems
- Portable Equipment
- LCD Bias Supplies
- GaAs FET Bias Supplies

### DESCRIPTION

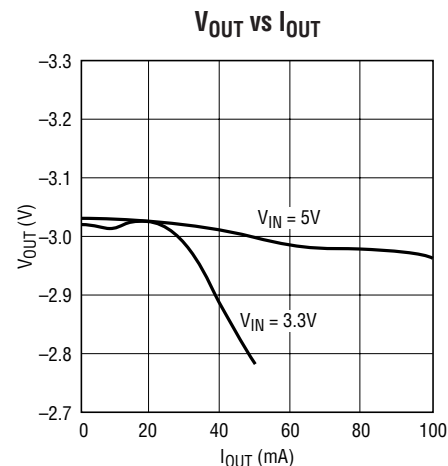
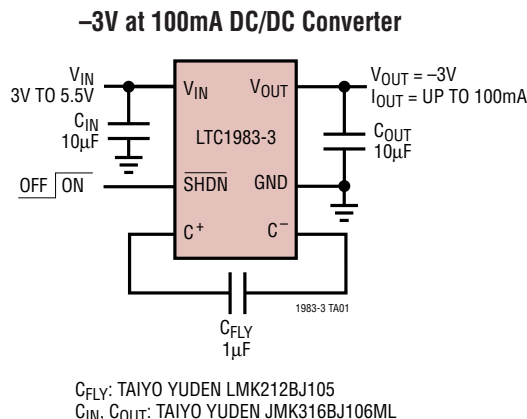
The LTC®1983-3 and LTC1983-5 are inverting charge pump DC/DC converters that produce negative regulated outputs. The parts require only three tiny external capacitors and can provide up to 100mA of output current. The devices can operate in open loop mode (creating a  $-V_{IN}$  supply) or regulated output mode depending on the input supply voltage and the output current.

The LTC1983-3/LTC1983-5 have many useful features for portable applications including very low quiescent current ( $25\mu A$  typical) and a zero current shutdown mode programmed through the SHDN pin.

The LTC1983-3/LTC1983-5 are over-temperature and short-circuit protected. The parts are available in a 6-pin low profile (1mm) ThinSOT package.

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ThinSOT is a trademark of Linear Technology Corporation.

### TYPICAL APPLICATION



# LTC1983-3/LTC1983-5

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ to GND .....	–0.3V to 6V
SHDN Voltage .....	–0.3V to 6V
$V_{OUT}$ to GND (LTC1983-3) .....	0.2V to $V_{OUT}$ Max
$V_{OUT}$ to GND (LTC1983-5) .....	0.2V to $V_{OUT}$ Max
$I_{OUT}$ Max .....	125mA
Output Short-Circuit Duration .....	Indefinite
Operating Temperature Range (Note 2) ...	–40°C to 85°C
Storage Temperature Range .....	–65°C to 125°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>VCC 1, VOUT 2, C+ 3, 6 SHDN, 5 GND, 4 C-</p> <p>S6 PACKAGE 6-LEAD PLASTIC SOT-23 T<sub>JMAX</sub> = 125°C, <math>\theta_{JA}</math> = 256°C/W</p>	ORDER PART NUMBER
	LTC1983ES6-3 LTC1983ES6-5
	S6 PART MARKING
	LTPC LTYB

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 5\text{V}$ ,  $C_{FLY} = 1\mu\text{F}$ ,  $C_{OUT} = 10\mu\text{F}$  unless otherwise noted.

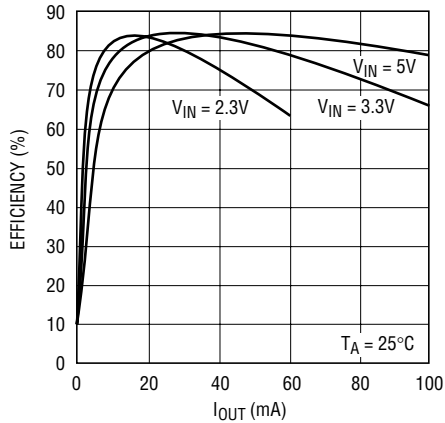
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}$ Operating Voltage (Regulated Output Mode) (LTC1983-3)		●	3.0		5.5	V
$V_{IN}$ Min Startup Voltage			2.3			V
$V_{OUT}$ (LTC1983-3)	$V_{IN} \geq 3.3\text{V}$ , $I_{OUT} \leq 25\text{mA}$	●	–2.88	–3	–3.12	V
	$V_{IN} \geq 5\text{V}$ , $I_{OUT} \leq 100\text{mA}$	●	–2.88	–3	–3.12	V
$V_{OUT}$ (LTC1983-5)	$V_{IN} \geq 5\text{V}$ , $V_{IN} - 5\text{V} \geq I_{OUT} \cdot R_{OUT}$	●	–4.8	–5	–5.2	V
$V_{IN}$ Operating Current	$V_{IN} \leq 5.5\text{V}$ , $I_{OUT} = 0\mu\text{A}$ , $\overline{\text{SHDN}} = V_{IN}$	●		25	60	$\mu\text{A}$
$V_{IN}$ Operating Current (Open-Loop Mode) (LTC1983-5)	$V_{IN} = 3.3\text{V}$			2.5		mA
	$V_{IN} = 4.75\text{V}$			4		mA
$V_{IN}$ Shutdown Current	$\overline{\text{SHDN}} = 0\text{V}$ , $V_{IN} \leq 5.5\text{V}$	●		0.1	1	$\mu\text{A}$
Output Ripple	$3.3 \leq V_{IN} \leq 5.5$			60		mV <sub>p-p</sub>
Open-Loop Output Impedance (LTC1983-3): $R_{OUT}$	$V_{IN} = 3.3\text{V}$ , $V_{OUT} = -3\text{V}$			11		$\Omega$
Open-Loop Output Impedance (LTC1983-5): $R_{OUT}$	$V_{IN} = 3.3\text{V}$ , $I_{OUT} \approx 50\text{mA}$			11		$\Omega$
	$V_{IN} = 5\text{V}$ , $I_{OUT} \approx 60\text{mA}$			8.5		$\Omega$
Oscillator Frequency	(Non-Burst Mode® Operation)			900		kHz
$\overline{\text{SHDN}}$ Input High		●	1.1			V
$\overline{\text{SHDN}}$ Input Low		●			0.3	V
$\overline{\text{SHDN}}$ Input Current	$V_{\overline{\text{SHDN}}} = 5.5\text{V}$	●		2.2	4	$\mu\text{A}$

Burst Mode is a registered trademark of Linear Technology Corporation.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

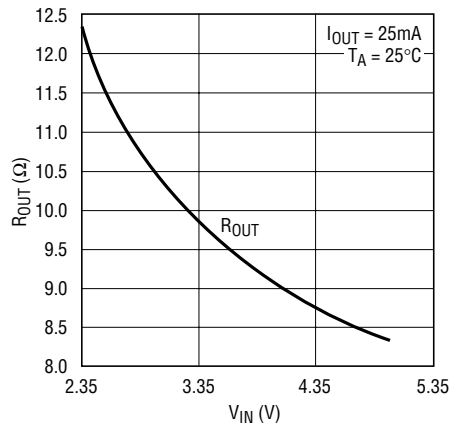
**Note 2:** The LTC1983E-3/LTC1983E-5 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

## TYPICAL PERFORMANCE CHARACTERISTICS

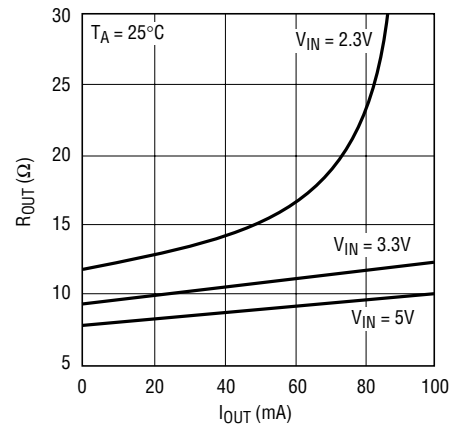
Efficiency vs  $I_{OUT}$  (LTC1983-5)

1983 G01

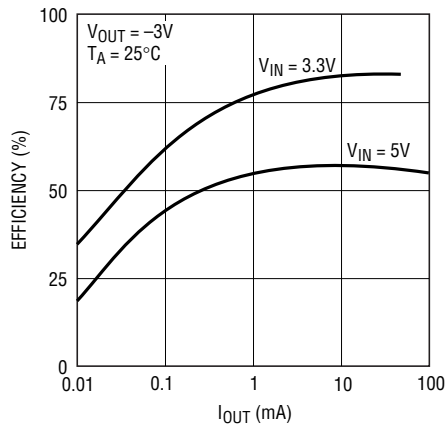
Output Impedance vs Input Voltage



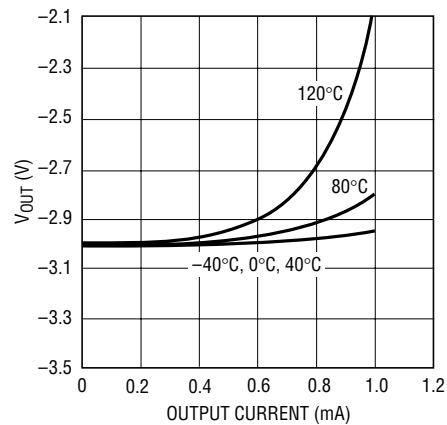
1983 TA02

Output Impedance vs  $I_{OUT}$  (LTC1983-5)

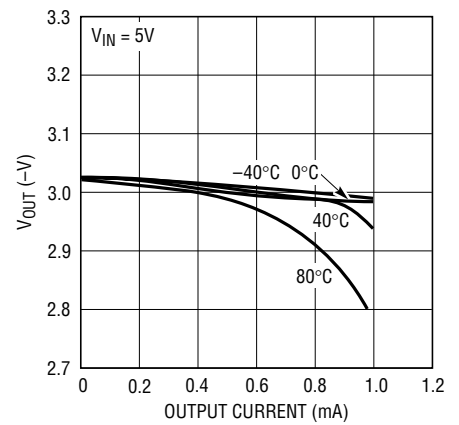
1983 G03

Efficiency vs  $I_{OUT}$ 

1983 G04

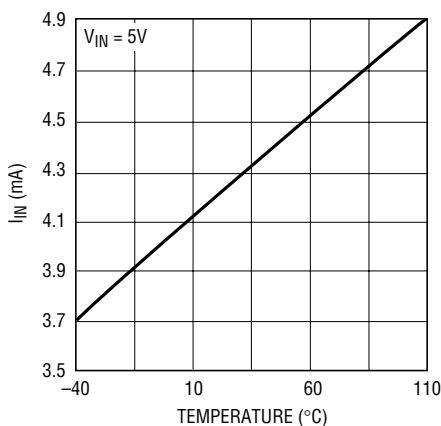
 $-3\text{V}_{OUT}$  vs  $I_{OUT}$  Over Temperature

1983 G05

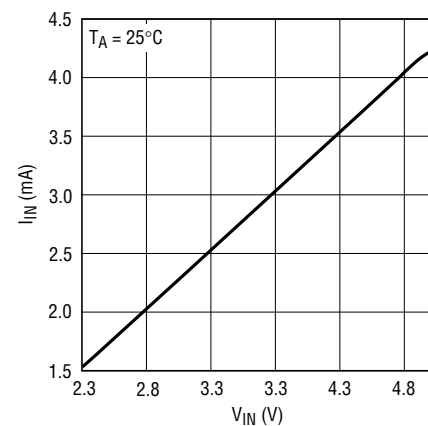
 $-3\text{V}_{OUT}$  vs  $I_{OUT}$  Over Temperature ( $V_{IN} = 5\text{V}$ )

1983 G06

Open-Loop Current vs Temperature (LTC1983-5)

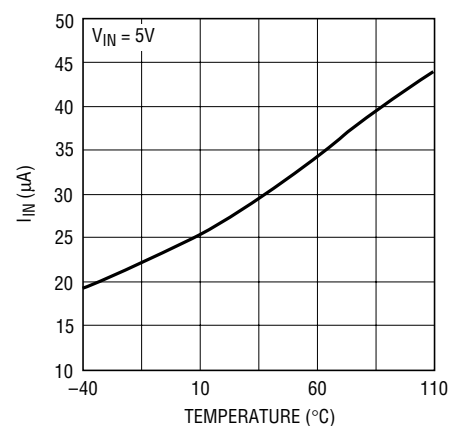


1983 G07

Open-Loop Input Current vs  $V_{IN}$  (LTC1983-5)

1983 G09

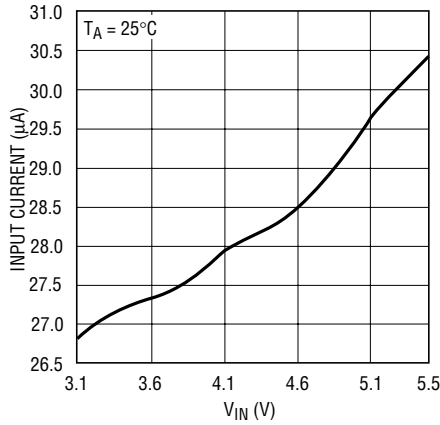
Burst Mode Current vs Temperature (LTC1983-3)



1983 G08

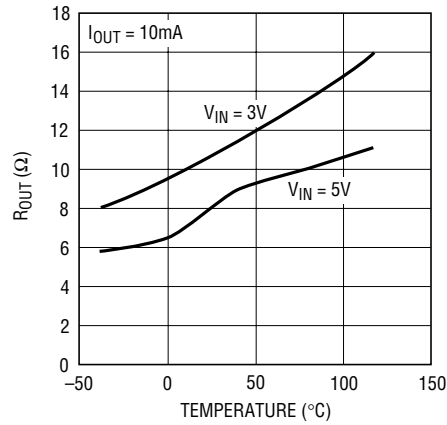
## TYPICAL PERFORMANCE CHARACTERISTICS

**Burst Mode Input Current vs  $V_{IN}$  (LTC1983-3)**



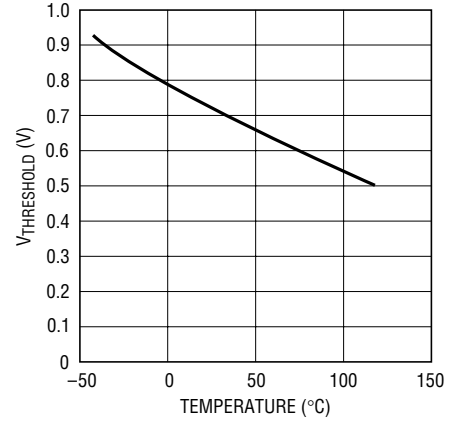
1983 G10

**$R_{OUT}$  vs Temperature ( $I_{OUT} = 10mA$ )**



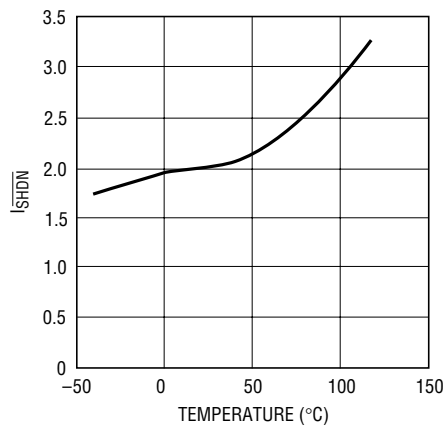
1983 G11

**SHDN Pin Threshold Voltage vs Temperature**



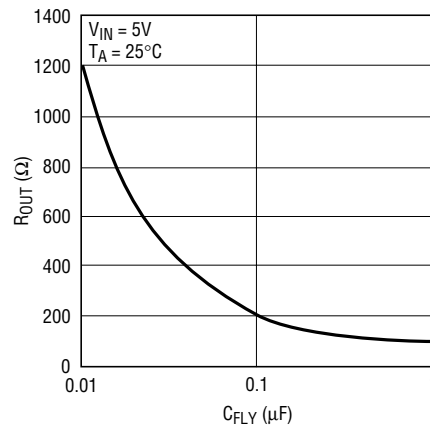
1983 G12

**SHDN Pin Input Current vs Temperature**



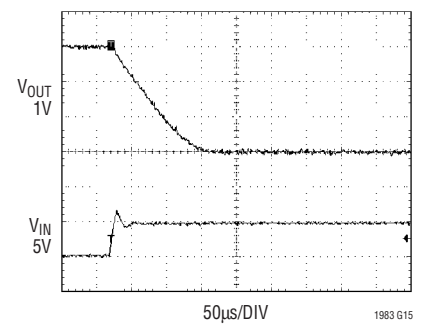
1983 G13

**$R_{OUT}$  vs  $C_{FLY}$  ( $V_{IN} = 5V$ )**



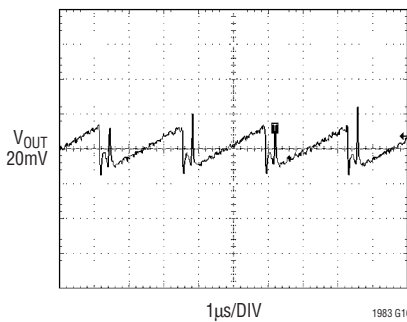
1983 G14

**$V_{OUT}$  Start-Up into 100mA Resistive Load**



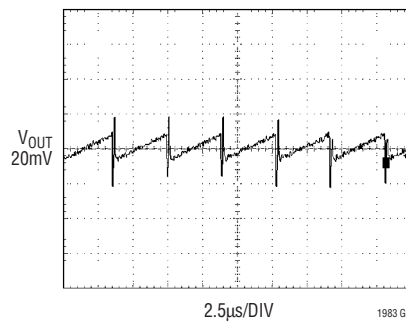
1983 G15

**$V_{OUT}$  Ripple at 100mA Load**



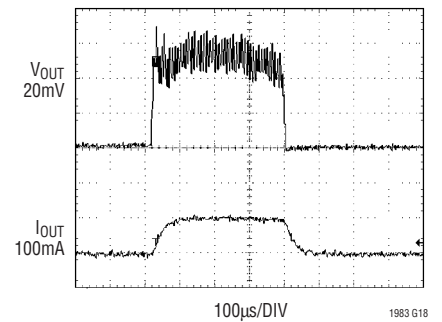
1983 G16

**$V_{OUT}$  Ripple at 30mA Load**



1983 G17

**$V_{OUT}$  Load Step Reponse from  $I_{OUT} = 0$  to  $I_{OUT} = 100mA$**



1983 G18

## PIN FUNCTIONS

**V<sub>IN</sub> (Pin 1):** Charge Pump Input Voltage. May be between 2.3V and 5.5V. V<sub>IN</sub> should be bypassed with a  $\geq 4.7\mu\text{F}$  low ESR capacitor as close as possible to the pin for best performance.

**V<sub>OUT</sub> (Pin 2):** Regulated Output Voltage for the IC. V<sub>OUT</sub> should be bypassed with a  $\geq 4.7\mu\text{F}$  low ESR capacitor as close as possible to the pin for best performance.

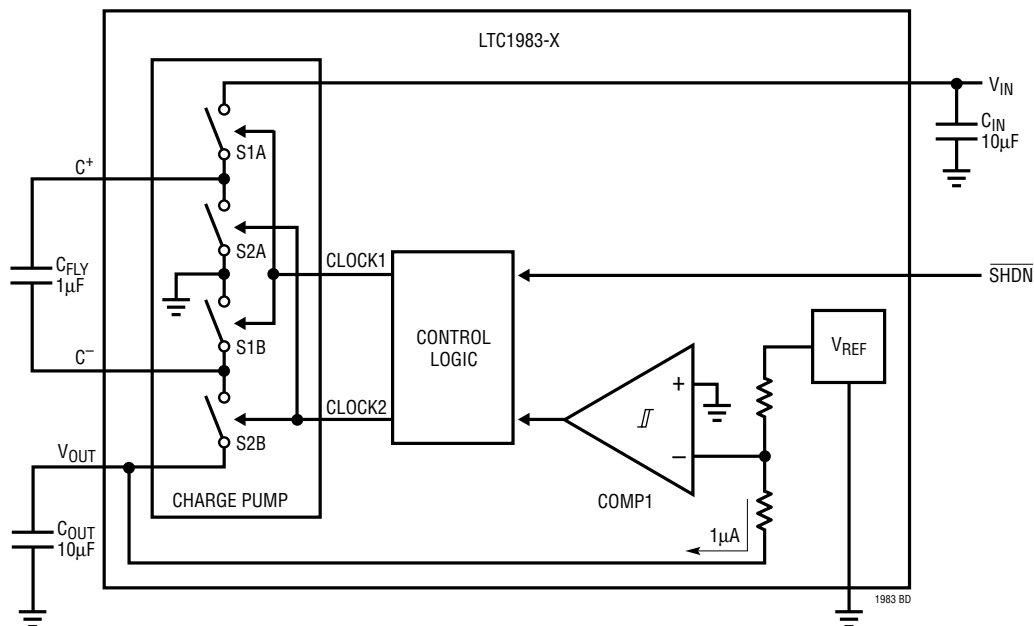
**C<sup>+</sup> (Pin 3):** Charge Pump Flying Capacitor Positive Terminal. This node is switched between V<sub>IN</sub> and GND (It is connected to V<sub>CC</sub> during shutdown).

**C<sup>-</sup> (Pin 4):** Charge Pump Flying Capacitor Negative Terminal. This node is switched between GND and V<sub>OUT</sub> (It is connected to GND during shutdown).

**GND (Pin 5):** Signal and Power Ground for the 6-Pin SOT-23 package. This pin should be tied to a ground plane for best performance.

**SHDN (Pin 6):** Shutdown. Grounding this pin shuts down the IC. Tie to V<sub>IN</sub> to enable. This pin should not be pulled above the V<sub>IN</sub> voltage or below GND.

## BLOCK DIAGRAM



## OPERATION (Refer to Block Diagram)

The LTC1983-3/LTC1983-5 use a switched capacitor charge pump to invert a positive input voltage to a regulated  $-3V \pm 4\%$  (LTC1983-3) or  $-5V \pm 4\%$  (LTC1983-5) output voltage. Regulation is achieved by sensing the output voltage through an internal resistor divider and enabling the charge pump when the output voltage droops above the upper trip point of COMP1. When the charge pump is enabled, a 2-phase, nonoverlapping clock controls the charge pump switches. Clock 1 closes the S1 switches which enables the flying capacitor to charge up to the  $V_{IN}$  voltage. Clock 2 closes the S2 switches that invert the  $V_{IN}$  voltage and connect the bottom plate of  $C_{FLY}$  to the output capacitor at  $V_{OUT}$ . This sequence of charging and discharging continues at a free-running frequency of 900kHz (typ) until the output voltage has been pumped down to the lower trip point of COMP1 and the charge pump is disabled. When the charge pump is disabled, the LTC1983 draws only 25 $\mu$ A (typ) from  $V_{IN}$  which provides high efficiency at low load conditions.

In shutdown mode, all circuitry is turned off and the part draws less than 1 $\mu$ A from the  $V_{IN}$  supply.  $V_{OUT}$  is also disconnected from  $V_{IN}$  and  $C_{FLY}$ . The SHDN pin has a threshold of approximately 0.7V. The part enters shutdown when a low is applied to the SHDN pin. The SHDN pin should not be floated; it must be driven with a logic high or low.

### Open-Loop Operation

The LTC1983-3/LTC1983-5 inverting charge pumps regulate at  $-3V/-5V$  respectively, unless the input voltage is too low or the output current is too high. The equations for output voltage regulation are as follows:

$$V_{IN} - 5.06V > I_{OUT} \cdot R_{OUT} \text{ (LTC1983-5)}$$

$$V_{IN} - 3.06V > I_{OUT} \cdot R_{OUT} \text{ (LTC1983-3)}$$

If this condition is not met, then the part will run in open loop mode and act as a low output impedance inverter for which the output voltage will be:

$$V_{OUT} = -[V_{IN} - (I_{OUT} \cdot R_{OUT})]$$

For all  $R_{OUT}$  values, check the corresponding curves in the Typical Performance Characteristics section (Note:  $C_{FLY} = 1\mu$ F for all  $R_{OUT}$  curves). The  $R_{OUT}$  value will be different for different flying caps, as shown in the following equation:

$$R_{OUT} = R_{OUT}(\text{curve}) - 1.11\Omega + \left( \frac{1}{f_{OSC} \cdot C_{FLY}} \right)$$

### Short-Circuit/Thermal Protection

During short-circuit conditions, the LTC1983 will draw several hundred milliamps from  $V_{IN}$  causing a rise in the junction temperature. On-chip thermal shutdown circuitry disables the charge pump once the junction temperature exceeds  $\approx 155^\circ\text{C}$ , and reenables the charge pump once the junction temperature falls back to  $\approx 145^\circ\text{C}$ . The LTC1983 will cycle in and out of thermal shutdown indefinitely without latchup or damage until the  $V_{OUT}$  short is removed.

### Capacitor Selection

For best performance, it is recommended that low ESR capacitors be used for both  $C_{IN}$  and  $C_{OUT}$  to reduce noise and ripple. The  $C_{IN}$  and  $C_{OUT}$  capacitors should be either ceramic or tantalum and should be 4.7 $\mu$ F or greater. Aluminum electrolytic are not recommended because of their high equivalent series resistance (ESR). If the source impedance is very low,  $C_{IN}$  may not be needed. Increasing the size of  $C_{OUT}$  to 10 $\mu$ F or greater will reduce output voltage ripple. The flying capacitor and  $C_{OUT}$  should also have low equivalent series inductance (ESL). The board layout is critical as well for inductance for the same reason (the suggested board layout should be used).

A ceramic capacitor is recommended for the flying capacitor with a value in the range of 0.1 $\mu$ F to 4.7 $\mu$ F. Note that a large value flying cap ( $>1\mu$ F) will increase output ripple unless  $C_{OUT}$  is also increased. For very low load applications, C1 may be reduced to 0.01 $\mu$ F to 0.047 $\mu$ F. This will reduce output ripple at the expense of efficiency and maximum output current.

## OPERATION (Refer to Block Diagram)

There are many aspects of the capacitors that must be taken into account. First, the temperature stability of the dielectric is a main concern. For ceramic capacitors, a three character code specifies the temperature stability (e.g. X7R, Y5V, etc.). The first two characters represent the temperature range that the capacitor is specified and the third represents the absolute tolerance that the capacitor is specified to over that temperature range. **The ceramic capacitor used for the flying and output capacitors should be X5R or better.** Second, the voltage coefficient of capacitance for the capacitor must be checked and the actual value usually needs to be derated for the operating voltage (the actual value has to be larger than the value needed to take into account the loss of capacitance due to voltage bias across the capacitor). Third, the frequency characteristics need to be taken into account because capacitance goes down as the frequency of oscillation goes up. Typically, the manufacturers have capacitance vs frequency curves for their products. This curve must be referenced to be sure the capacitance will not be too small for the application. Finally, the capacitor ESR and ESL must be low for reasons mentioned in the following section.

### Output Ripple

Normal LTC1983 operation produces voltage ripple on the  $V_{OUT}$  pin. Output voltage ripple is required for the LTC1983 to regulate. Low frequency ripple exists due to the hysteresis in the sense comparator and propagation delays in the charge pump enable/disable circuits. High frequency ripple is also present mainly due to ESR of the output capacitor. Typical output ripple under maximum load is  $60\text{mV}_{P-P}$  with a low ESR  $10\mu\text{F}$  output capacitor. The magnitude of the ripple voltage depends on several factors. High input voltage to negative output voltage differentials [ $(V_{IN} + V_{OUT}) > 1\text{V}$ ] increase the output ripple since more charge is delivered to  $C_{OUT}$  per clock cycle. A large flying capacitor ( $>1\mu\text{F}$ ) also increases ripple for the same reason. Large output current load and/or a small output capacitor ( $<10\mu\text{F}$ )

results in higher ripple due to higher output voltage  $dV/dt$ . High ESR capacitors ( $\text{ESR} > 0.1\Omega$ ) on the output pin cause high frequency voltage spikes on  $V_{OUT}$  with every clock cycle.

There are several ways to reduce the output voltage ripple. A larger  $C_{OUT}$  capacitor ( $22\mu\text{F}$  or greater) will reduce both the low and high frequency ripple due to the lower  $C_{OUT}$  charging and discharging  $dV/dt$  and the lower ESR typically found with higher value (larger case size) capacitors. A low ESR ceramic output capacitor will minimize the high frequency ripple, but will not reduce the low frequency ripple unless a high capacitance value is chosen. A reasonable compromise is to use a  $10\mu\text{F}$  to  $22\mu\text{F}$  tantalum capacitor in parallel with a  $1\mu\text{F}$  to  $4.7\mu\text{F}$  ceramic capacitor on  $V_{OUT}$  to reduce both the low and high frequency ripple. However, the best solution is to use  $10\mu\text{F}$  to  $22\mu\text{F}$ , X5R ceramic capacitors which are available in 1206 package sizes. An RC filter may also be used to reduce high frequency voltage spikes (see Figure 1).

In low load or high  $V_{IN}$  applications, smaller values for  $C_{FLY}$  may be used to reduce output ripple. A smaller flying capacitor ( $0.01\mu\text{F}$  to  $0.047\mu\text{F}$ ) delivers less charge per clock cycle to the output capacitor resulting in lower output ripple. However, the smaller value flying caps also reduce the maximum  $I_{OUT}$  capability as well as efficiency.

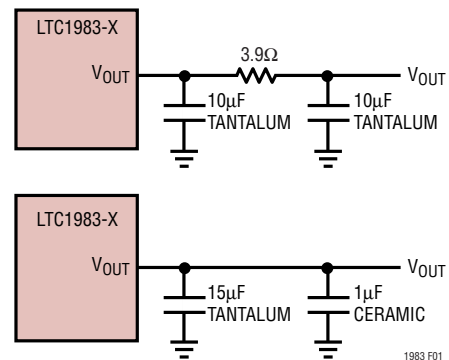


Figure 1. Output Ripple Reduction Techniques



## OPERATION (Refer to Block Diagram)

### Inrush Currents

During normal operation,  $V_{IN}$  will experience current transients in the several hundred milliamp range whenever the charge pump is enabled. During start-up, these inrush currents may approach 1 to 2 amps. For this reason, it is important to minimize the source resistance between the input supply and the  $V_{IN}$  pin. Too much source resistance may result in regulation problems or even prevent start-up. One way that this can be avoided (especially when the source impedance can't be lowered due to system constraints) is to use a large  $V_{IN}$  capacitor with low ESR right at the  $V_{IN}$  pin. If ceramic capacitors are used, you may need to add 1 $\mu$ F to 10 $\mu$ F tantalum capacitor in parallel to limit input voltage transients. Input voltage transients will occur if  $V_{IN}$  is applied via a switch or a plug. One example of this situation is in USB applications.

### Ultralow Quiescent Current Regulated Supply

The LTC1983 contains an internal resistor divider (refer to the Block Diagram) that draws only 1 $\mu$ A (typ for the 3V version) from  $V_{OUT}$  during normal operation. During shutdown, the resistor divider is disconnected from the output and the part draws only leakage current from the output. During no-load conditions, applying a 1Hz to 100Hz, 2% to 5% duty cycle signal to the SHDN pin ensures that the circuit of Figure 2 comes out of shutdown frequently enough to maintain regulation even under low-load conditions. Since the part spends nearly all of its time in shutdown, the no-load quiescent current is essentially zero. However, the part will still be in operation during the time the SHDN pin is high, so the current will not be zero and can be calculated using the following equations to determine the approximate maximum current:  $I_{IN(MAX)} = [(Time\ out\ of\ shutdown) \cdot (Burst\ Mode\ operation\ quiescent\ current) + (Normal\ operating\ I_{IN}) \cdot (Time\ output\ is\ being\ charged\ before\ the\ LTC1983\ enters\ Burst\ Mode\ operation)] / (Period\ of\ SHDN\ signal)$ . This number will be highly dependent on the amount of board leakage current and how many devices are connected to  $V_{OUT}$  (each will draw some leakage current) and must be calculated and verified for each different board design.

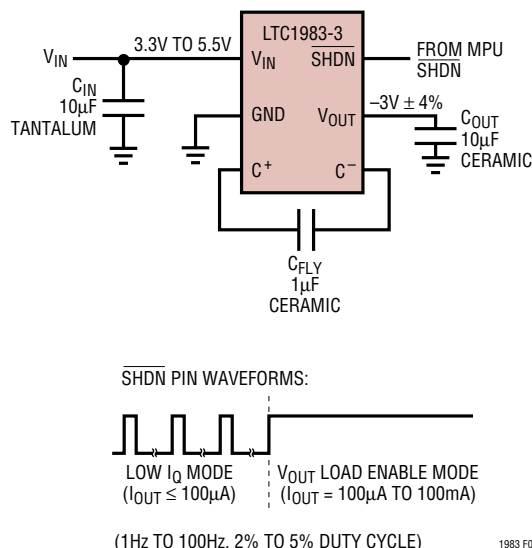


Figure 2. Ultralow Quiescent Current Regulated Supply

The LTC1983 must be out of shutdown for a minimum duration of 200 $\mu$ s to allow enough time to sense the output and keep it in regulation. A 1Hz, 2% duty cycle signal will keep  $V_{OUT}$  in regulation under no-load conditions. Even though the term no-load is used, there will always be board leakage current and leakage current drawn by anything connected to  $V_{OUT}$ . This is why it is necessary to wake the part up every once in a while to verify regulation. As the  $V_{OUT}$  load current increases, the frequency with which the part is taken out of shutdown must also be increased to prevent  $V_{OUT}$  from drooping below the -2.88V (for the 3V version) during the OFF phase (see Figure 3). A 100Hz, 2% duty cycle signal on the SHDN pin ensures proper regulation with load currents as high as 100 $\mu$ A. When load current greater than 100 $\mu$ A is needed, the SHDN pin must be forced high as in normal operation.

Each time the LTC1983 comes out of shutdown, the part delivers a minimum of one clock cycle worth of charge to the output. Under high  $V_{IN}$  (>4V) and/or low  $I_{OUT}$  (<10 $\mu$ A) conditions, this behavior may cause a net excess of charge to be delivered to the output capacitor if a high frequency signal is used on the SHDN pin (e.g., 50Hz to 100Hz). Under such conditions,  $V_{OUT}$  will slowly drift positive and may even go out of regulation. To avoid this potential



## OPERATION (Refer to Block Diagram)

problem in the low  $I_Q$  mode, it is necessary to switch the part in and out of shutdown at the minimum allowable frequency (refer to Figure 3) for a given output load.

### General Layout Considerations

Due to the high switching frequency and high transient currents produced by the LTC1983, careful board layout is a must. A clean board layout using a ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions (refer to Figures 4a and 4b). You will not get advertised performance with careless layout.

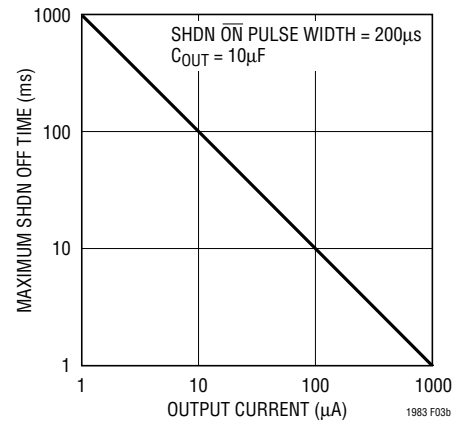


Figure 3

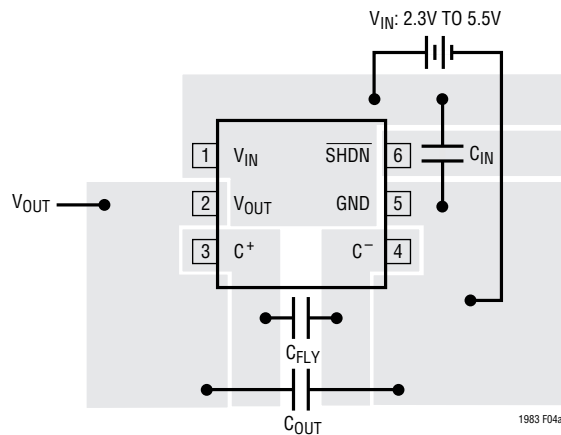


Figure 4a. Recommended Component Placement for a Single Layer Board

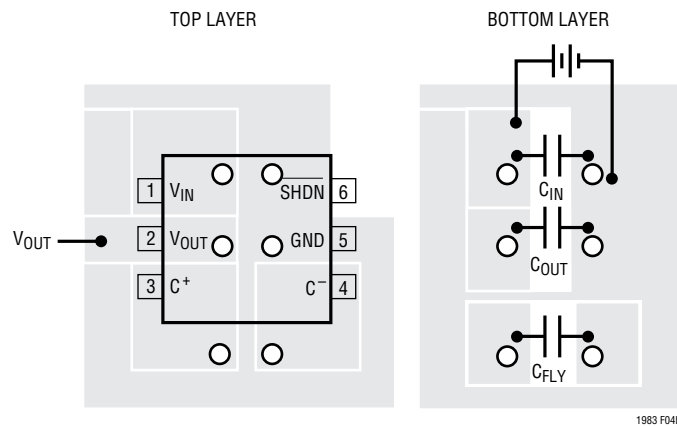
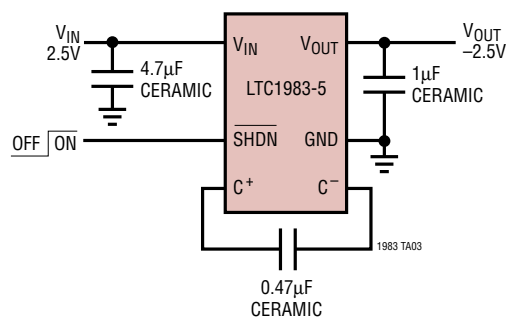


Figure 4b. Recommended Component Placement for a Double Layer Board

## TYPICAL APPLICATIONS

### 2.5V to -2.5V DC/DC Converter



### 100mA Inverting DC/DC Converter

