SINGLE HOT-SWAP POWER CONTROLLERS WITH CIRCUIT BREAKER AND POWER-GOOD REPORTING

Check for Samples: TPS2330, TPS2331

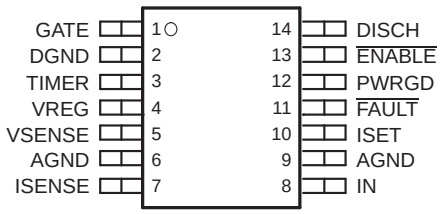
FEATURES

- **Single-Channel High-Side MOSFET Driver**
- **Input Voltage: 3 V to 13 V**
- **Output dV/dt Control Limits Inrush Current**
- **Circuit-Breaker With Programmable Overcurrent Threshold and Transient Timer**
- **Power-Good Reporting With Transient Filter**
- **CMOS- and TTL-Compatible Enable Input**
- **Low 5-µA Standby Supply Current (Max)**
- **Available in 14-Pin SOIC and TSSOP Package**
- **–40°C to 85°C Ambient Temperature Range**
- **Electrostatic Discharge Protection**

APPLICATIONS

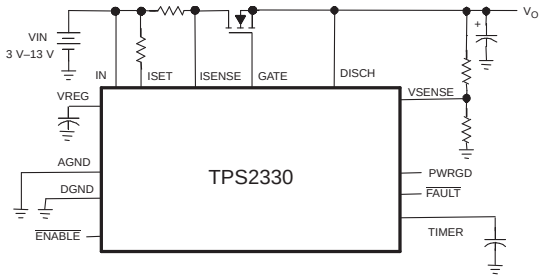
- **Hot-Swap/Plug/Dock Power Management**
- **Hot-Plug PCI, Device Bay**
- **Electronic Circuit Breaker**

D OR PW PACKAGE
(TOP VIEW)



NOTE: Terminal 13 is active-high on TPS2331.

typical application



DESCRIPTION

The TPS2330 and TPS2331 are single-channel hot-swap controllers that use external N-channel MOSFETs as high-side switches in power applications. Features of these devices, such as overcurrent protection (OCP), inrush-current control, output-power status reporting, and the ability to discriminate between load transients and faults, are critical requirements for hot-swap applications.

The TPS2330/31 devices incorporate undervoltage lockout (UVLO) and power-good (PG) reporting to ensure the device is off at start-up and confirm the status of the output voltage rails during operation. An internal charge pump, capable of driving multiple MOSFETs, provides enough gate-drive voltage to fully enhance the N-channel MOSFETs. The charge pump controls both the rise times and fall times (dV/dt) of the MOSFETs, reducing power transients during power up/down. The circuit-breaker functionality combines the ability to sense overcurrent conditions with a timer function; this allows designs such as DSPs, that may have high peak currents during power-state transitions, to disregard transients for a programmable period.

Table 1. AVAILABLE OPTIONS

T_A	HOT-SWAP CONTROLLER DESCRIPTION	PIN COUNT	PACKAGES(1)	
			$\overline{\text{ENABLE}}$	ENABLE
–40°C to 85°C	Dual-channel with independent OCP and adjustable PG	20	TPS2300IPW	TPS2301IPW
	Dual-channel with interdependent OCP and adjustable PG	20	TPS2310IPW	TPS2311IPW
	Dual-channel with independent OCP	16	TPS2320ID TPS2320IPW	TPS2321ID TPS2321IPW
	Single-channel with OCP and adjustable PG	14	TPS2330ID TPS2330IPW	TPS2331ID TPS2331IPW

(1) The packages are available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TPS2331IPWR).

FUNCTIONAL BLOCK DIAGRAM

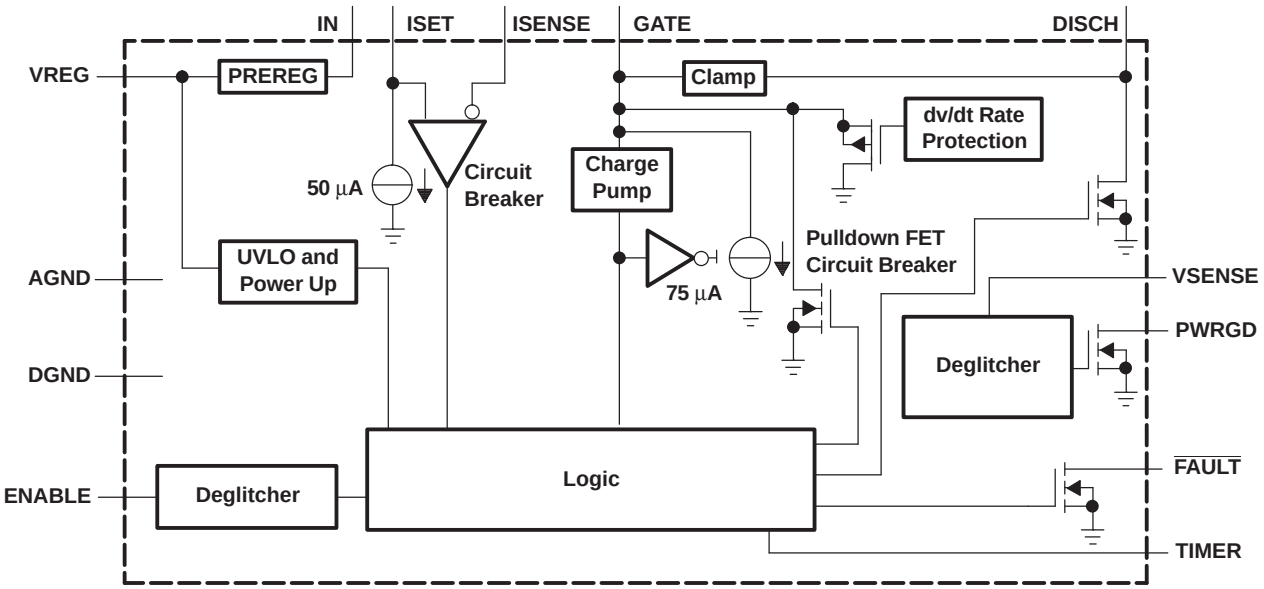


Table 2. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6, 9	I	Analog ground, connects to DGND as close as possible
DGND	2	I	Digital ground
DISCH	14	O	Discharge transistor
$\overline{\text{ENABLE}}$/ENABLE	13	I	Active-low (TPS2330) or active-high enable (TPS2331)
$\overline{\text{FAULT}}$	11	O	Overcurrent fault, open-drain output
GATE	1	O	Connects to gate of high-side MOSFET
IN	8	I	Input voltage
ISENSE	7	I	Current-sense input
ISET	10	I	Adjusts circuit-breaker threshold with resistor connected to IN
PWRGD	12	O	Open-drain output, asserted low when VSENSE voltage is less than reference.
TIMER	3	O	Adjusts circuit-breaker deglitch time
VREG	4	O	Connects to bypass capacitor, for stable operation
VSENSE	5	I	Power-good sense input

DETAILED DESCRIPTION

DISCH – DISCH should be connected to the source of the external N-channel MOSFET transistor connected to GATE. This pin discharges the load when the MOSFET transistor is disabled. They also serve as reference-voltage connection for internal gate-voltage-clamp circuitry.

$\overline{\text{ENABLE}}$ or ENABLE – $\overline{\text{ENABLE}}$ for TPS2330 is active-low. ENABLE for TPS2331 is active-high. When the controller is enabled, GATE voltage powers up to turn on the external MOSFETs. When the $\overline{\text{ENABLE}}$ pin is pulled high for TPS2330 or the ENABLE pin is pulled low for TPS2331 for more than 50 µs, the gate of the MOSFET is discharged at a controlled rate by a current source, and a transistor is enabled to discharge the output bulk capacitance. In addition, the device turns on the internal regulator PREREG (see VREG) when enabled and shuts down PREREG when disabled so that total supply current is much less than 5 µA.

$\overline{\text{FAULT}}$ – $\overline{\text{FAULT}}$ is an open-drain overcurrent flag output. When an overcurrent condition is sustained long enough to charge TIMER to 0.5 V, the device latches off and pulls $\overline{\text{FAULT}}$ low. In order to turn the device back on, either the enable pin must be toggled or the input power must be cycled.

GATE – GATE connects to the gate of the external N-channel MOSFET transistor. When the device is enabled, internal charge-pump circuitry pulls this pin up by sourcing approximately 15 µA. The turnon slew rates depend on the capacitance present at the GATE terminal. If desired, the turnon slew rates can be further reduced by connecting capacitors between this pin and ground. These capacitors also reduce inrush current and protect the device from false overcurrent triggering during power up. The charge-pump circuitry generates gate-to-source voltages of 9 V–12 V across the external MOSFET transistor.

IN – IN should be connected to the power source driving the external N-channel MOSFET transistor connected to GATE. The TPS2330/31 draws its operating current from IN, and remains disabled until the IN power supply has been established. The device has been constructed to support 3-V, 5-V, or 12-V operation.

ISENSE, ISET – ISENSE in combination with ISET implements overcurrent sensing for GATE. ISET sets the magnitude of the current that generates an overcurrent fault, through an external resistor connected to ISET. An internal current source draws 50 µA from ISET. With a sense resistor from IN to ISENSE, which is also connected to the drain of the external MOSFET, the voltage on the sense resistor reflects the load current. An overcurrent condition is assumed to exist if ISENSE is pulled below ISET. To ensure proper circuit breaker operation, $V_{I(ISENSE)}$ and $V_{I(ISET)}$ should never exceed $V_{I(IN)}$.

PWRGD – PWRGD signals the presence of undervoltage conditions on VSENSE. The pin is an open-drain output and is pulled low during an undervoltage condition. To minimize erroneous PWRGD responses from transients on the voltage rail, the voltage sense circuit incorporates a 20-µs deglitch filter. When VSENSE is lower than the reference voltage (about 1.23 V), PWRGD is active-low to indicate an undervoltage condition on the power-rail voltage. PWRGD may not correctly report power conditions when the device is disabled because there is no gate drive power for the PWRGD output transistor in the disable mode, or, in other words, PWRGD is floating. Therefore, PWRGD is pulled up to its pullup power supply rail in disable mode.

TIMER – A capacitor on TIMER sets the time during which the power switch can be in overcurrent before turning off. When the overcurrent protection circuits sense an excessive current, a current source is enabled which charges the capacitor on TIMER. Once the voltage on TIMER reaches approximately 0.5 V, the circuit-breaker latch is set and the power switch is latched off. Power must be recycled or the ENABLE pin must be toggled to restart the controller. In high-power or high-temperature applications, a minimum 50-pF capacitor is strongly recommended from TIMER to ground, to prevent any false triggering.

VREG – VREG is the output of an internal low-dropout voltage regulator, where IN1 is the input. The regulator is used to generate a regulated voltage source, less than 5.5 V, for the device. A 0.1-µF ceramic capacitor should be connected between VREG and ground to aid in noise rejection. In this configuration, on disabling the device, the internal low-dropout regulator also is disabled, which removes power from the internal circuitry and allows the device to be placed in low-quiescent-current mode. In applications where IN1 is less than 5.5 V, VREG and IN1 may be connected together. However, under these conditions, disabling the device may not place the device in low-quiescent-current mode, because the internal low-dropout voltage regulator is being bypassed, thereby keeping internal circuitry operational. If VREG and IN1 are connected together, a 0.1-µF ceramic capacitor between VREG and ground is not needed if IN1 already has a bypass capacitor of 1 µF to 10 µF.

VSENSE – VSENSE can be used to detect undervoltage conditions on external circuitry. If VSENSE senses a voltage below approximately 1.23 V, PWRGD is pulled low.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
Input voltage range	$V_{I(IN1)}$, $V_{I(ISENSE)}$, $V_{I(VSENSE)}$, $V_{I(ISET)}$, $V_{I(ENABLE)}$	–0.3 to 15	V
	$V_{I(VREG)}$	–0.3 to 7	V
Output voltage range	$V_{O(GATE)}$	–0.3 to 30	V
	$V_{O(DISCH)}$, $V_{O(PWRGD)}$, $V_{O(\overline{FAULT})}$, $V_{O(TIMER)}$	–0.3 to 15	V
Sink current range	$I_{(GATE)}$, $I_{(DISCH)}$	0 to 100	mA
	$I_{(PWRGD)}$, $I_{(TIMER)}$, $I_{(\overline{FAULT})}$	0 to 10	mA
Operating virtual junction temperature range, T_J		–40 to 100	°C
Storage temperature range, T_{stg}		–55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to DGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW-14	755 mW	10.07 mW/°C	302 mW	151 mW
D-14	613 mW	8.18 mW/°C	245 mW	123 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_I	Input voltage	$V_{I(IN)}$, $V_{I(ISENSE)}$, $V_{I(VSENSE)}$, $V_{I(ISET)}$	3		13	V
		$V_{I(VREG)}$	3		5.5	
		$V_{I(ISENSE)}$, $V_{I(ISET)}$, $V_{I(VSENSE)}$			$V_{I(IN)}$	
T_J	Operating virtual junction temperature		–40		100	°C

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range (–40°C < T_A < 85°C), 3V ≤ $V_{I(IN1)}$ ≤13 V, 3 V ≤ $V_{I(IN2)}$ ≤ 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
$I_{I(IN)}$	Input current, IN	$V_{I(ENABLE)}$ = 5 V (TPS2331), $V_{I(\overline{ENABLE})}$ = 0 V (TPS2330)			0.5	1	mA
$I_{I(stby)}$	Standby current (sum of currents into IN, ISENSE, and ISET)	$V_{I(ENABLE)}$ = 0 V (TPS2331), $V_{I(\overline{ENABLE})}$ = 5 V (TPS2330)				5	µA
GATE							
$V_{G(GATE\_3V)}$	Gate voltage	$I_{I(GATE)}$ = 500 nA, DISCH open	$V_{I(IN)}$ = 3 V	9	11.5		V
$V_{G(GATE\_4.5V)}$			$V_{I(IN)}$ = 4.5 V	10.5	14.5		
$V_{G(GATE\_10.8V)}$			$V_{I(IN)}$ = 10.8 V	16.8	21		
$V_{C(GATE)}$	Clamping voltage, GATE to DISCH			9	10	12	V
$I_{S(GATE)}$	Source current, GATE	3 V ≤ $V_{I(IN)}$ ≤ 13.2 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE)}$ = $V_{I(IN)}$ + 6 V		10	14	20	µA
	Sink current, GATE	3 V ≤ $V_{I(IN)}$ ≤ 13.2 V, 3 V ≤ $V_{O(VREG)}$ ≤ 5.5 V, $V_{I(GATE)}$ = $V_{I(IN)}$		50	75	100	µA
$t_{r(GATE)}$	Rise time, GATE	C_g to GND = 1 nF(1)	$V_{I(IN)}$ = 3 V		0.5		ms
			$V_{I(IN)}$ = 4.5 V		0.6		
			$V_{I(IN)}$ = 10.8 V		1		
$t_{f(GATE)}$	Fall time, GATE	C_g to GND = 1 nF(1)	$V_{I(IN)}$ = 3 V		0.1		ms
			$V_{I(IN)}$ = 4.5 V		0.12		
			$V_{I(IN)}$ = 10.8 V		0.2		
TIMER							
$V_{(TO\_TIMER)}$	Threshold voltage, TIMER			0.4	0.5	0.6	V
	Charge current, TIMER	$V_{I(TIMER)}$ = 0 V		35	50	65	µA
	Discharge current, TIMER	$V_{I(TIMER)}$ = 1 V		1	2.5		mA
CIRCUIT BREAKER							
$V_{IT(CB)}$	Threshold voltage, circuit breaker	R_{ISET} = 1 kΩ		40	50	60	mV
		R_{ISET} = 400 Ω, T_A = 25°C		14	19	24	
		R_{ISET} = 1 kΩ, T_A = 25°C		44	50	53	
		R_{ISET} = 1.5 kΩ, T_A = 25°C		68	73	78	
$I_{(IB\_ISENSE)}$	Input bias current, I_{SENSE}				0.1	5	µA
	Discharge current, GATE	$V_{O(GATE)}$ = 4 V		400	800		mA
		$V_{O(GATE)}$ = 1 V		25	150		
$t_{pd(CB)}$	Propagation (delay) time, comparator inputs to gate output	C_g = 50 pF, (50% to 10%),	10-mV overdrive, C_{TIMER} = 50 pF		1.3		µs
$\overline{ENABLE}$, ACTIVE LOW (TPS2330)							
$V_{IH(\overline{ENABLE})}$	High-level input voltage, $\overline{ENABLE}$			2			V
$V_{IL(\overline{ENABLE})}$	Low-level input voltage, $\overline{ENABLE}$					0.8	V
$R_{I(\overline{ENABLE})}$	Input pullup resistance, $\overline{ENABLE}$	See (2)		100	200	300	kΩ
$t_{d(off\_\overline{ENABLE})}$	Turnoff delay time, $\overline{ENABLE}$	$V_{I(\overline{ENABLE})}$ increasing above stop threshold; 100 ns rise time, 20 mV overdrive(1)			60		µs
$t_{d(on\_\overline{ENABLE})}$	Turnon delay time, $\overline{ENABLE}$	$V_{I(\overline{ENABLE})}$ decreasing below start threshold; 100 ns fall time, 20 mV overdrive(1)			125		µs

(1) Specified, but not production tested.

(2) Test I_O of $\overline{ENABLE}$ at $V_{I(\overline{ENABLE})}$ = 1 V and 0 V, then $R_{I(\overline{ENABLE})} = \frac{1\ V}{I_{O\_0V} - I_{O\_1V}}$

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating temperature range (–40°C < T_A < 85°C), 3 V ≤$V_{I(IN1)}$ ≤13 V, 3 V ≤ $V_{I(IN2)}$ ≤ 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE, ACTIVE HIGH (TPS2331)						
$V_{IH(ENABLE)}$	High-level input voltage, ENABLE		2			V
$V_{IL(ENABLE)}$	Low-level input voltage, ENABLE				0.7	V
$R_{I(ENABLE)}$	Input pulldown resistance, ENABLE		100	150	300	kΩ
$t_{d(on\_ENABLE)}$	Turnon delay time, ENABLE	$V_{I(ENABLE)}$ increasing above start threshold; 100-ns rise time, 20-mV overdrive (1)		85		µs
$t_{d(off\_ENABLE)}$	Turnoff delay time, ENABLE	$V_{I(ENABLE)}$ decreasing below stop threshold; 100-ns fall time, 20-mV overdrive (1)		100		µs
PREREG						
$V_{(VREG)}$	PREREG output voltage	4.5 ≤ $V_{I(IN)}$ ≤ 13 V	3.5	4.1	5.5	V
$V_{(drop\_PREREG)}$	PREREG dropout voltage	$V_{I(IN)}$ = 3 V			0.1	V
VREG UVLO						
$V_{(TO\_UVLOstart)}$	Output threshold voltage, start		2.75	2.85	2.95	V
$V_{(TO\_UVLOstop)}$	Output threshold voltage, stop		2.65	2.78		V
$V_{hys(UVLO)}$	Hysteresis		50	75		mV
	UVLO sink current, GATE	$V_{I(GATE)}$ = 2 V	10			mA
PWRGD1 and PWRGD2						
$V_{IT(ISENSE)}$	Trip threshold, VSENSE	$V_{I(VSENSE)}$ decreasing	1.2	1.225	1.25	V
V_{hys}	Hysteresis voltage, power-good comparator		20	30	40	mV
$V_{O(sat\_PWRGD)}$	Output saturation voltage, PWRGD	I_O = 2 mA		0.2	0.4	V
$V_{O(VREG\_min)}$	Minimum $V_{O(VREG)}$ for valid power-good	I_O = 100 µA, $V_{O(PWRGD)}$ = 1 V			1	V
	Input bias current, power-good comparator	$V_{I(VSENSE)}$ = 5.5 V			1	µA
$I_{lkg(PWRGD)}$	Leakage current, PWRGD	$V_{O(PWRGD)}$ = 13 V			1	µA
t_{dr}	Delay time, rising edge, PWRGD	$V_{I(VSENSE)}$ increasing, overdrive = 20 mV, t_r = 100 ns (1)		25		µs
t_{df}	Delay time, falling edge, PWRGDx	$V_{I(VSENSEx)}$ decreasing, overdrive = 20 mV, t_r = 100 ns (1)		2		µs
$\overline{\text{FAULT}}$ OUTPUT						
$V_{O(sat\_\overline{FAULT})}$	Output saturation voltage, $\overline{\text{FAULT}}$	I_O = 2 mA			0.4	V
$I_{lkg(\overline{FAULT})}$	Leakage current, $\overline{\text{FAULT}}$	$V_{O(\overline{FAULT})}$ = 13 V			1	µA
DISCH						
$I_{(DISCH)}$	Discharge current, DISCH	$V_{I(DISCH)}$ = 1.5 V, $V_{I(VIN)}$ = 5 V	5	10		mA
$V_{IH(DISCH)}$	Discharge on high-level input voltage		2			V
$V_{IL(DISCH)}$	Discharge on low-level input voltage				1	V

(1) Specified, but not production tested.

PARAMETER MEASUREMENT INFORMATION

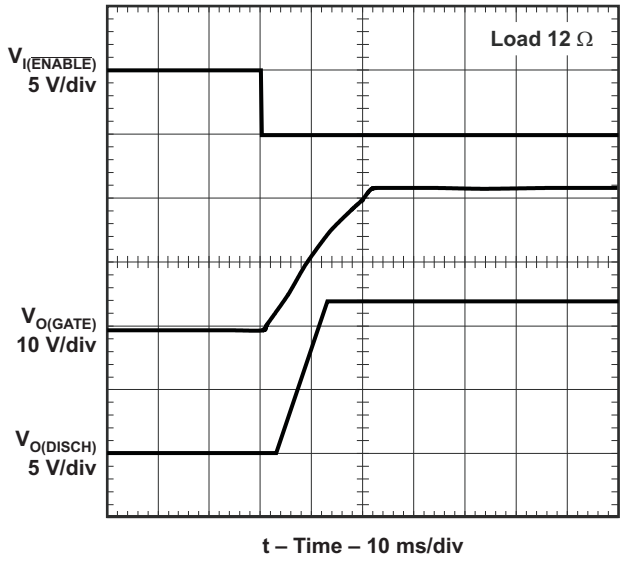


Figure 1. Turnon Voltage Transition

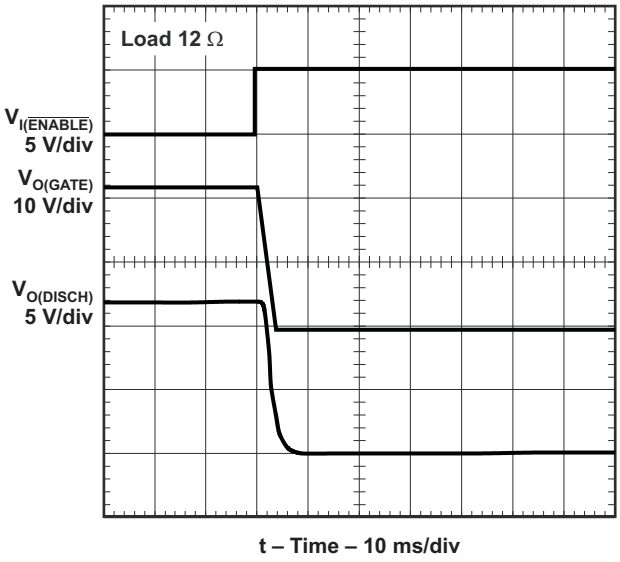


Figure 2. Turnoff Voltage Transition

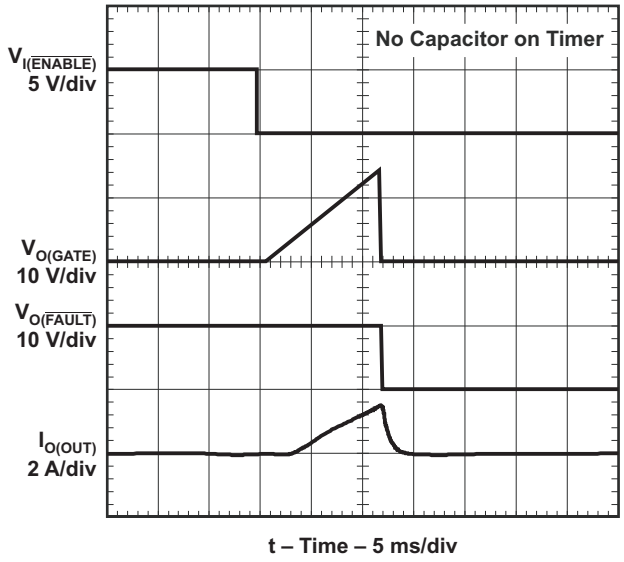


Figure 3. Overcurrent Response: Enabled Into Overcurrent Load

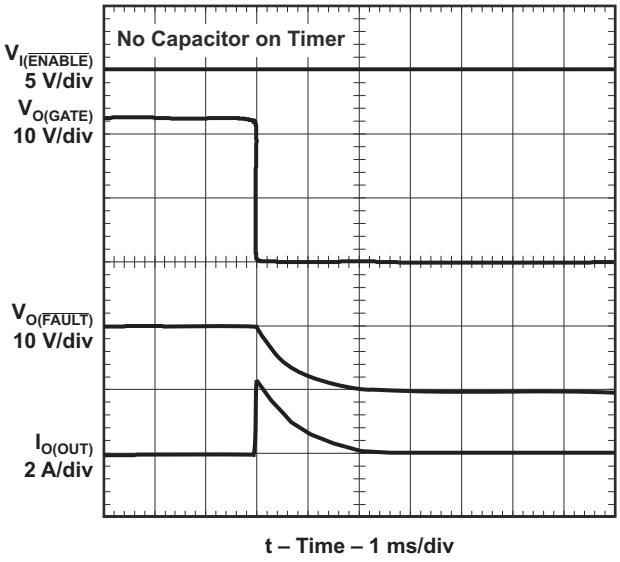


Figure 4. Overcurrent Response: an Overcurrent Load Plugged Into the Enabled Board

PARAMETER MEASUREMENT INFORMATION (continued)

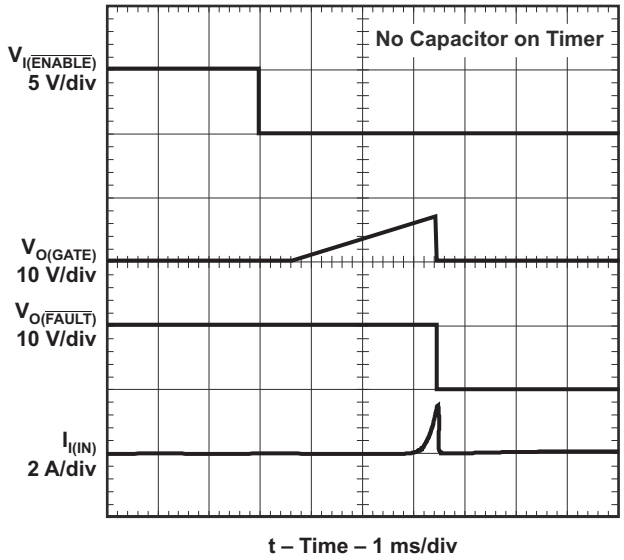


Figure 5. Enabled Into Short Circuit

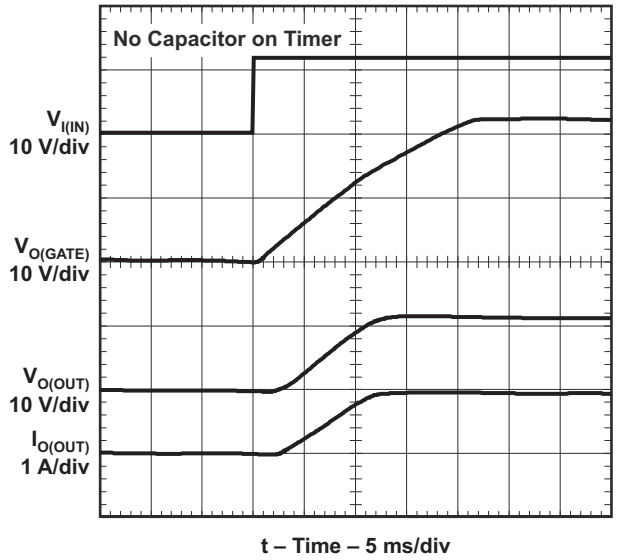


Figure 6. Hot Plug

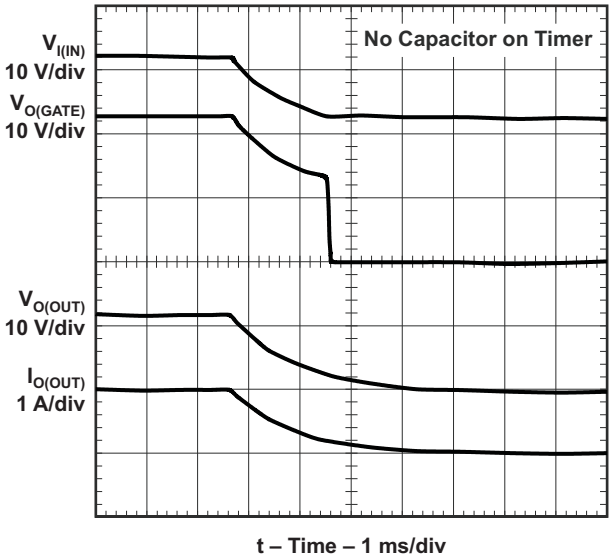


Figure 7. Hot Removal

TYPICAL CHARACTERISTICS

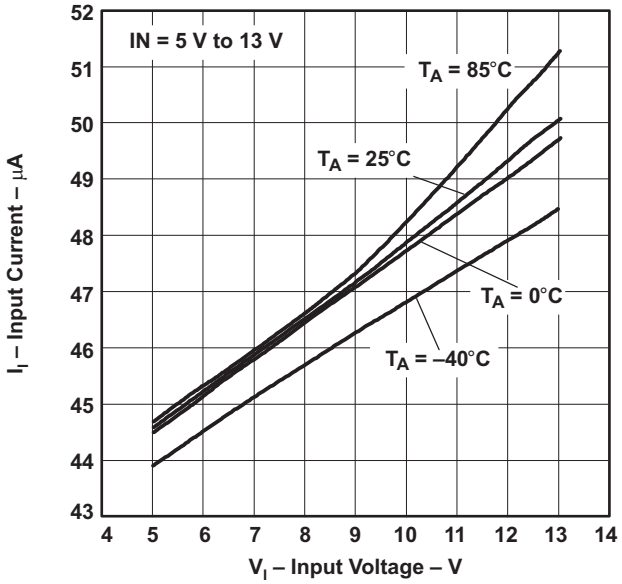


Figure 8.

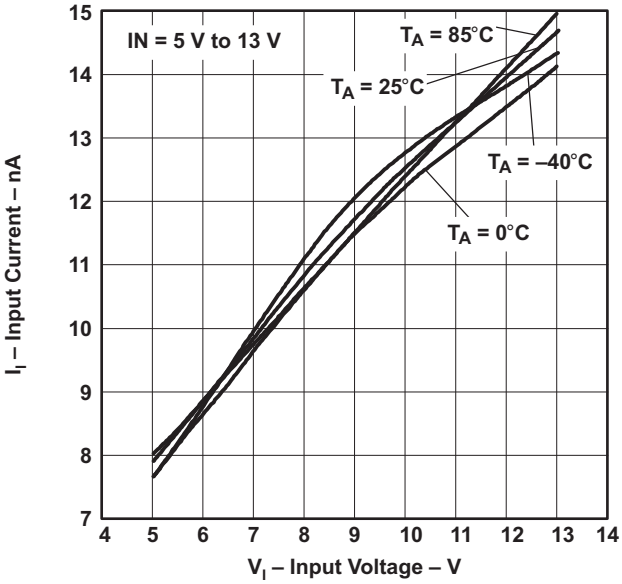


Figure 9.

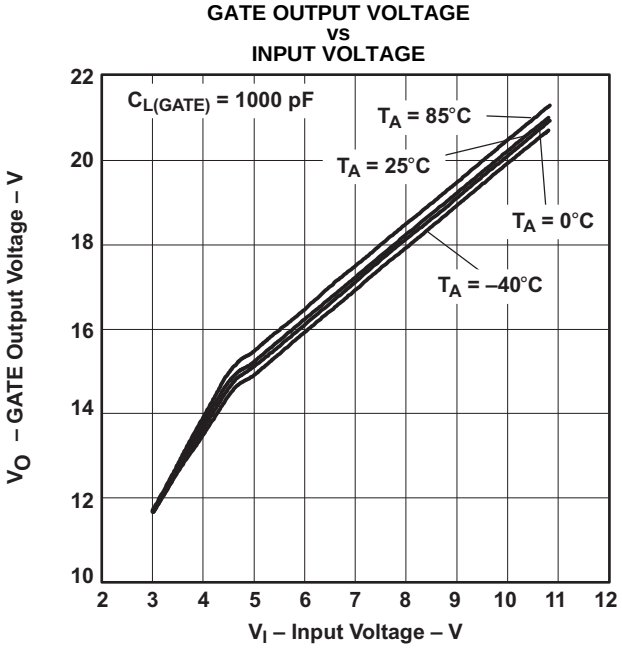


Figure 10.

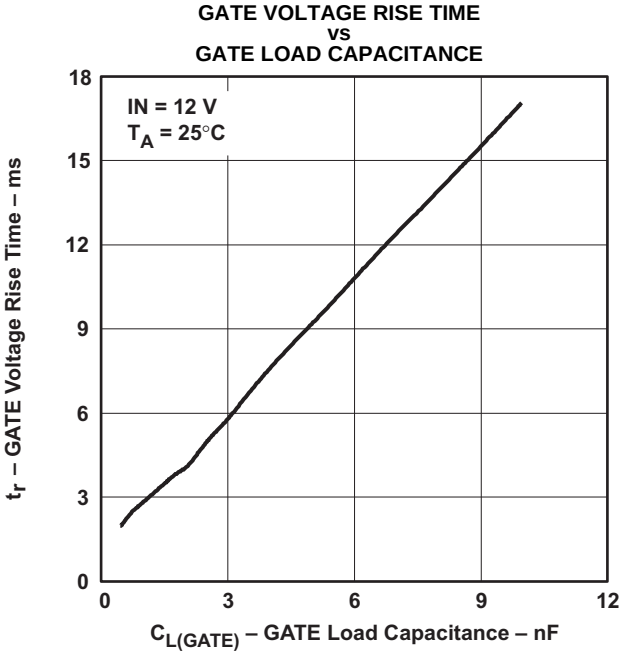


Figure 11.

TYPICAL CHARACTERISTICS (continued)

GATE VOLTAGE FALL TIME
vs
GATE LOAD CAPACITANCE

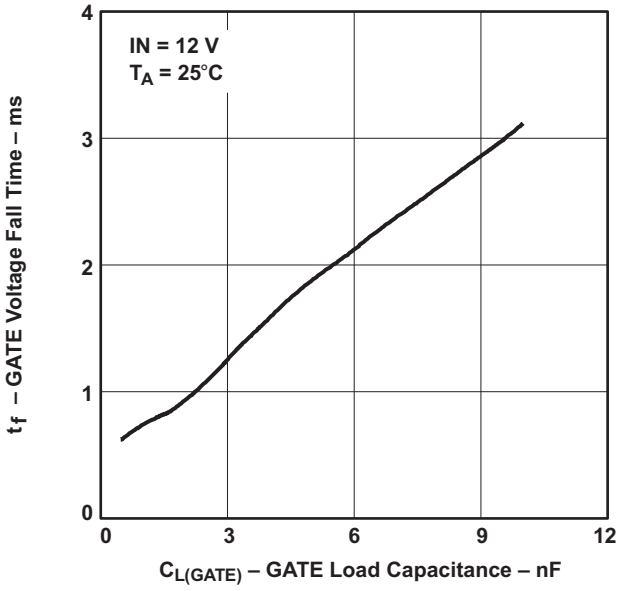


Figure 12.

GATE OUTPUT CURRENT
vs
GATE VOLTAGE

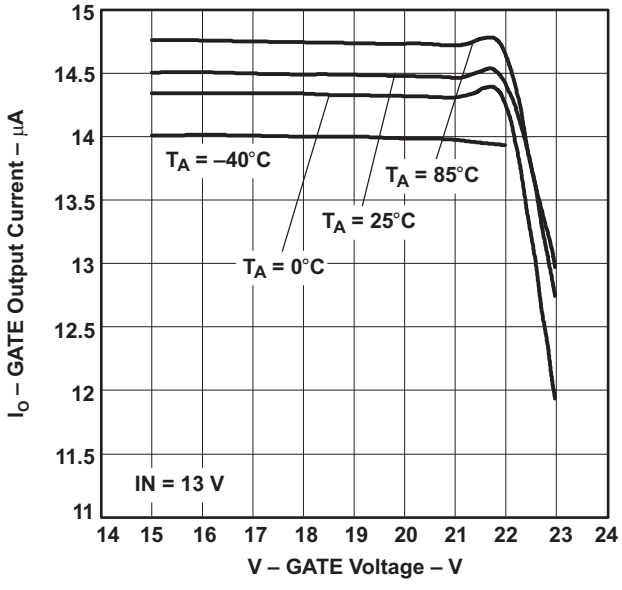


Figure 13.

CIRCUIT-BREAKER RESPONSE TIME
vs
TIMER CAPACITANCE

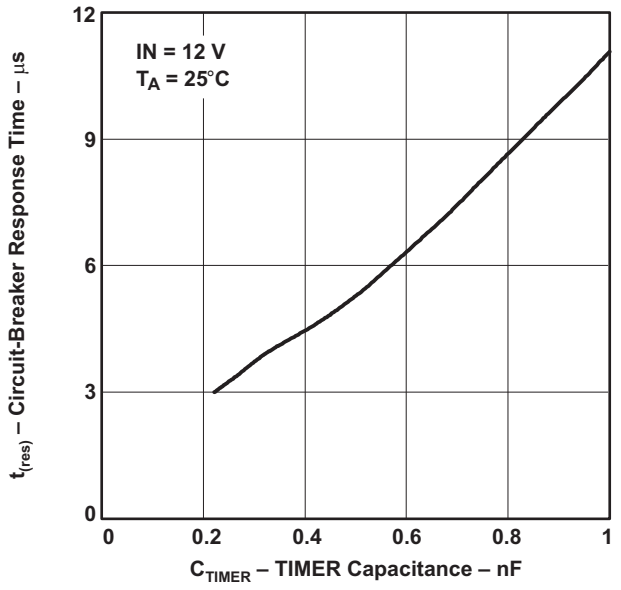


Figure 14.

LOAD VOLTAGE DISCHARGE TIME
vs
LOAD CAPACITANCE

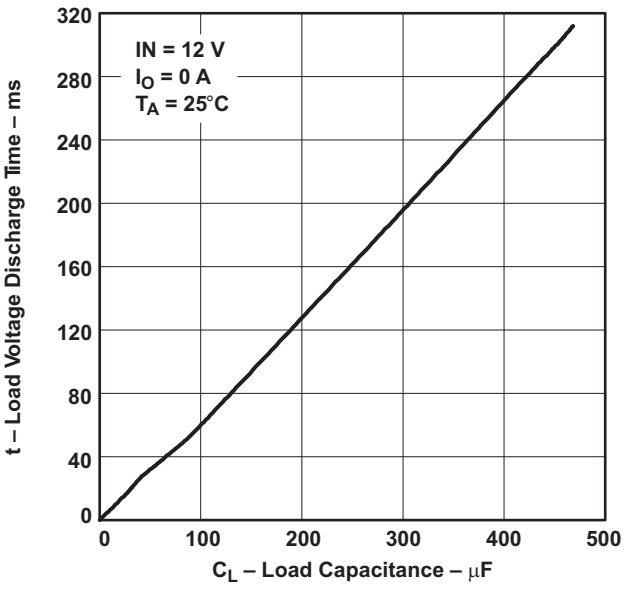


Figure 15.

TYPICAL CHARACTERISTICS (continued)

UVLO START AND STOP THRESHOLDS vs TEMPERATURE

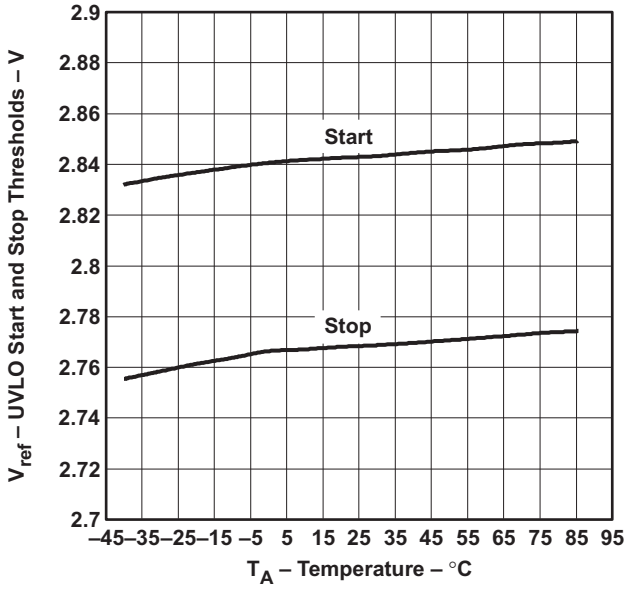


Figure 16.

PWRGD INPUT THRESHOLD vs TEMPERATURE

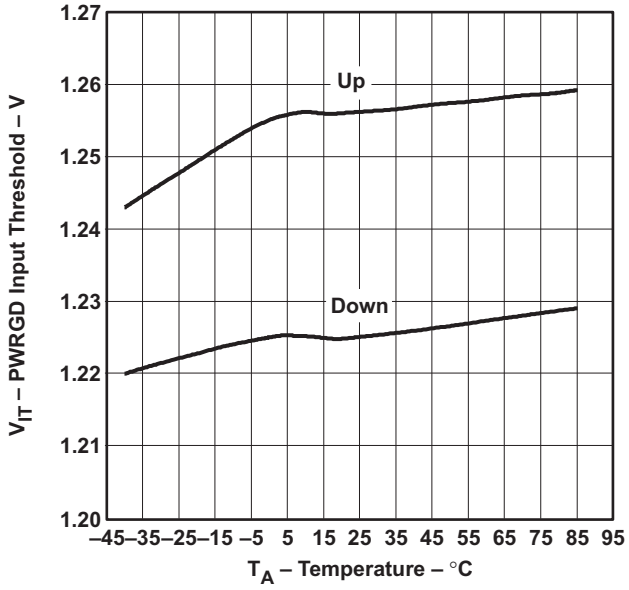


Figure 17.

APPLICATION INFORMATION

This diagram shows a typical dual hot-swap application. The pullup resistors at PWRGD and $\overline{\text{FAULT}}$ should be relatively large (e.g. 100 kΩ) to reduce power loss unless they are required to drive a large load.

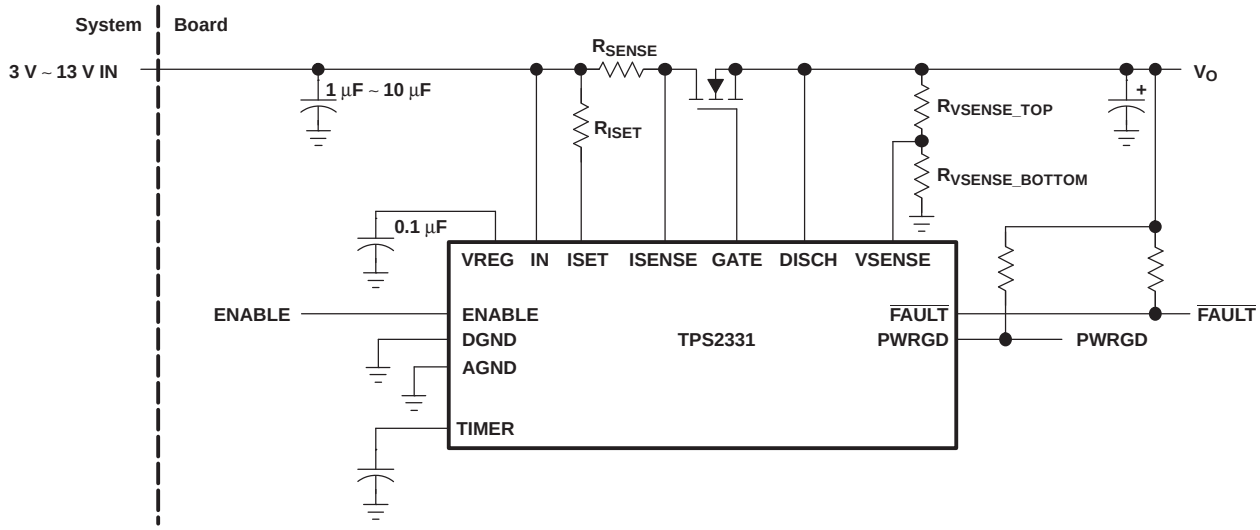


Figure 18. Typical Hot-Swap Application

INPUT CAPACITOR

A 0.1-µF ceramic capacitor in parallel with a 1-µF ceramic capacitor should be placed on the input power terminals near the connector on the hot-plug board to help stabilize the voltage rails on the cards. There is no need to mount the TPS2330/31 near the connector or these input capacitors. For applications with more severe power environments, a 2.2-µF or higher ceramic capacitor is recommended near the input terminals of the hot-plug board. A bypass capacitor for IN should be placed close to the device.

OUTPUT CAPACITOR

A 0.1-µF ceramic capacitor is recommended per load on the TPS2330/31; these capacitors should be placed close to the external FETs and to TPS2330/31. A larger bulk capacitor on the load is also recommended. The value of the bulk capacitor should be selected based on the power requirements and the transients generated by the application.

EXTERNAL FET

To deliver power from the input sources to the loads, the controller needs an external N-channel MOSFET. A few widely used MOSFETs are shown in Table 3. But many other MOSFETs on the market can also be used with the TPS23xx in hot-swap systems.

Table 3. Some Available N-Channel MOSFETs

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	IRF7601	N-channel, $r_{DS(on)}$ = 0.035 Ω, 4.6 A, Micro-8	International Rectifier
	MTSF3N03HDR2	N-channel, $r_{DS(on)}$ = 0.040 Ω, 4.6 A, Micro-8	ON Semiconductor
	IRF7101	Dual N-channel, $r_{DS(on)}$ = 0.1 Ω, 2.3 A, SO-8	International Rectifier
	MMSF5N02HDR2	Dual N-channel, $r_{DS(on)}$ = 0.04 Ω, 5 A, SO-8	ON Semiconductor
2 to 5	IRF7401	N-channel, $r_{DS(on)}$ = 0.022 Ω, 7 A, SO-8	International Rectifier
	MMSF5N02HDR2	N-channel, $r_{DS(on)}$ = 0.025 Ω, 5 A, SO-8	ON Semiconductor
	IRF7313	Dual N-channel, $r_{DS(on)}$ = 0.029 Ω, 5.2 A, SO-8	International Rectifier
	SI4410	N-channel, $r_{DS(on)}$ = 0.020 Ω, 8 A, SO-8	Vishay Dale
5 to 10	IRLR3103	N-channel, $r_{DS(on)}$ = 0.019 Ω, 29 A, d-Pak	International Rectifier
	IRLR2703	N-channel, $r_{DS(on)}$ = 0.045 Ω, 14 A, d-Pak	International Rectifier

TIMER

For most applications, a minimum capacitance of 50 pF is recommended to prevent false triggering. This capacitor should be connected between TIMER and ground. The presence of an overcurrent condition on of the TPS2330/31 causes a 50-µA current source to begin charging this capacitor. If the overcurrent condition persists until the capacitor has been charged to approximately 0.5 V, the TPS2330/31 latches off the transistor and pulls the $\overline{\text{FAULT}}$ pin low. The timer capacitor can be made as large as desired to provide additional time delay before registering a fault condition. The time delay is approximately:

$$dt(sec) = C_{(TIMER)}(F) \times 10{,}000(\Omega)$$

OUTPUT-VOLTAGE SLEW-RATE CONTROL

When enabled, the TPS2330/TPS2331 controllers supply the gate of an external MOSFET transistor with a current of approximately 15 µA. The slew rate of the MOSFET source voltage is thus limited by the gate-to-drain capacitance C_{gd} of the external MOSFET capacitor to a value approximating:

$$\frac{dV_S}{dt} = \frac{15\ \mu A}{C_{gd}} \quad (1)$$

If a slower slew rate is desired, an additional capacitance can be connected between the gate of the external MOSFET and ground.

VREG CAPACITOR

The internal voltage regulator connected to VREG requires an external capacitor to ensure stability. A 0.1-µF or 0.22-µF ceramic capacitor is recommended.

GATE DRIVE CIRCUITRY

The TPS2330/TPS2331 includes four separate features associated with each gate-drive terminal:

- A charging current of approximately 15 µA is applied to enable the external MOSFET transistor. This current is generated by an internal charge pump that can develop a gate-to-source potential (referenced to DISCH) of 9 V–12 V. DISCH must be connected to the external MOSFET source terminal to ensure proper operation of this circuitry.
- A discharge current of approximately 75 µA is applied to disable the external MOSFET transistor. Once the transistor gate voltage has dropped below approximately 1.5 V, this current is disabled and the UVLO discharge driver is enabled instead. This feature allows the part to enter a low-current shutdown mode while ensuring that the gate of the external MOSFET transistor remains at a low voltage.
- During a UVLO condition, the gate of the MOSFET transistor is pulled down by an internal PMOS transistor. This transistor continues to operate even if the voltage at IN is 0 V. This circuitry also helps hold the external MOSFET transistor off when power is suddenly applied to the system.
- During an overcurrent fault condition, the external MOSFET transistor that exhibited an overcurrent condition is rapidly turned off by an internal pulldown circuit capable of pulling in excess of 400 mA (at 4 V) from the

pin. Once the gate has been pulled below approximately 1.5 V, this driver is disengaged and the UVLO driver is enabled instead.

SETTING THE CURRENT-LIMIT CIRCUIT-BREAKER THRESHOLD

The current sensing resistor R_{ISENSE} and the current limit setting resistor R_{ISET} determine the current limit of the channel, and can be calculated by the following equation:

$$I_{LMT} = \frac{R_{ISET} \times 50 \times 10^{-6}}{R_{ISENSE}} \quad (2)$$

Typically R_{ISENSE} is usually very small (0.001 Ω to 0.1 Ω). If the trace and solder-junction resistances between the junction of R_{ISENSE} and ISENSE and the junction of R_{ISENSE} and R_{ISET} are greater than 10% of the R_{ISENSE} value, then these resistance values should be added to the R_{ISENSE} value used in the foregoing calculation.

Table 4 shows some of the current-sense resistors available in the market.

Table 4. Some Current-Sense Resistors

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 1	WSL-1206, 0.05 1%	0.05 Ω, 0.25 W, 1% resistor	Vishay Dale
1 to 2	WSL-1206, 0.025 1%	0.025 Ω, 0.25 W, 1% resistor	
2 to 4	WSL-1206, 0.015 1%	0.015 Ω, 0.25 W, 1% resistor	
4 to 6	WSL-2010, 0.010 1%	0.010 Ω, 0.5 W, 1% resistor	
6 to 8	WSL-2010, 0.007 1%	0.007 Ω, 0.5 W, 1% resistor	
8 to 10	WSR-2, 0.005 1%	0.005 Ω, 0.5 W, 1% resistor	

SETTING THE POWER-GOOD THRESHOLD VOLTAGE

The two feedback resistors R_{VSENSE_TOP} and R_{VSENSE_BOT} connected between V_O and ground form a resistor divider, setting the voltage at the VSENSE pins. VSENSE voltage equals:

$$V_{I(SENSE)} = V_O \times R_{VSENSE\_BOT}/(R_{VSENSE\_TOP} + R_{VSENSE\_BOT})$$

This voltage is compared to an internal voltage reference (1.225 V ±2%) to determine whether the output voltage level is within a specified tolerance. For example, given a nominal output voltage at V_O, and defining V_{O_min} as the minimum required output voltage, then the feedback resistors are defined by:

$$R_{VSENSE\_TOP} = \frac{V_{O\_min} - 1.225}{1.225} \times R_{VSENSE\_BOT} \quad (3)$$

Start the process by selecting a large standard resistor value for R_{VSENSE_BOT} to reduce power loss. Then R_{VSENSE_TOP} can be calculated by inserting all of the known values into the preceding equation. When V_O is lower than V_{O_min}, PWRGD is low as long as the controller is enabled.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS2330/TPS2331 includes an undervoltage lockout (UVLO) feature that monitors the voltage present on the VREG pin. This feature disables the external MOSFET if the voltage on VREG drops below 2.78 V (nominal) and re-enables normal operation when it rises above 2.85 V (nominal). Because VREG is fed from IN through a low-dropout voltage regulator, the voltage on VREG tracks the voltage on IN within 50 mV. While the undervoltage lockout is engaged, GATE is held low by an internal PMOS pulldown transistor, ensuring that the external MOSFET transistor remain off at the times, even if the power supply has fallen to 0 V.

POWER-UP CONTROL

The TPS2330/TPS2331 includes a 500-µs (nominal) start-up delay that ensures that internal circuitry has sufficient time to start before the device begins turning on the external MOSFETs. This delay is triggered only on the rapid application of power to the circuit. If the power supply ramps up slowly, the undervoltage lockout circuitry provides adequate protection against undervoltage operation.

THREE-CHANNEL HOT-SWAP APPLICATION

Some applications require hot-swap control of up to three voltage rails, but may not explicitly require the sensing of the status of the output power on all three of the voltage rails. One such application is a device bay, where dV/dt control of 3.3 V, 5 V, and 12 V is required. By using TPS2330/TPS2331 to drive all three power rails, as is shown in Figure 19, TPS2330/31 can deliver three different voltages to three loads while monitoring the status of one of the loads.

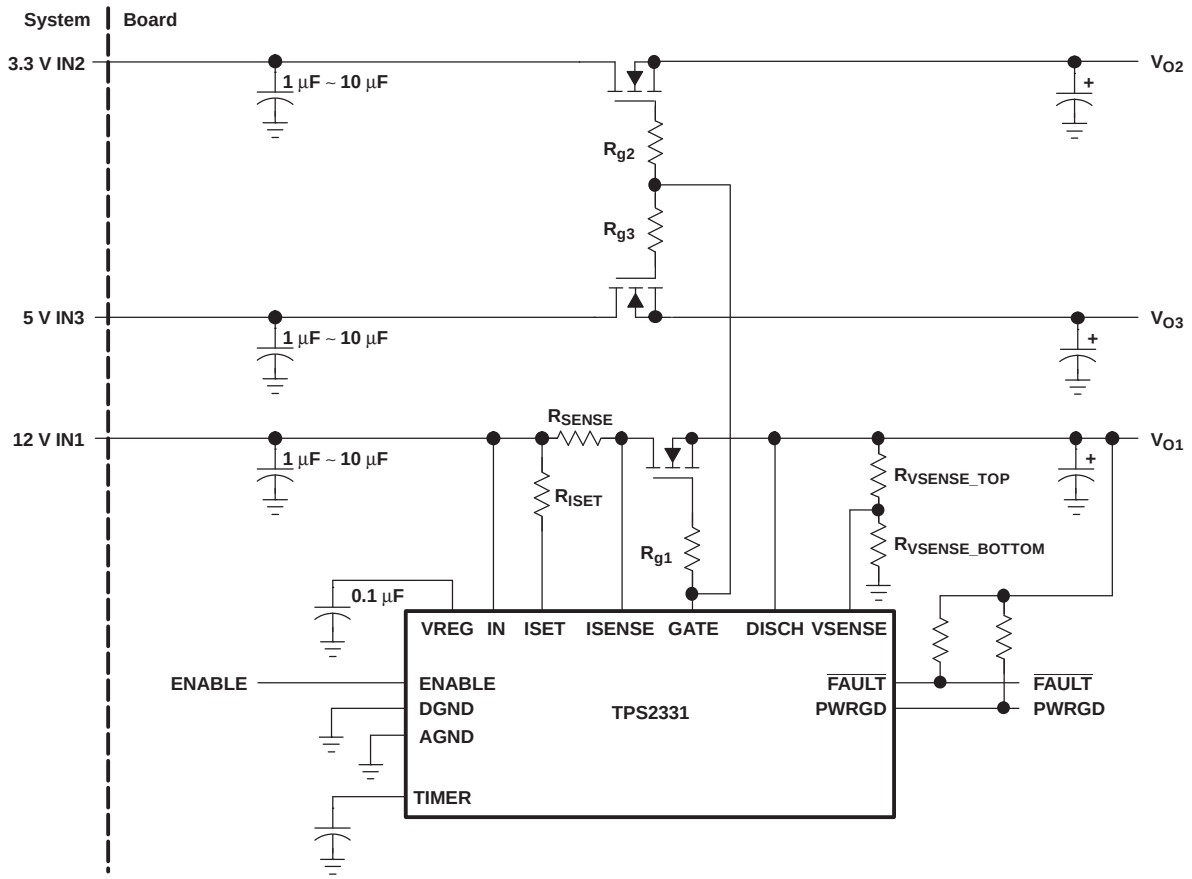


Figure 19. Three-Channel Application

Figure 20 shows ramp-up waveforms of the three output voltages.

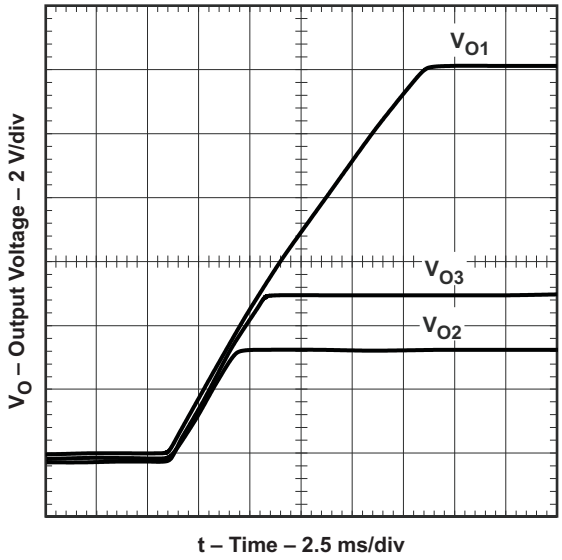


Figure 20.

REVISION HISTORY

Note: Revision history for previous versions is not available. Page numbers of previous versions may differ.

Changes from Revision F (November 2006) to Revision G	Page
• Added text to ISENSE, ISET pin description paragraph for clarification.	3
• Added additional V_I specs to ROC table for clarification	4
• Added minus sign to 40°C MIN T_J temperature	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2330ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2330I
TPS2330ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2330I
TPS2330IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2330I
TPS2330IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2330I
TPS2330IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2330IPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2330IPWG4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2330IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2330IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2330IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2330I
TPS2331ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2331I
TPS2331ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2331I
TPS2331IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2331I
TPS2331IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2331I
TPS2331IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2331I
TPS2331IPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2331I
TPS2331IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2331I
TPS2331IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD2331I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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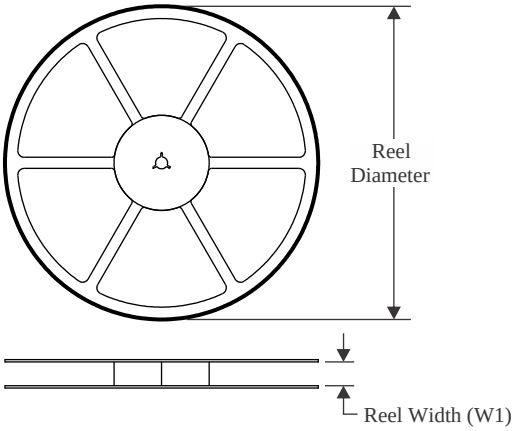
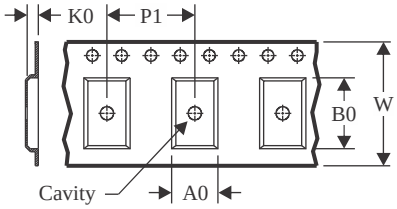
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

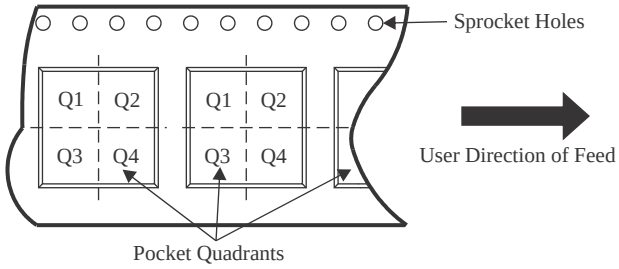


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

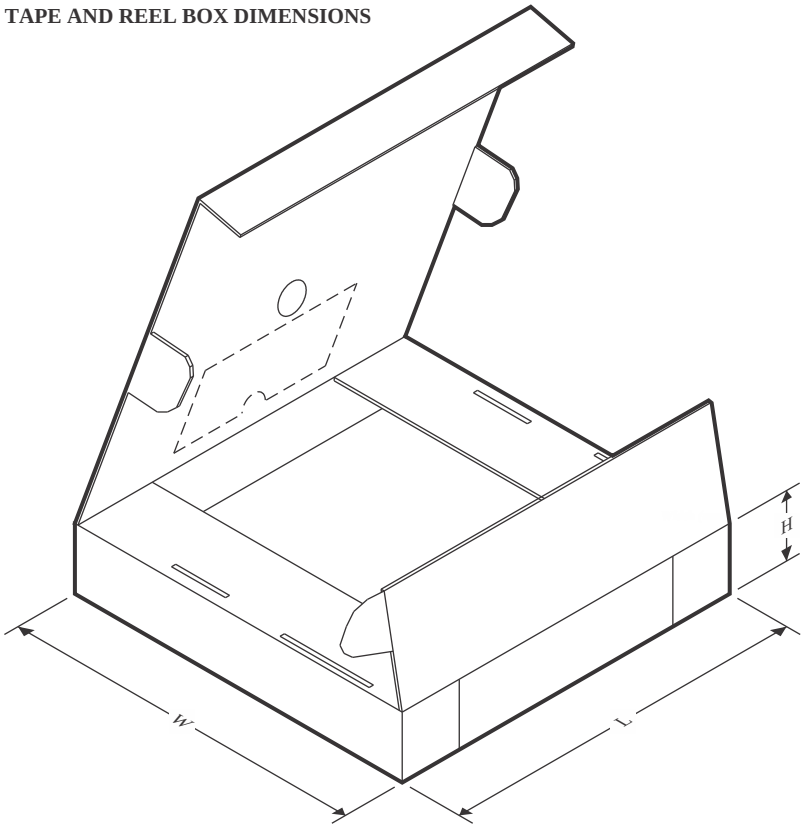
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2330IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TPS2330IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2331IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TPS2331IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

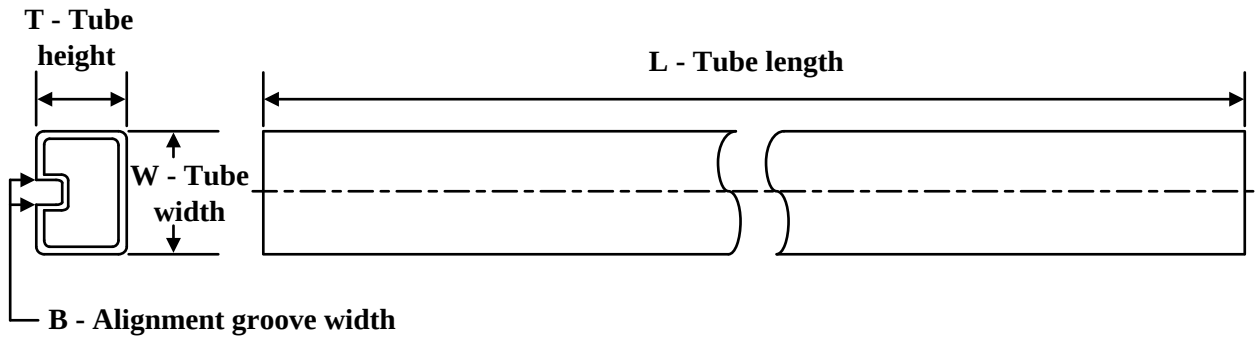
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

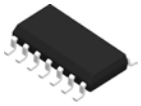
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2330IDR	SOIC	D	14	2500	350.0	350.0	43.0
TPS2330IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TPS2331IDR	SOIC	D	14	2500	350.0	350.0	43.0
TPS2331IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2330ID	D	SOIC	14	50	505.46	6.76	3810	4
TPS2330ID.A	D	SOIC	14	50	505.46	6.76	3810	4
TPS2330IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS2330IPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS2330IPWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS2331ID	D	SOIC	14	50	505.46	6.76	3810	4
TPS2331ID.A	D	SOIC	14	50	505.46	6.76	3810	4
TPS2331IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS2331IPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

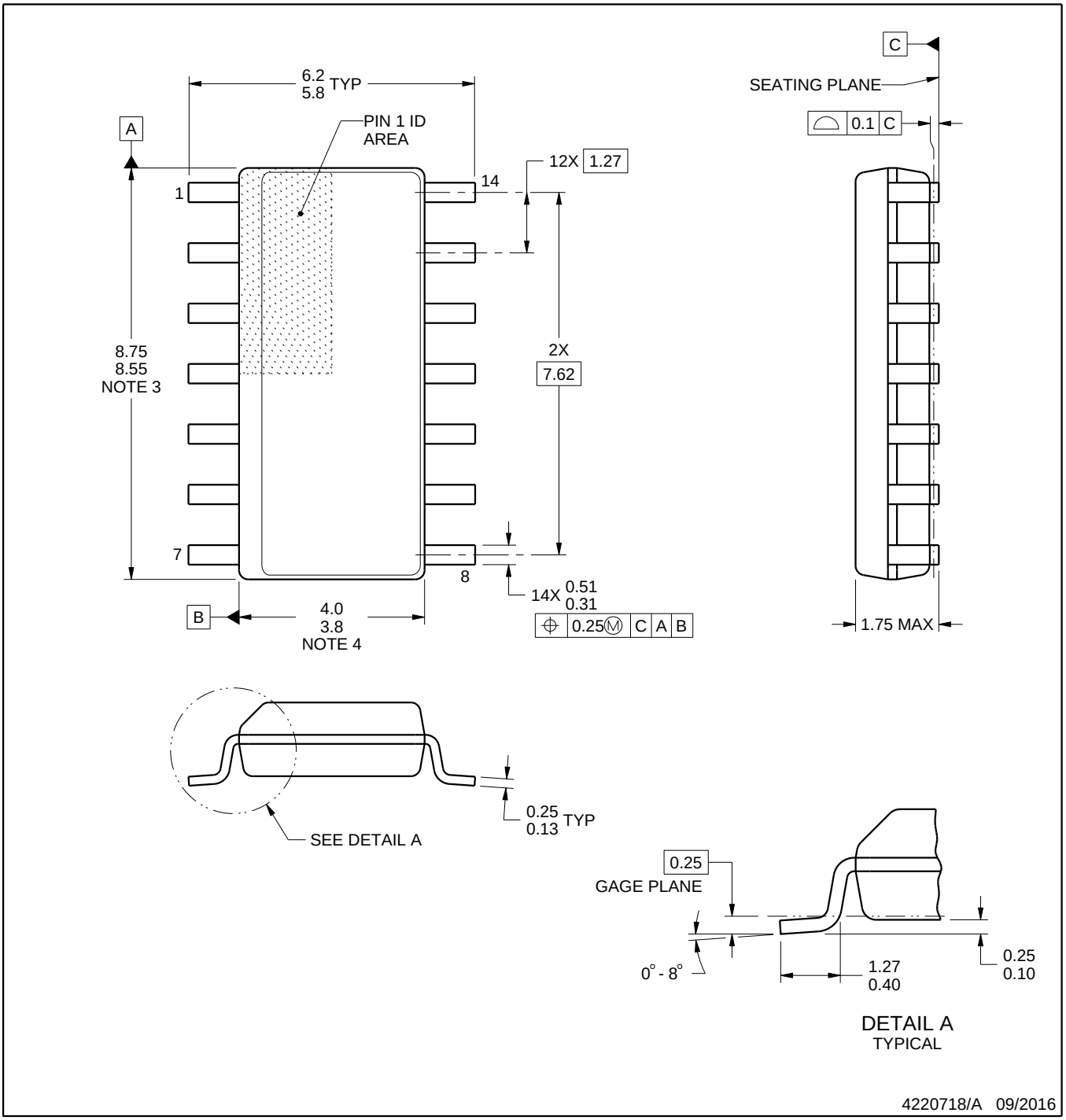


PACKAGE OUTLINE

D0014A

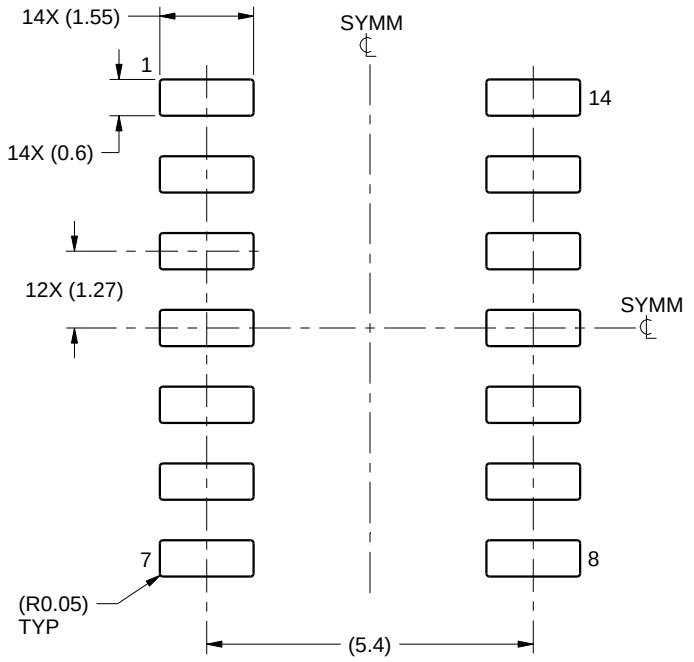
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

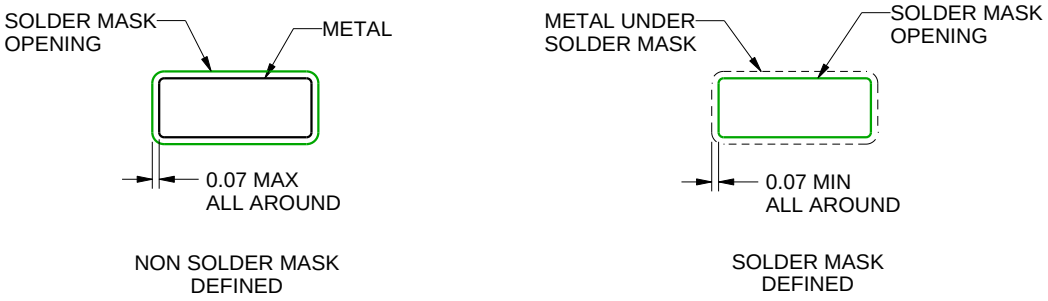


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

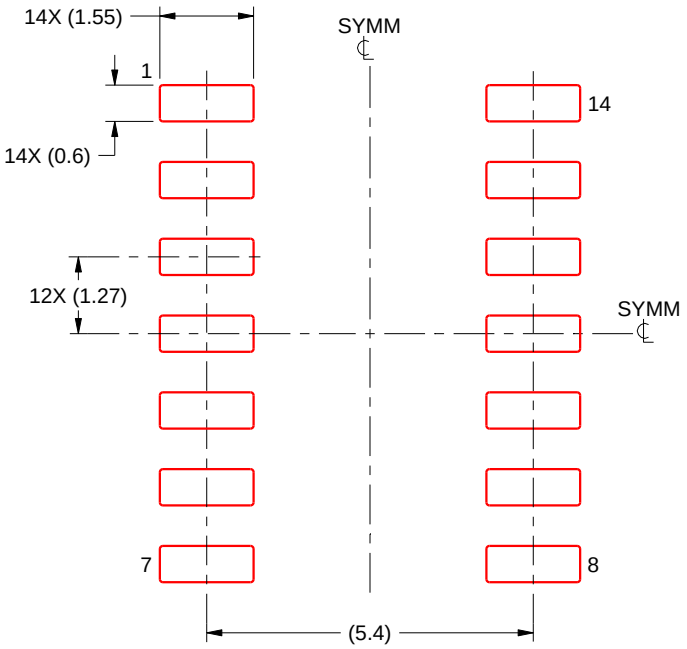
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

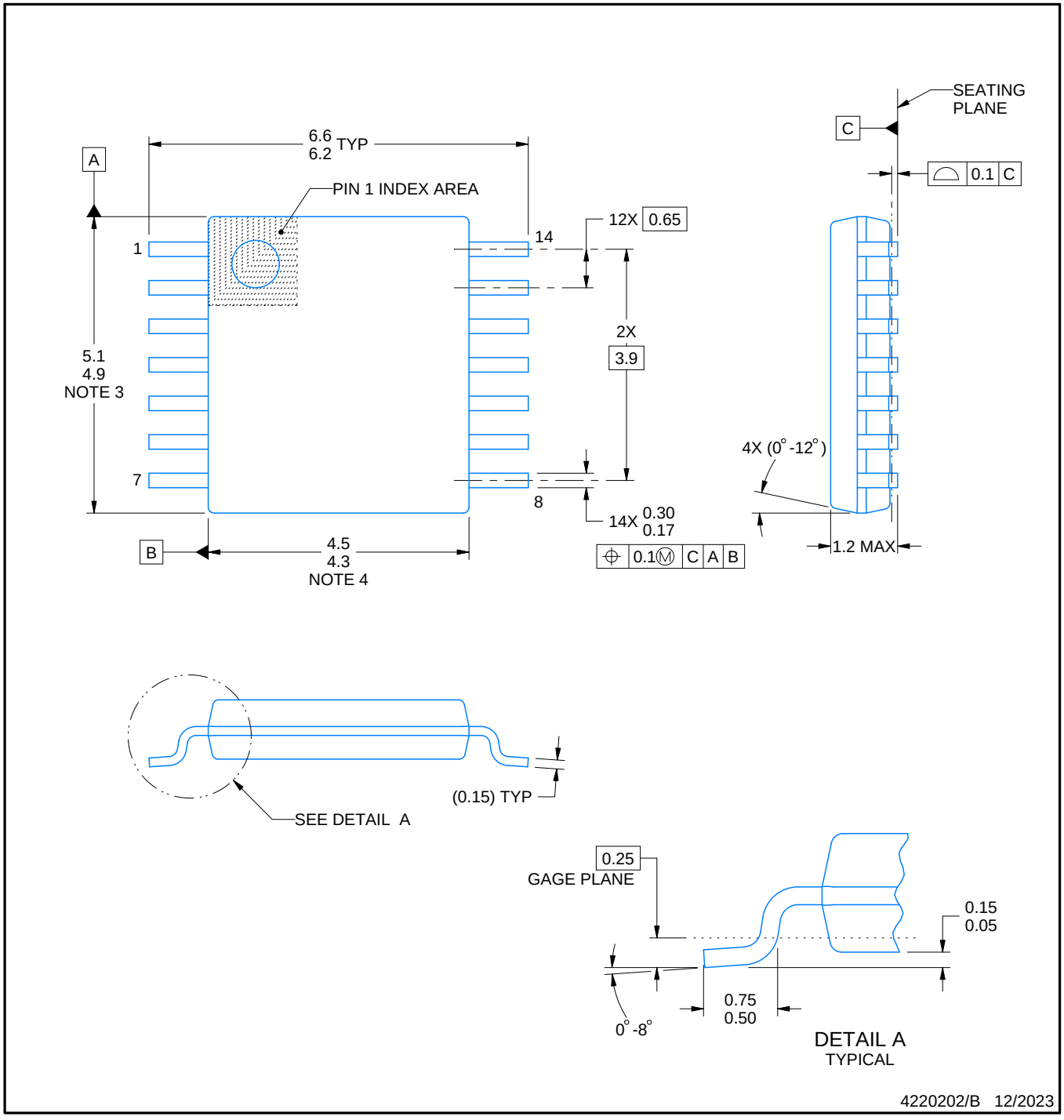
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

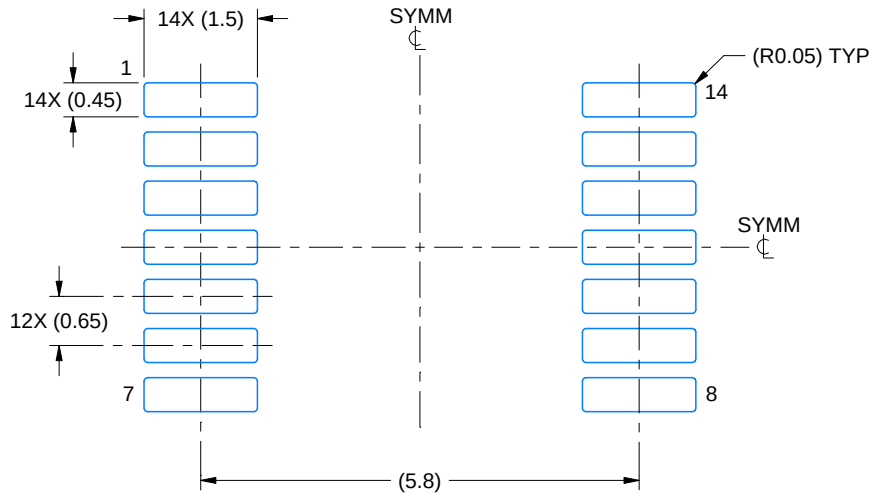
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

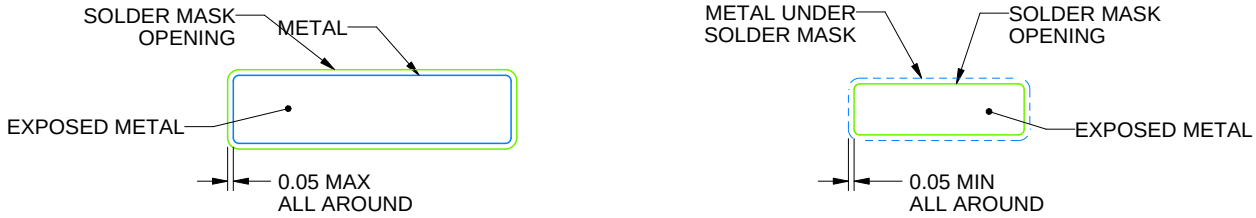


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

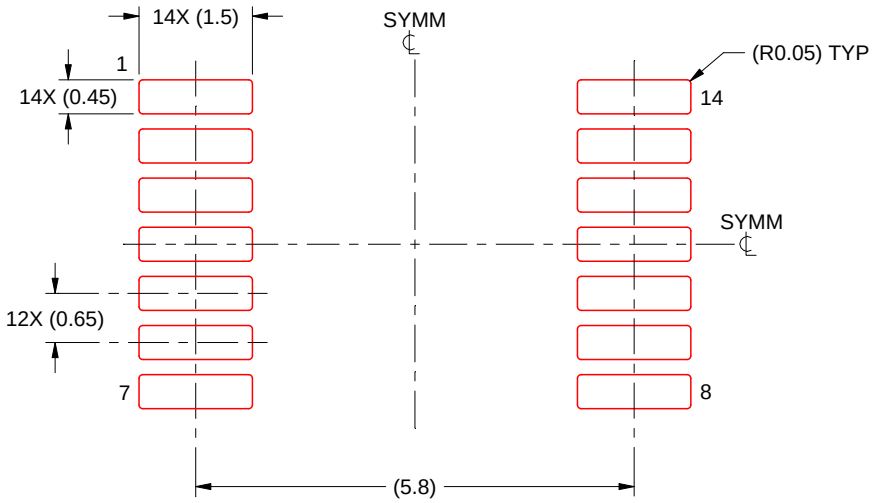


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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