

# DATA SHEET

## **74LVT162374**

**3.3V LVT 16-bit edge-triggered D-type  
flip-flop with 30  $\Omega$  termination resistors  
(3-State)**

Product specification

1999 Sep 23

IC23 Data Handbook

## 3.3V 16-bit edge-triggered D-type flip-flop with 30 $\Omega$ termination resistors (3-State)

# 74LVT162374

### FEATURES

- 16-bit edge-triggered flip-flop
- 3-State buffers
- Output capability: +12 mA / -12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30  $\Omega$  making external resistors unnecessary
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

### DESCRIPTION

The 74LVT162374 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

The 74LVT162374 is designed with 30  $\Omega$  series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	$C_L = 50\text{pF}$ ; $V_{CC} = 3.3\text{V}$	2.9	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $3.0\text{V}$	3	pF
$C_{OUT}$	Output pin capacitance	Outputs disabled; $V_O = 0\text{V}$ or $3.0\text{V}$	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	70	$\mu\text{A}$

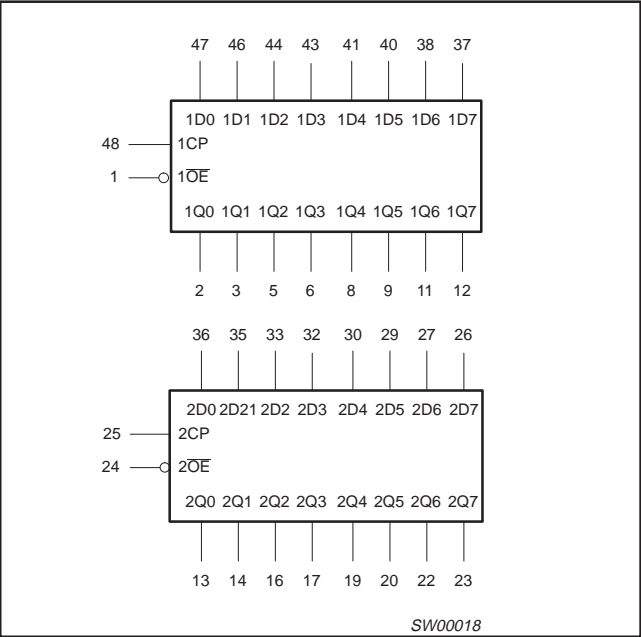
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDERING CODE	DWG NUMBER
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT162374 DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT162374 DGG	SOT362-1

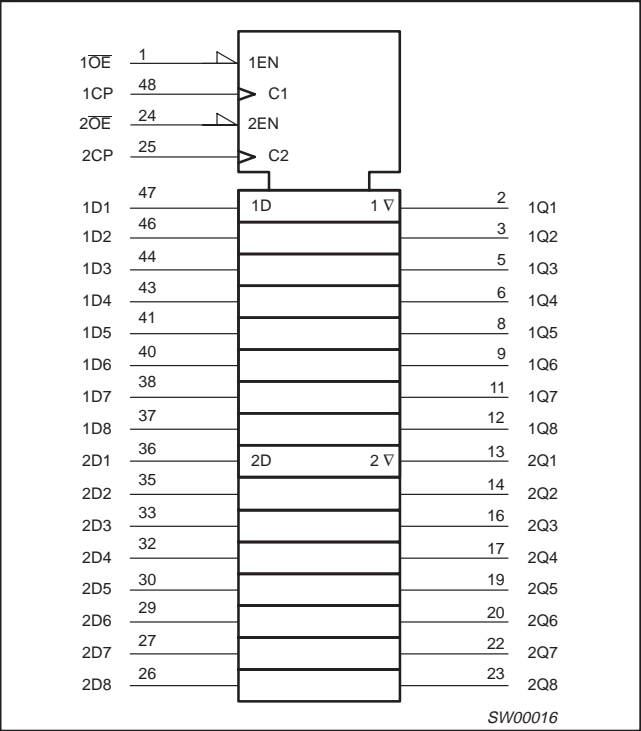
3.3V 16-bit edge-triggered D-type flip-flop with  
30 Ω termination resistors (3-State)

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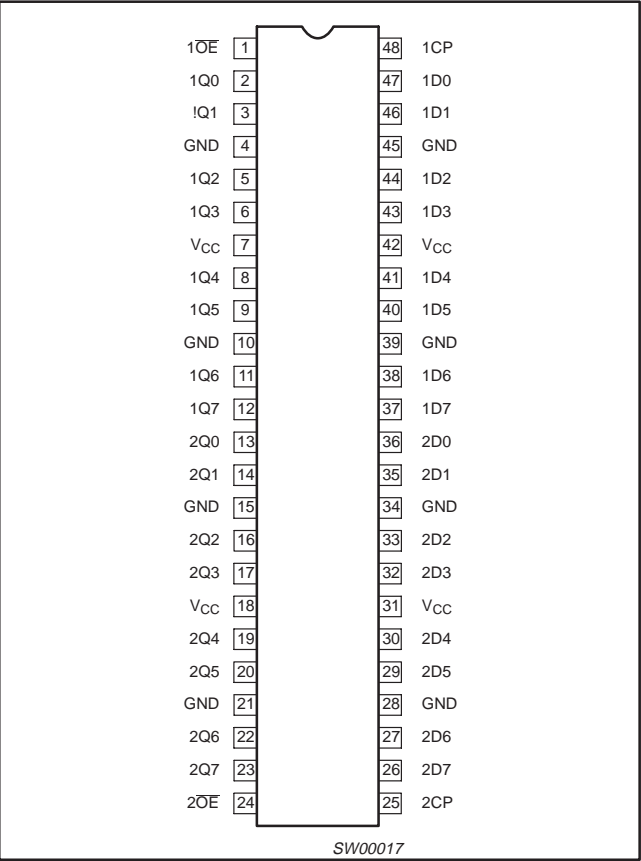
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



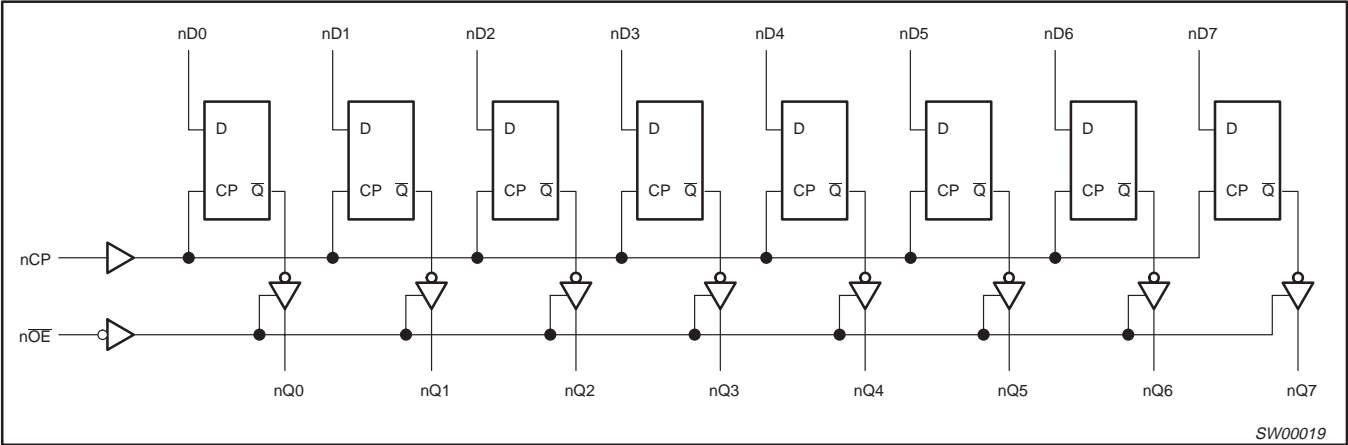
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 - 1D7 2D0 - 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 - 1Q7 2Q0 - 2Q7	Data outputs
1, 24	1OE, 2OE	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage

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LOGIC DIAGRAM

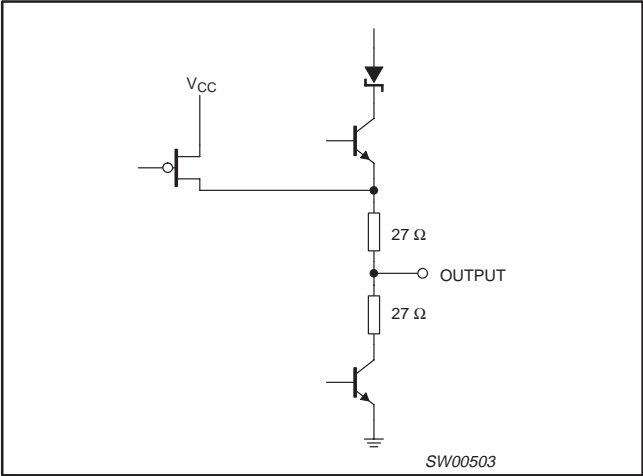


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 - nQ7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	nDx	nDx	Z	

H = High voltage level  
h = High voltage level one set-up time prior to the High-to-Low E transition  
L = Low voltage level  
l = Low voltage level one set-up time prior to the High-to-Low E transition  
NC= No change  
X = Don't care  
Z = High impedance "off" state  
↑ = Low-to-High clock transition  
↕ = Not a Low-to-High clock transition

SCHEMATIC OF EACH OUTPUT



# 3.3V 16-bit edge-triggered D-type flip-flop with 30 $\Omega$ termination resistors (3-State)

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
$I_{OUT}$	DC output current	Output in Low state	128	mA
		Output in High state	-64	
$T_{stg}$	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	2.7	3.6	V
$V_I$	Input voltage	0	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Input voltage		0.8	V
$I_{OH}$	High-level output current		-12	mA
$I_{OL}$	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

# 3.3V 16-bit edge-triggered D-type flip-flop with 30 $\Omega$ termination resistors (3-State)

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = −18 mA			−0.85	−1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = −12 mA		2.0			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 12 mA				0.8	V
V <sub>RST</sub>	Power-up output Low voltage <sup>5</sup>	V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>			0.1	0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		0.1	±1	μA
		V <sub>CC</sub> = 0 or 3.6 V; V <sub>I</sub> = 5.5 V			0.4	10	
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>	Data pins <sup>4</sup>		0.1	1	
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V			−0.4	−5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V			0.1	±100	μA
I <sub>HOLD</sub>	Bus Hold current D inputs <sup>7</sup>	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V		75	135		μA
		V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V		−75	−135		
		V <sub>CC</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 3.6 V		±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V			50	125	μA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care			1	±100	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.5	5	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>			0.5	−5	
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6 V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0			0.07	0.12	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6 V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0			4	6	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6 V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>6</sup>			0.07	0.12	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3 V to 3.6 V; One input at V <sub>CC</sub> -0.6 V, Other inputs at V <sub>CC</sub> or GND			0.1	0.2	mA

### NOTES:

1. All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25^\circ\text{C}$ .
2. This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.
3. This parameter is valid for any  $V_{CC}$  between 0V and 1.2V with a transition time of up to 10 msec. From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of 100  $\mu\text{sec}$  is permitted. This parameter is valid for  $T_{amb} = 25^\circ\text{C}$  only.
4. Unused pins at  $V_{CC}$  or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6.  $I_{CCZ}$  is measured with outputs pulled to  $V_{CC}$  or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

# 3.3V 16-bit edge-triggered D-type flip-flop with 30 $\Omega$ termination resistors (3-State)

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## AC CHARACTERISTICS

GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$f_{max}$	Maximum clock frequency	1	150				MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	1	1.5 1.5	3.0 3.0	5.3 4.9	6.2 5.1	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to High and Low level	3 4	1.5 1.5	3.5 3.2	5.6 4.9	6.9 6.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from High and Low Level	3 4	1.5 1.5	3.5 3.2	5.4 5.0	5.7 5.1	ns

### NOTE:

1. All typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_{amb} = 25^\circ\text{C}$ .

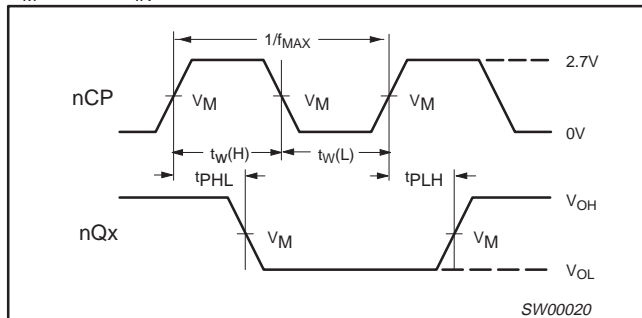
## AC SETUP REQUIREMENTS

GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

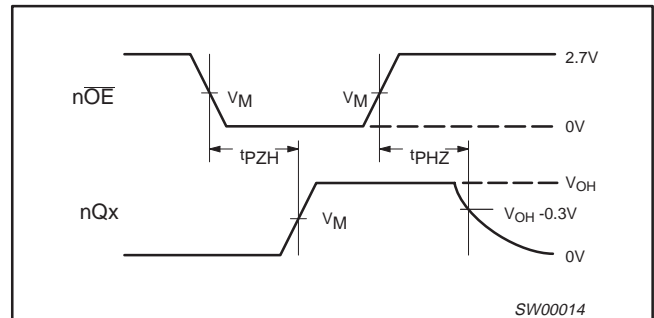
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time nDx to nCP	2	2.5 2.5	0.7 0.7	2.5 2.5	ns
$t_H(H)$ $t_H(L)$	Hold time nDx to nCP	2	0.5 0.5	0 0	0 0	ns
$t_W(H)$ $t_W(L)$	nCP pulse width High or Low	1	1.5 3.0	0.6 1.6	1.5 3.0	ns

## AC WAVEFORMS

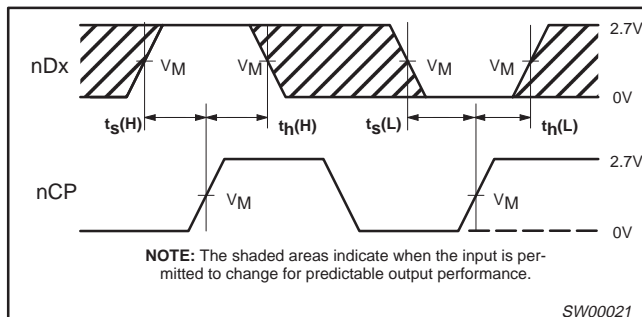
$V_M = 1.5 \text{ V}$ ,  $V_{IN} = \text{GND to } 3.0 \text{ V}$



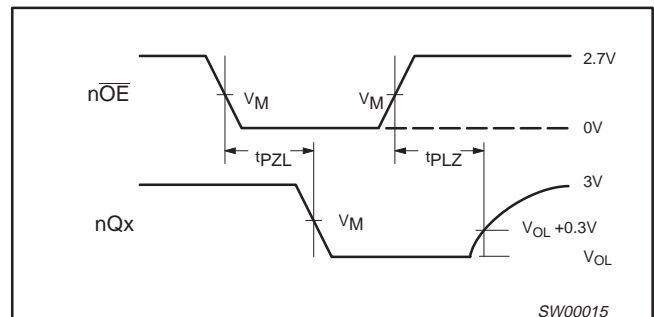
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Setup and Hold Times

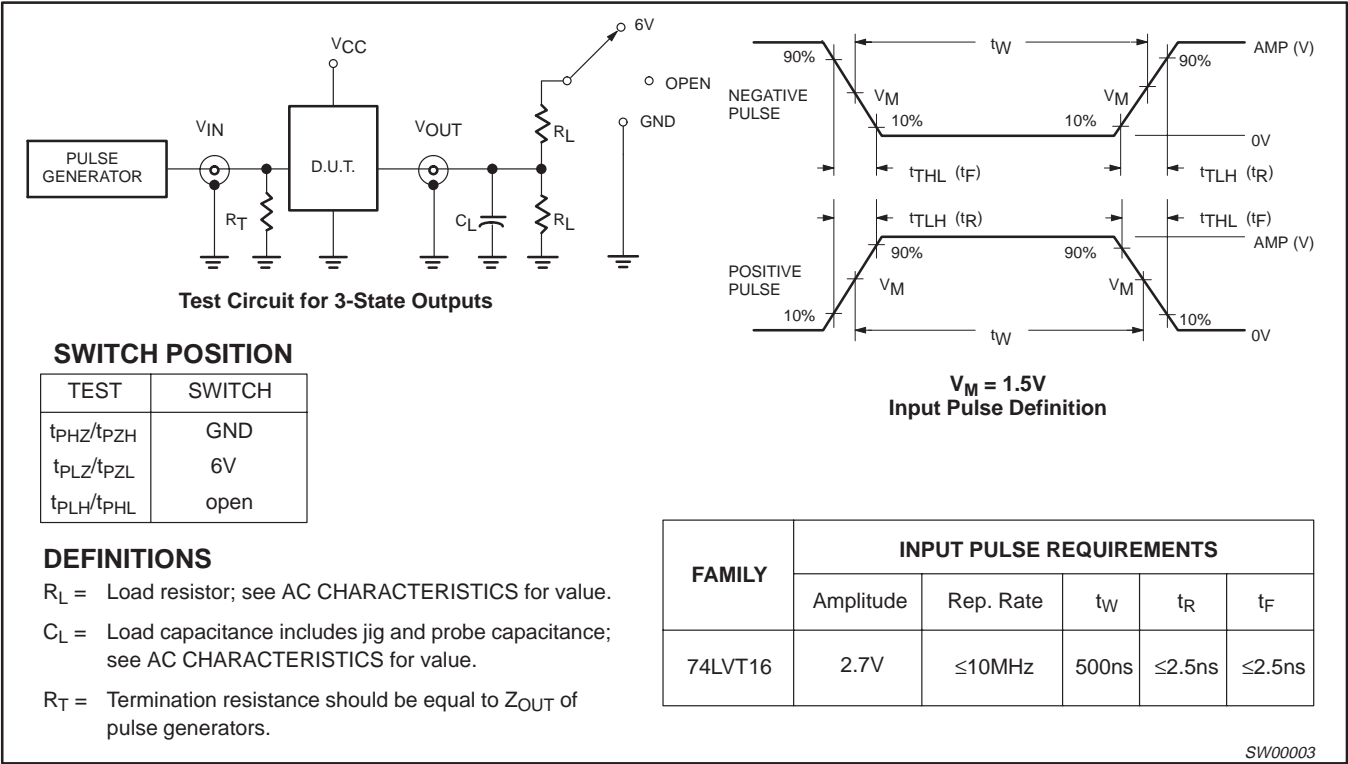


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

3.3V 16-bit edge-triggered D-type flip-flop with  
30 Ω termination resistors (3-State)

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TEST CIRCUIT AND WAVEFORMS



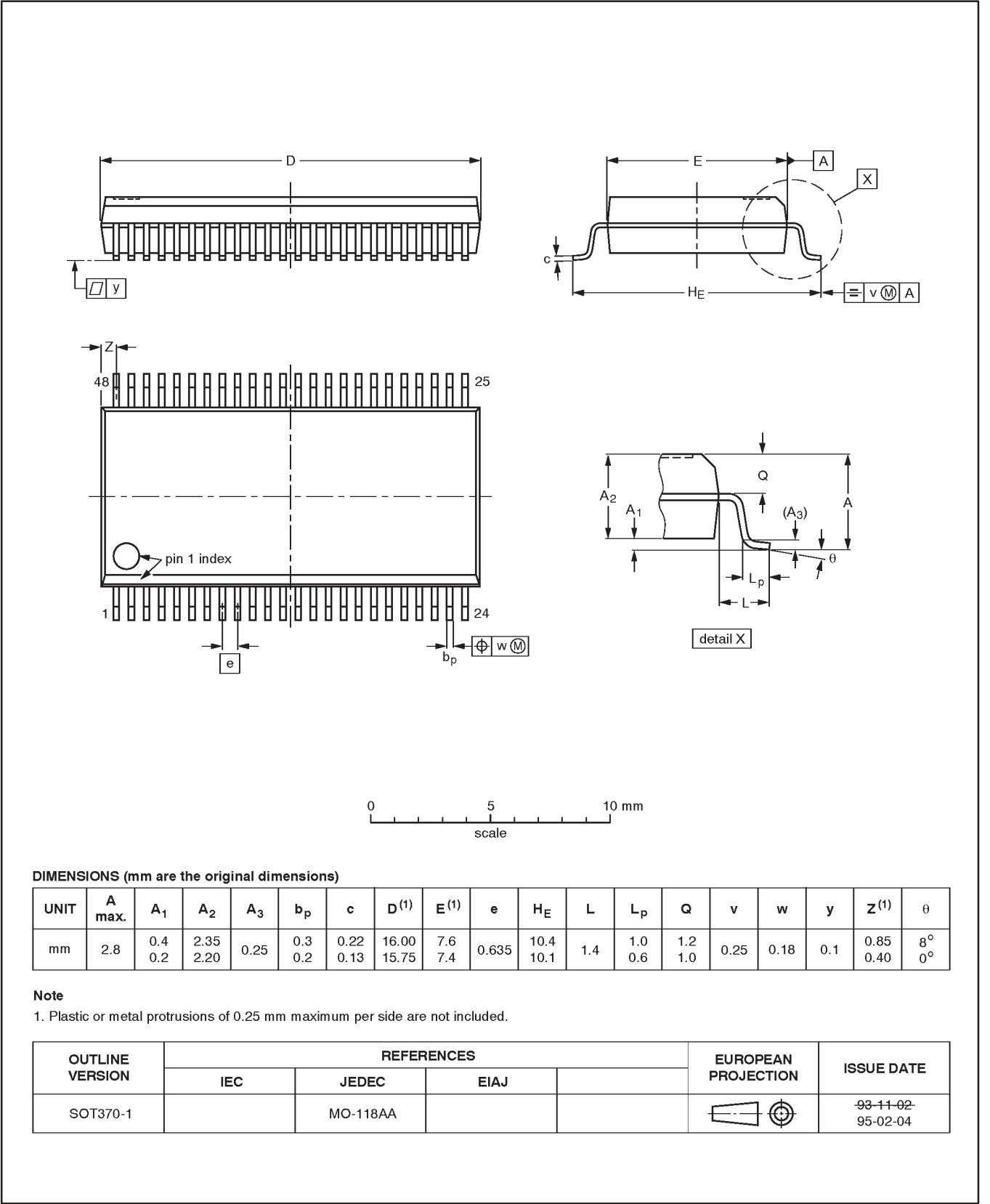


3.3V 16-bit edge-triggered D-type flip-flop with  
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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

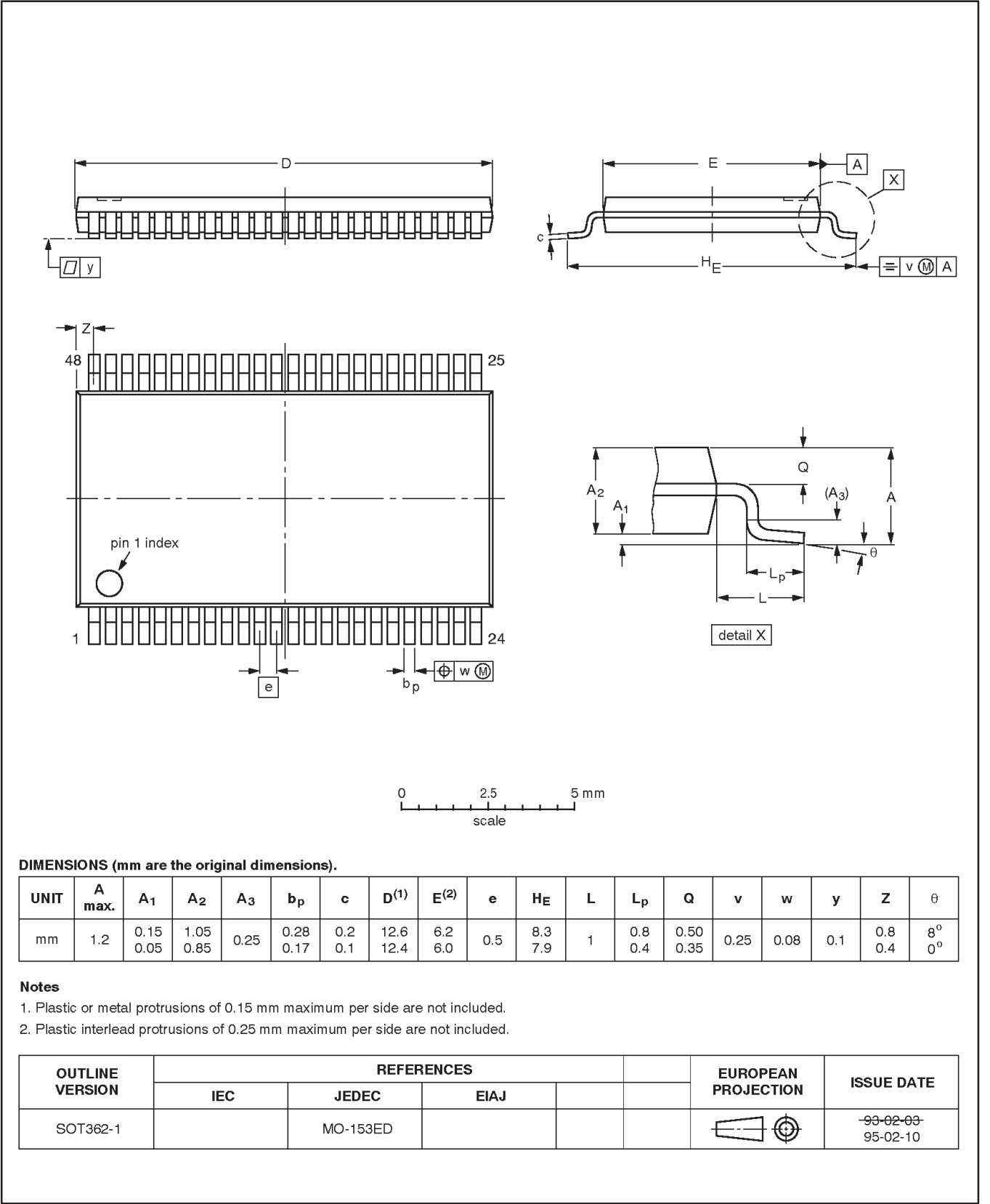


3.3V 16-bit edge-triggered D-type flip-flop with  
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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



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3.3V 16-bit edge-triggered D-type flip-flop with  
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## NOTES

# 3.3V 16-bit edge-triggered D-type flip-flop with 30 $\Omega$ termination resistors (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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