



# T-SMINTI 4B3T Second Gen. Modular ISDN NT (Intelligent) PEF 82902 Version 1.1

Wired  
Communications



Never stop thinking.

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# T-SMINTI

## 4B3T Second Gen.

### Modular ISDN NT

### (Intelligent)

PEF 82902 Version 1.1

Wired  
Communications



Never stop thinking.

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# 1 Overview

The **PEB 82902** (T-SMINT<sup>®</sup>I) offers U-transceiver, S-transceiver and an IOM<sup>®</sup>-2 interface. A microcontroller interface provides access to both transceivers as well as the IOM<sup>®</sup>-2 interface.

However, as opposed to its bigger brother T-SMINT<sup>®</sup>IX, the T-SMINT<sup>®</sup>I does not have an HDLC controller. Main target applications of the T-SMINT<sup>®</sup>I are intelligent NT applications where the HDLC controller(s) is (are) provided by the microcontroller. An example for such a microcontroller is the Infineon UTAH chip which features four flexible HDLC controllers.

**Table 1** on **Page 1** summarizes the 2nd generation NT products.

**Table 1 NT Products of the 2nd Generation**

|                                                                                                                 | <b>PEF 80902</b>            | <b>PEF 81902</b>                         | <b>PEF 82902</b>                         |
|-----------------------------------------------------------------------------------------------------------------|-----------------------------|------------------------------------------|------------------------------------------|
|                                                                                                                 | <b>T-SMINT<sup>®</sup>O</b> | <b>T-SMINT<sup>®</sup>IX</b>             | <b>T-SMINT<sup>®</sup>I</b>              |
| Package                                                                                                         | P-MQFP-44                   | P-MQFP-64<br>P-TQFP-64                   | P-MQFP-64<br>P-TQFP-64                   |
| Register access                                                                                                 | no                          | U+S+HDLC+ IOM <sup>®</sup> -2            | U+S+IOM <sup>®</sup> -2                  |
| Access via                                                                                                      | n.a                         | parallel (or SCI or IOM <sup>®</sup> -2) | parallel (or SCI or IOM <sup>®</sup> -2) |
| MCLK, watchdogtimer, SDS, BCL, D-channel arbitration, IOM <sup>®</sup> -2 access and manipulation etc. provided | no                          | yes                                      | yes                                      |
| HDLC controller                                                                                                 | no                          | yes                                      | no                                       |
| NT1 mode available                                                                                              | yes (only)                  | no                                       | no                                       |

## 1.1 References

- [1] TS 102 080, Transmission and Multiplexing; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998
- [2] FTZ 1 TR 220 Technische Richtlinie, Spezifikation der ISDN Schnittstelle Uk0 Schicht 1, Deutsche Telecom AG, August 1991
- [3] TS 0284/96 Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b (ohne Internverkehr), Deutsche Telekom AG, März 2001
- [4] pr ETS 300 012 Draft, ISDN; Basic User Network Interface (UNI), ETSI, November 1996
- [5] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991
- [6] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988
- [7] IEC-T, ISDN Echocancellation Circuit, PEB 20901 (IEC - TD) / PEB 20902 (IEC - TA), preliminary Target Specification 11.88, Siemens AG, 1988
- [8] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996
- [9] NTC-T, Network Termination Controller (4B3T), PEB 8090 V1.1, Data Sheet 06.98, Siemens AG, 1998
- [10] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997
- [11] Q-SMINTO, 2B1Q Second Gen. **Modular ISDN NT (Ordinary)**, PEF 80912  
Q-SMINTIX, 2B1Q Second Gen. **Modular ISDN NT (Intelligent eXtended)**, PEF 81912  
Q-SMINTI, 2B1Q Second Gen. **Modular ISDN NT (Intelligent)**, PEF 82912 V1.3, Data Sheets 03.01, Infineon AG, 2001
- [12] IOM<sup>®</sup>-2 Interface Reference Guide, Siemens AG, 03.91
- [13] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.1, Preliminary Data Sheet 08.98, Infineon Technologies AG, 1999
- [14] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September 1997
- [15] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

# T-SMINT®I

## 4B3T Second Gen. Modular ISDN NT (Intelligent)

PEF 82902

Version 1.1

CMOS

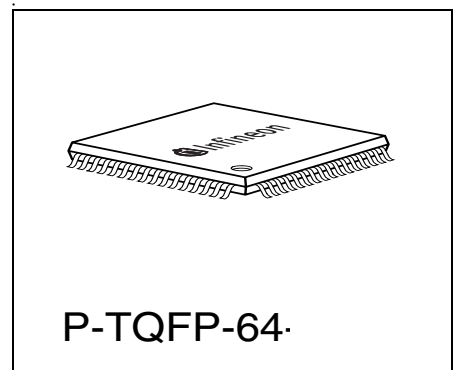
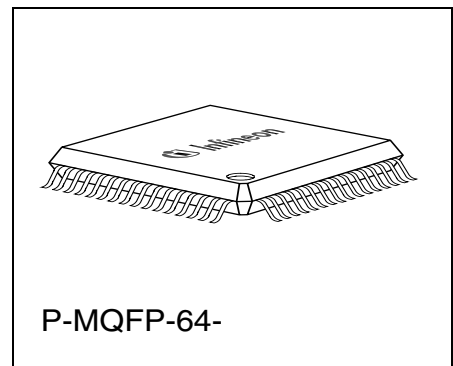
### 1.2 Features

#### Features known from the PEB 8090

- U-transceiver and S-transceiver on one chip
- U-interface (4B3T) conform to ETSI [1] and FTZ [2]:
  - Meets all transmission requirements on all ETSI and FTZ loops with margin
- S/T-interface conform to ETSI [4], ANSI [5] and ITU [6]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Access to IOM®-2 C/I and Monitor channels
- Power-on reset and Undervoltage Detection with no external components
- ESD robustness 2kV

#### New Features

- Conforms to 'Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b' of Deutsche Telekom AG [3]
- Perfectly suited for high-end intelligent NTs that require multiple HDLC controllers
- Pin compatible with Q-SMINT®I (2nd Generation)
- Parallel or serial µP-interface
  - Siemens/Intel non-multiplexed (direct or indirect addressing (SCOUT))
  - Siemens/Intel multiplexed
  - Motorola
  - programmable MCLK (can be disabled) (SCOUT)



| Type      | Package   |
|-----------|-----------|
| PEF 82902 | P-MQFP-64 |
| PEF 82902 | P-TQFP-64 |

- Enhanced IOM<sup>®</sup>-2 interface
  - Timeslot access and manipulation (SCOUT)
  - BCL output; programmable and flexible strobes SDS1/2, e.g. active during several timeslots.
  - Optional: All registers can be read and written to via new Monitor channel concept
  - External Awake ( $\overline{\text{EAW}}$ )
- Optional: Implementation of S-transceiver statemachine in software
- Power Down and reset states (e.g. S-transceiver) for individual circuits
- Automatic D-channel arbitration between S-bus and external HDLC controller
- Priority setting (8/10) for off-chip HDLC controller
- Pin Vref and the according external capacitor removed
- Inputs accept 3.3V and 5V
- I/O (open drain) accepts pull-up to 3.3V<sup>1)</sup>
- Lowest power consumption due to
  - Low power CMOS technology (0.35μ)
  - Newly optimized low power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply

### 1.3 Not Supported are ...

- No integrated hybrid is provided by the T-SMINT<sup>®</sup>I. Therefore, an external hybrid is always required, which consists of only two additional resistors as compared to an integrated hybrid, but allows for more flexibility in board design.
- On-chip HDLC controller
- Auxiliary IOM<sup>®</sup>-2 interface
- SRA (capacitive receiver coupling is not suited for S-feeding)
- NT-Star with star point on the IOM<sup>®</sup>-2 bus (already not supported in NTC-T).
- No access to S2-5 channels. Access only to S1 and Q channel as in Scout-S. No selection between transparent and non-auto mode provided.

<sup>1)</sup> Pull-ups to 5V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

## 1.4 Pin Configuration

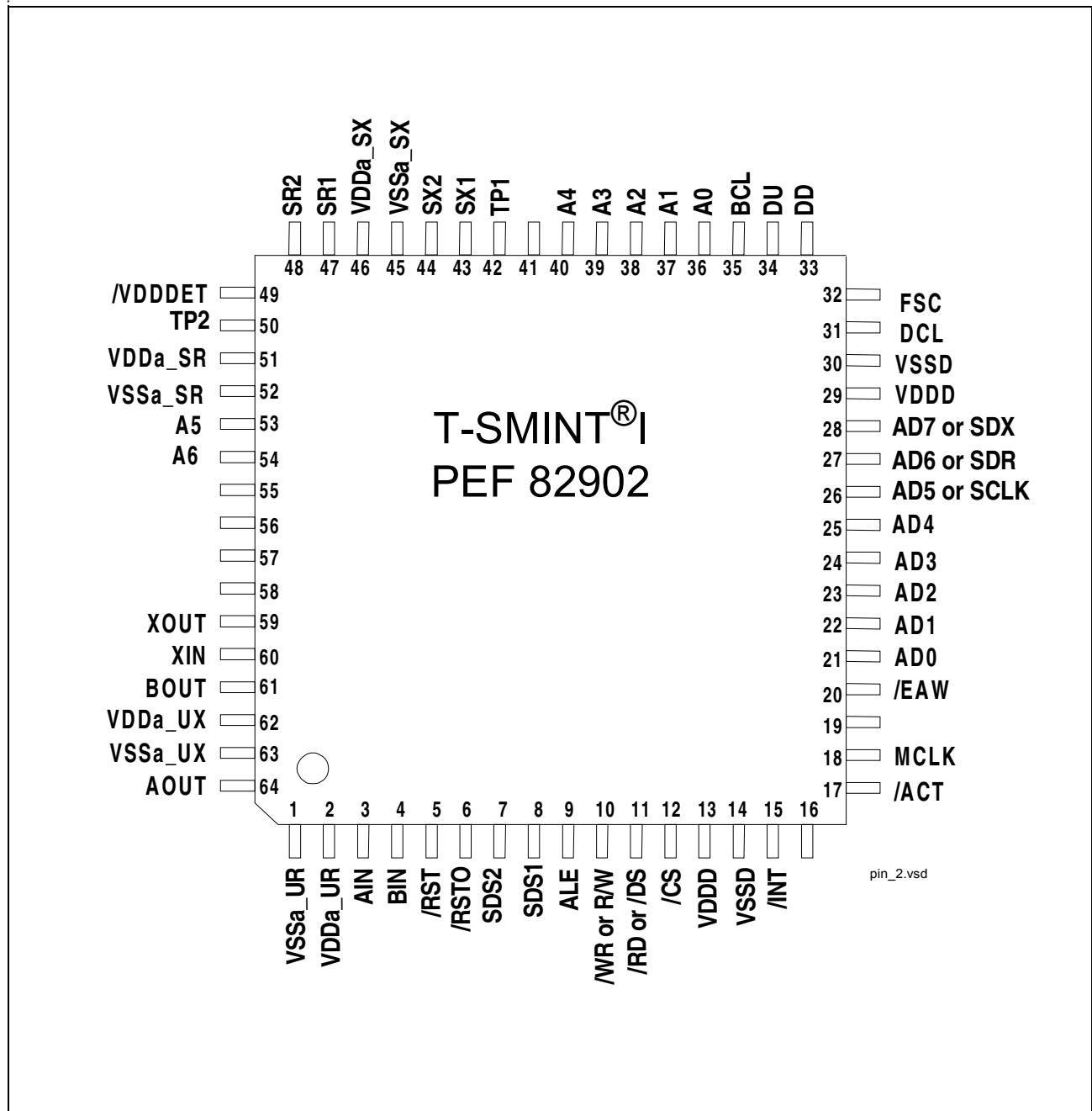


Figure 1 Pin Configuration

## 1.5 Block Diagram

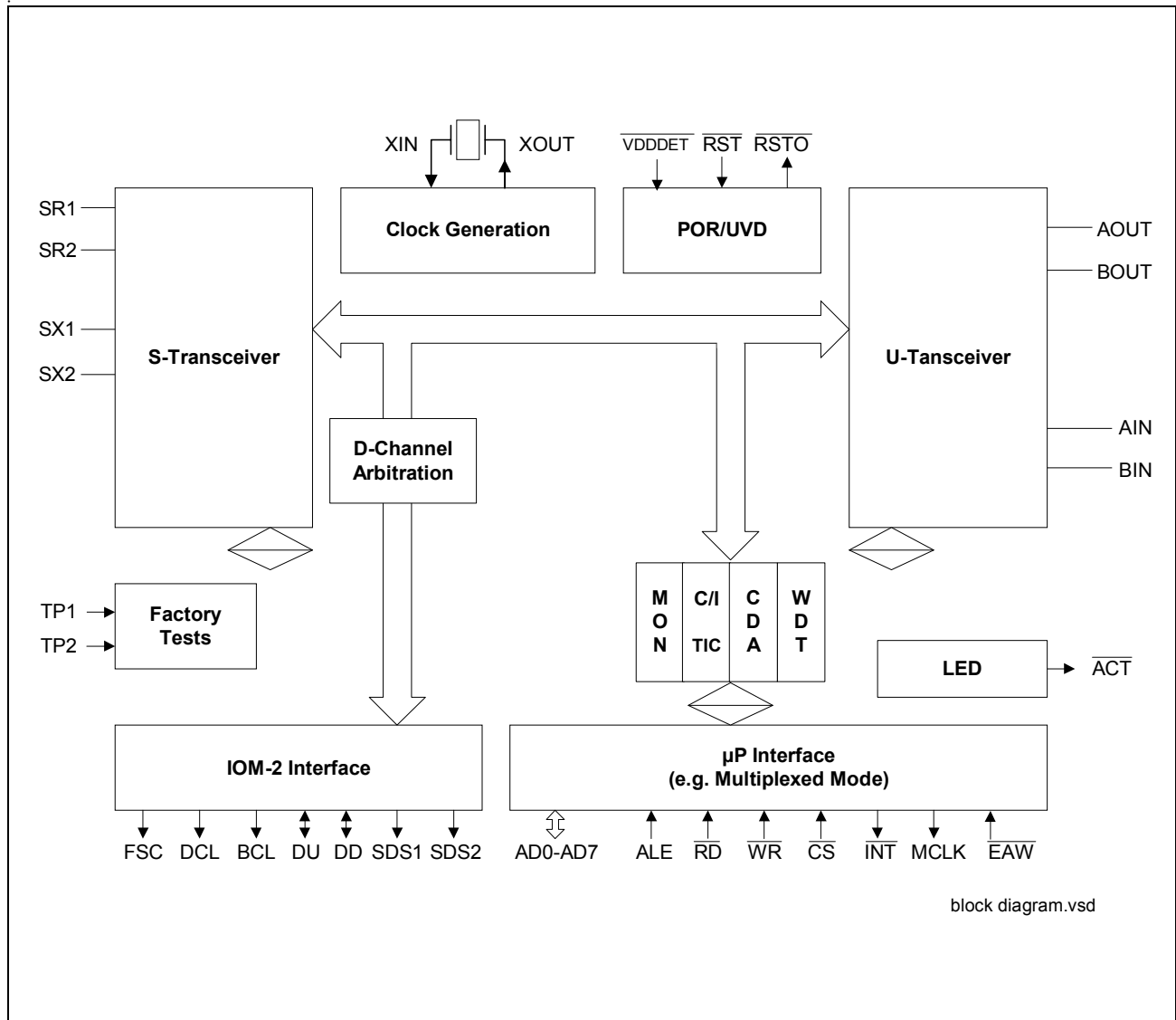


Figure 2 Block Diagram

## 1.6 Pin Definitions and Functions

**Table 2 Pin Definitions and Functions**

|  | Pin | Symbol  | Type      | Function                                                                                          |
|--|-----|---------|-----------|---------------------------------------------------------------------------------------------------|
|  | 2   | VDDa_UR | –         | Supply voltage for U-Receiver<br>(3.3 V $\pm$ 5 %)                                                |
|  | 1   | VSSa_UR | –         | Analog ground (0 V) U-Receiver                                                                    |
|  | 62  | VDDa_UX | –         | Supply voltage for U-Transmitter<br>(3.3 V $\pm$ 5 %)                                             |
|  | 63  | VSSa_UX | –         | Analog ground (0 V) U-Transmitter                                                                 |
|  | 51  | VDDa_SR | –         | Supply voltage for S-Receiver<br>(3.3 V $\pm$ 5 %)                                                |
|  | 52  | VSSa_SR | –         | Analog ground (0 V) S-Receiver                                                                    |
|  | 46  | VDDa_SX | –         | Supply voltage for S-Transmitter<br>(3.3 V $\pm$ 5 %)                                             |
|  | 45  | VSSa_SX | –         | Analog ground (0 V) S-Transmitter                                                                 |
|  | 29  | VDDD    | –         | Supply voltage digital circuits<br>(3.3 V $\pm$ 5 %)                                              |
|  | 30  | VSSD    | –         | Ground (0 V) digital circuits                                                                     |
|  | 13  | VDDD    | –         | Supply voltage digital circuits<br>(3.3 V $\pm$ 5 %)                                              |
|  | 14  | VSSD    | –         | Ground (0 V) digital circuits                                                                     |
|  | 32  | FSC     | O         | <b>Frame Sync:</b><br>8-kHz frame synchronization signal                                          |
|  | 31  | DCL     | O         | <b>Data Clock:</b><br>IOM <sup>®</sup> -2 interface clock signal (double clock):<br>1.536 MHz     |
|  | 35  | BCL     | O         | <b>Bit Clock:</b><br>The bit clock is identical to the IOM <sup>®</sup> -2 data rate<br>(768 kHz) |
|  | 33  | DD      | I/O<br>OD | <b>Data Downstream:</b><br>Data on the IOM <sup>®</sup> -2 interface                              |
|  | 34  | DU      | I/O<br>OD | <b>Data Upstream:</b><br>Data on the IOM <sup>®</sup> -2 interface                                |

**Table 2 Pin Definitions and Functions (cont'd)**

|  | Pin | Symbol                 | Type | Function                                                                                                                                                                                                                            |
|--|-----|------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | 8   | SDS1                   | O    | <b>Serial Data Strobe1:</b><br>Programmable strobe signal for time slot and/or D-channel indication on IOM <sup>®</sup> -2                                                                                                          |
|  | 7   | SDS2                   | O    | <b>Serial Data Strobe2:</b><br>Programmable strobe signal for time slot and/or D-channel indication on IOM <sup>®</sup> -2                                                                                                          |
|  | 12  | $\overline{\text{CS}}$ | I    | <b>Chip Select:</b><br>A low level indicates a microcontroller access to the T-SMINT <sup>®</sup> I                                                                                                                                 |
|  | 26  | SCLK                   | I    | <b>Serial Clock:</b><br>Clock signal of the SCI interface if a serial interface is selected                                                                                                                                         |
|  | 26  | AD5                    | I/O  | <b>Multiplexed Bus Mode:</b><br><b>Address/data bus</b><br>Address/data line AD5 if the parallel interface is selected<br><b>Non-Multiplexed Bus Mode:</b><br><b>Data bus</b><br>Data line D5 if the parallel interface is selected |
|  | 27  | SDR                    | I    | <b>Serial Data Receive:</b><br>Receive data line of the SCI interface if a serial interface is selected                                                                                                                             |
|  | 27  | AD6                    | I/O  | <b>Multiplexed Bus Mode:</b><br><b>Address/data bus</b><br>Address/data line AD6 if the parallel interface is selected<br><b>Non-Multiplexed Bus Mode:</b><br><b>Data bus</b><br>Data line D6 if the parallel interface is selected |

**Table 2 Pin Definitions and Functions (cont'd)**

|  | Pin | Symbol                 | Type | Function                                                                                                                                                                                                                                                                                                                                                            |
|--|-----|------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | 28  | SDX                    | OD/O | <b>Serial Data Transmit:</b><br>Transmit data line of the SCI interface if a serial interface is selected                                                                                                                                                                                                                                                           |
|  | 28  | AD7                    | I/O  | <b>Multiplexed Bus Mode:</b><br><b>Address/data bus</b><br>Address/data line AD7 if the parallel interface is selected<br><b>Non-Multiplexed Bus Mode:</b><br><b>Data bus</b><br>Data line D7 if the parallel interface is selected                                                                                                                                 |
|  | 21  | AD0                    | I/O  | <b>Multiplexed Bus Mode:</b><br><b>Address/data bus</b><br>Transfers addresses from the microcontroller to the T-SMINT <sup>®</sup> I and data between the microcontroller and the T-SMINT <sup>®</sup> I.<br><b>Non-Multiplexed Bus Mode:</b><br><b>Data bus.</b><br>Transfers data between the microcontroller and the T-SMINT <sup>®</sup> I (data lines D0-D4). |
|  | 22  | AD1                    | I/O  |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 23  | AD2                    | I/O  |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 24  | AD3                    | I/O  |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 25  | AD4                    | I/O  |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 36  | A0                     | I    | <b>Non-Multiplexed Bus Mode:</b><br>Address bus transfers addresses from the microcontroller to the T-SMINT <sup>®</sup> I. For indirect address mode only A0 is valid.<br><b>Multiplexed Bus Mode</b><br>Not used in multiplexed bus mode. In this case A0-A6 should directly be connected to VDD.                                                                 |
|  | 37  | A1                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 38  | A2                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 39  | A3                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 40  | A4                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 53  | A5                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 54  | A6                     | I    |                                                                                                                                                                                                                                                                                                                                                                     |
|  | 11  | $\overline{\text{RD}}$ | I    | <b>Read</b><br>Indicates a read access to the registers (Intel bus mode).                                                                                                                                                                                                                                                                                           |
|  |     | $\overline{\text{DS}}$ | I    | <b>Data Strobe</b><br>The rising edge marks the end of a valid read or write operation (Motorola bus mode).                                                                                                                                                                                                                                                         |

## Overview

Table 2 Pin Definitions and Functions (cont'd)

|  | Pin | Symbol                                  | Type       | Function                                                                                                                                                                                                                                            |
|--|-----|-----------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | 10  | $\overline{WR}$<br><br>$R/\overline{W}$ | I<br><br>I | <b>Write</b><br>Indicates a write access to the registers (Intel bus mode).<br><b>Read/Write</b><br>A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).    |
|  | 9   | ALE                                     | I          | <b>Address Latch Enable</b><br>An address on the external address/data bus (multiplexed bus type only) is latched with the falling edge of ALE.<br>ALE also selects the microcontroller interface type (multiplexed or non multiplexed).            |
|  | 5   | $\overline{RST}$                        | I          | <b>Reset:</b><br>Low active reset input. Schmitt-Trigger input with hysteresis of typical 360mV. Tie to '1' if not used.                                                                                                                            |
|  | 6   | $\overline{RSTO}$                       | OD         | <b>Reset Output:</b><br>Low active reset output.                                                                                                                                                                                                    |
|  | 15  | $\overline{INT}$                        | OD         | <b>Interrupt Request:</b><br>$\overline{INT}$ becomes active if the T-SMINT <sup>®</sup> I requests an interrupt.                                                                                                                                   |
|  | 18  | MCLK                                    | O          | <b>Microcontroller Clock:</b><br>Clock output for the microcontroller                                                                                                                                                                               |
|  | 20  | $\overline{EAW}$                        | I          | <b>External Awake:</b><br>A low level on $\overline{EAW}$ during power down activates the clock generation of the T-SMINT <sup>®</sup> I, i.e. the IOM <sup>®</sup> -2 interface provides FSC, DCL and BCL for read and write access. <sup>1)</sup> |
|  | 43  | SX1                                     | O          | <b>S-Bus Transmitter Output (positive)</b>                                                                                                                                                                                                          |
|  | 44  | SX2                                     | O          | <b>S-Bus Transmitter Output (negative)</b>                                                                                                                                                                                                          |
|  | 47  | SR1                                     | I          | <b>S-Bus Receiver Input</b>                                                                                                                                                                                                                         |

## Overview

**Table 2 Pin Definitions and Functions (cont'd)**

|  | Pin               | Symbol                     | Type | Function                                                                                                                                                                                                                                                       |
|--|-------------------|----------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | 48                | SR2                        | I    | <b>S-Bus Receiver Input</b>                                                                                                                                                                                                                                    |
|  | 60                | XIN                        | I    | <b>Crystal 1:</b><br>Connected to a 15.36 MHz crystal                                                                                                                                                                                                          |
|  | 59                | XOUT                       | O    | <b>Crystal 2:</b><br>Connected to a 15.36 MHz crystal                                                                                                                                                                                                          |
|  | 64                | AOUT                       | O    | <b>Differential U-interface Output</b>                                                                                                                                                                                                                         |
|  | 61                | BOUT                       | O    | <b>Differential U-interface Output</b>                                                                                                                                                                                                                         |
|  | 3                 | AIN                        | I    | <b>Differential U-interface Input</b>                                                                                                                                                                                                                          |
|  | 4                 | BIN                        | I    | <b>Differential U-interface Input</b>                                                                                                                                                                                                                          |
|  | 49                | $\overline{\text{VDDDET}}$ | I    | <b>VDD Detection:</b><br>This pin selects if the $V_{DD}$ detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$ . |
|  | 17                | $\overline{\text{ACT}}$    | O    | <b>Activation LED.</b><br>Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4mA).                                                                                                                                             |
|  | 42                | TP1                        | I    | <b>Test Pin 1.</b><br>Used for factory device test.<br>Tie to 'V <sub>SS</sub> '                                                                                                                                                                               |
|  | 50                | TP2                        | I    | <b>Test Pin 2.</b><br>Used for factory device test.<br>Tie to 'V <sub>SS</sub> '                                                                                                                                                                               |
|  | 16, 19,<br>41, 55 |                            |      | Tie to '1'                                                                                                                                                                                                                                                     |
|  | 56, 57,<br>58     | res                        |      | <b>Reserved</b><br>These pins are reserved for future use. Do not connect.                                                                                                                                                                                     |

<sup>1)</sup> This function of pin  $\overline{\text{EAW}}$  is different to that defined in Ref. [13]

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

## 1.6.1 Specific Pins and Test Modes

### LED Pin $\overline{\text{ACT}}$

A LED can be connected to pin  $\overline{\text{ACT}}$  to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to [Table 3](#). or it is programmable via two bits (LED1 and LED2 in register MODE2).

**Table 3** **ACT States**

| Pin $\overline{\text{ACT}}$ | LED           | U_Deactivated | U_Activated | S_Activated |
|-----------------------------|---------------|---------------|-------------|-------------|
| V <sub>DD</sub>             | OFF           | 1             | x           | x           |
| 2Hz (1 : 1)*                | fast flashing | 0             | 0           | x           |
| 1Hz (3 : 1)*                | slow flashing | 0             | 1           | 0           |
| GND                         | ON            | 0             | 1           | 1           |

Note: \* denotes the duty cycle 'high' : 'low'.

with:

**U\_Deactivated:** 'Deactivated State' as defined in [Chapter 2.4.7.6](#).

**U\_Activated:** 'SBC Synchronizing', 'Wait for Info U4H', and 'Transparent' as defined in [Chapter 2.4.7.6](#).

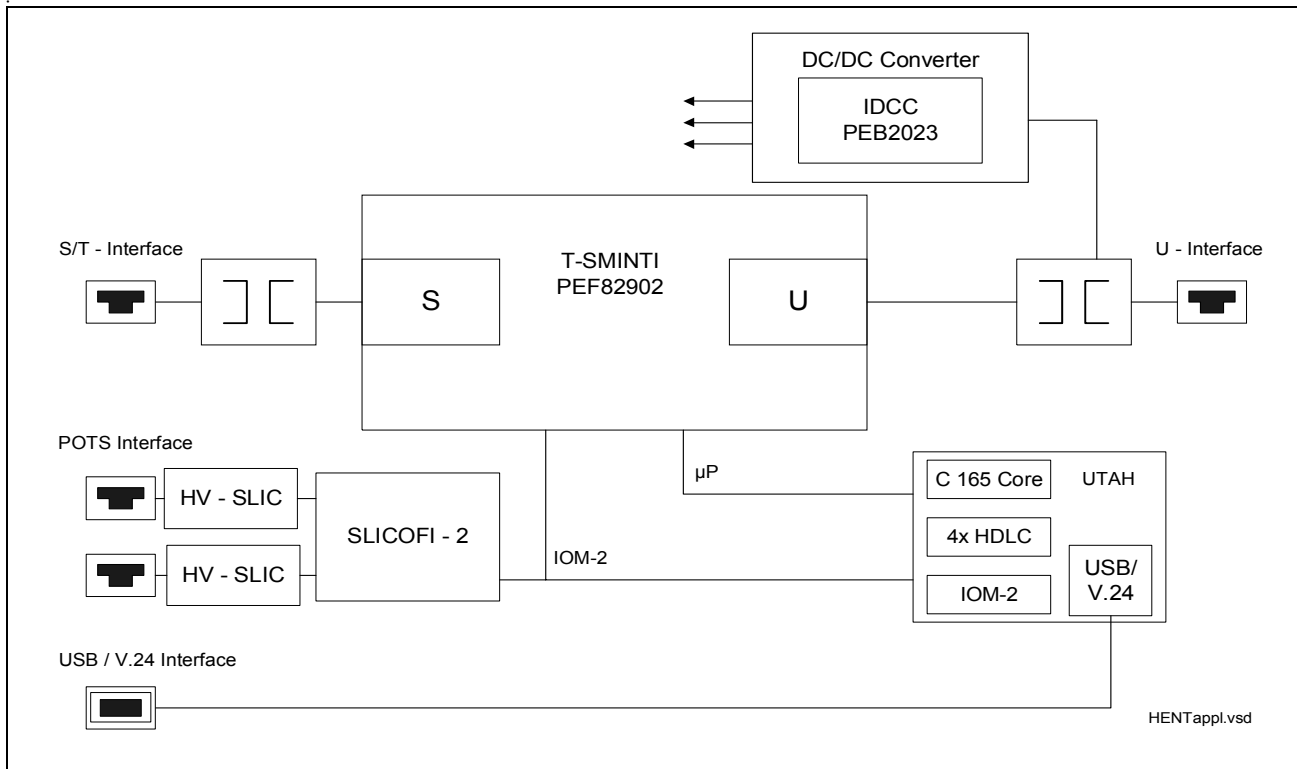
**S-Activated:** 'Activated State' as defined in [Chapter 2.5.5.2](#).

Note: Optionally, pin  $\overline{\text{ACT}}$  can drive a second LED with inverse polarity (connect this additional LED to 3.3V only).

### Test Modes

The test patterns on the S-interface ('2 kHz Single Pulses', '96 kHz Continuous Pulses') and on the U-interface ('Data Through', 'Send Single Pulses',) are invoked via C/I codes (TM1, TM2, DT, SSP). Setting SRES.RES\_U to '1' forces the U-transceiver into test mode 'Quiet Mode' (QM), i.e. the U-transceiver is hardware reset.

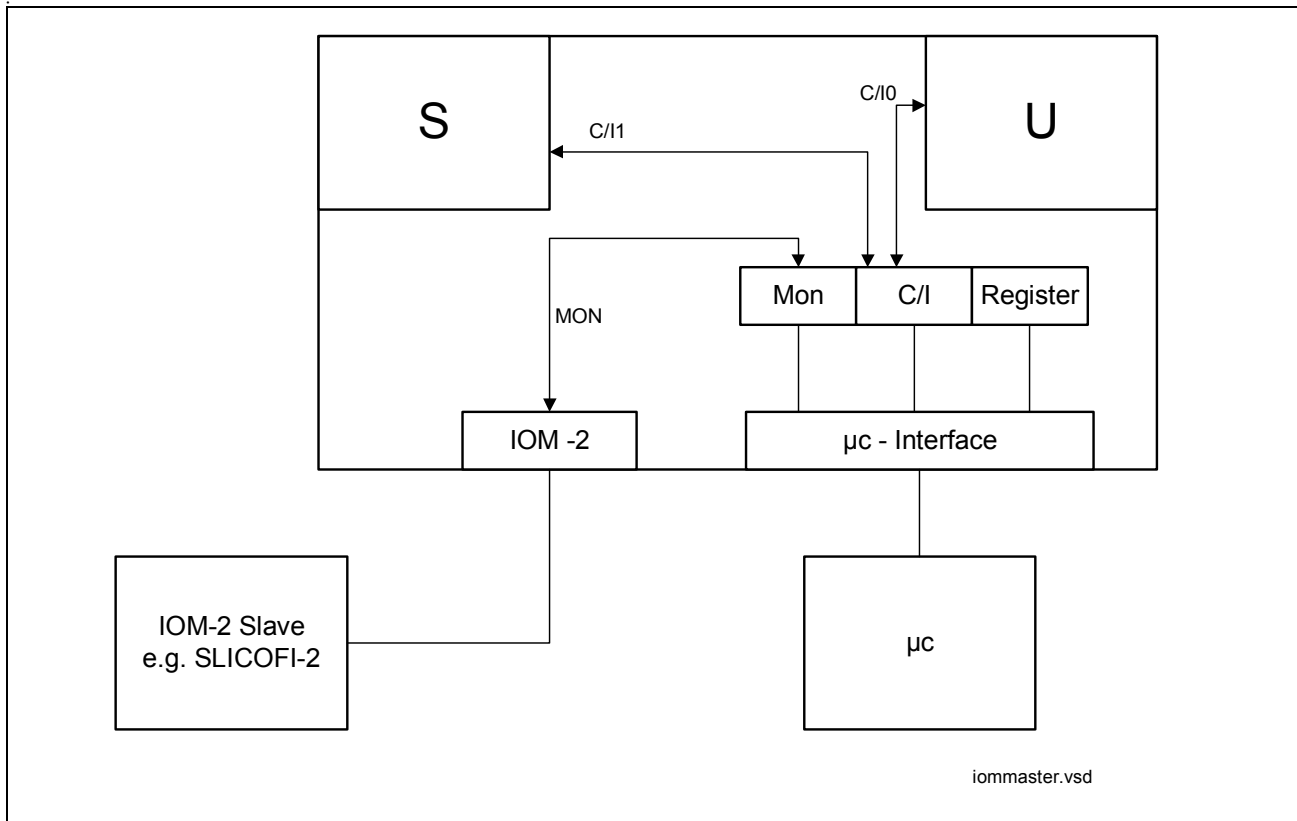
## 1.7 System Integration



**Figure 3 Application Example T-SMINT<sup>®</sup>I: High Feature Intelligent NT**

The U-transceiver, the S-transceiver and the IOM<sup>®</sup>-2 channels can be controlled and monitored via:

- a) the parallel or serial microprocessor interface
  - Access of on-chip registers via  $\mu$ P interface Address/Data format
  - Activation/Deactivation control of U- and S-transceiver via  $\mu$ P interface and C/I handler
  - T-SMINT<sup>®</sup>I is Monitor channel master
  - TIC bus is transparent on IOM<sup>®</sup>-2 interface and is used for D-channel arbitration between S-transceiver and off-chip HDLC controllers.

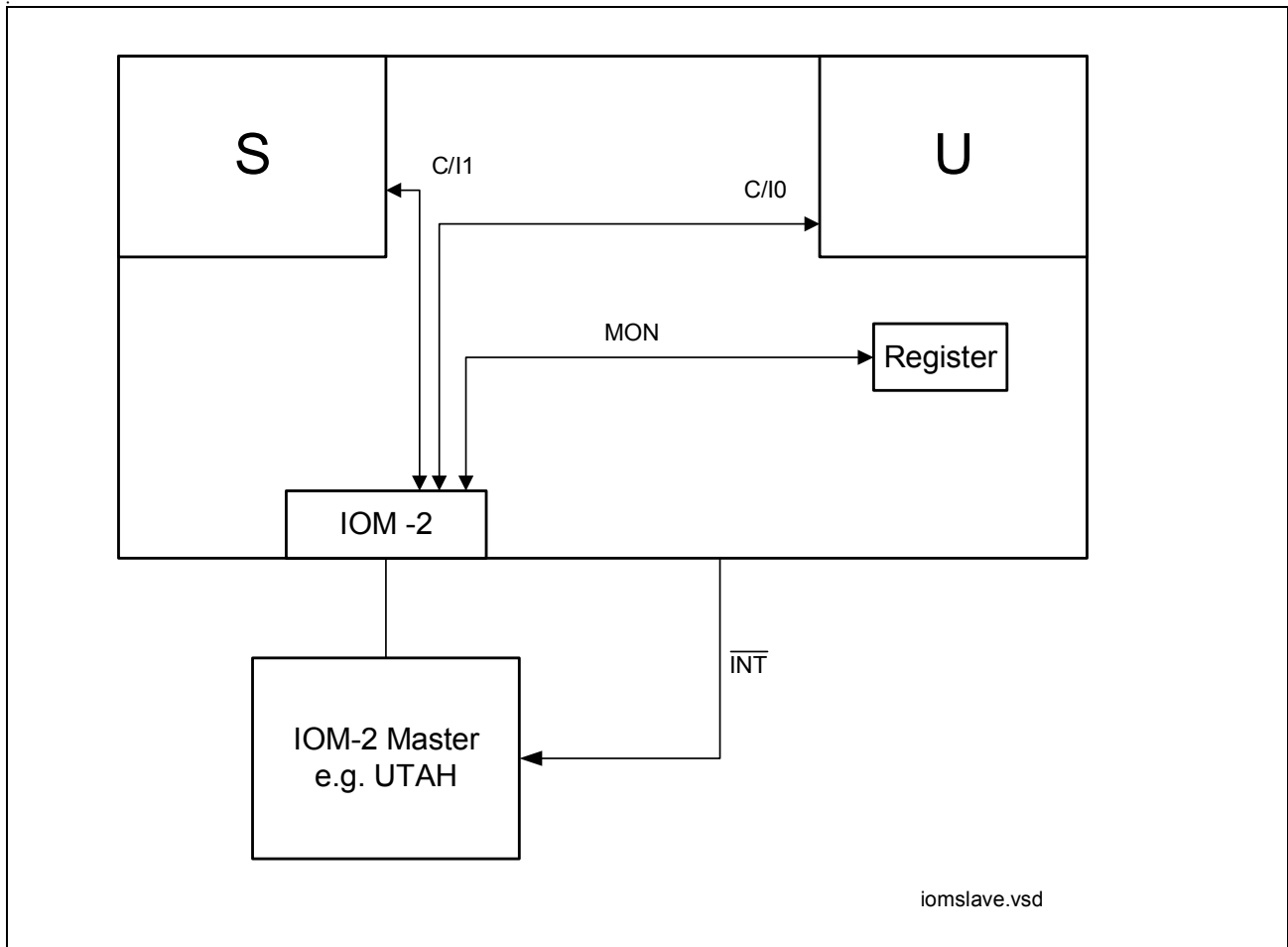


**Figure 4 Control via  $\mu$ P Interface**

Alternatively, the T-SMINT<sup>®</sup>I can be controlled via

b) the IOM<sup>®</sup>-2 Interface

- Access of on-chip registers via the Monitor channel with Header/Address/Data format (Device is Monitor slave)
- Activation/Deactivation control of U- and S-transceiver via the C/I channels CI0 and CI1
- TIC bus is transparent on IOM<sup>®</sup>-2 interface and is used for D-channel arbitration between S-transceiver and off-chip HDLC controllers.



**Figure 5** Control via IOM<sup>®</sup>-2 Interface

## 2 Functional Description

### 2.1 Microcontroller Interfaces

The T-SMINT<sup>®</sup>I supports either a serial or a parallel microcontroller interface. For applications where no controller is connected to the T-SMINT<sup>®</sup>I microcontroller interface, register programming is done via the IOM<sup>®</sup>-2 MONITOR channel from a master device. In such applications the T-SMINT<sup>®</sup>I operates in the IOM<sup>®</sup>-2 slave mode (refer to the corresponding chapter of the IOM<sup>®</sup>-2 MONITOR handler).

The interface selections are all done by pinstrapping. The possible interface selections are listed in [Table 4](#). The selection pins are evaluated when the reset input  $\overline{\text{RST}}$  is released. For the pin levels stated in the tables the following is defined:

'High':dynamic pin value which must be 'High' when the pin level is evaluated

$V_{DD}$ ,  $V_{SS}$ :static 'High' or 'Low' level (tied to  $V_{DD}$ ,  $V_{SS}$ )

**Table 4 Interface Selection for the T-SMINT<sup>®</sup>I**

| PINS     |          | Serial/Parallel Interface | PINS     |          | Interface Type/Mode                              |
|----------|----------|---------------------------|----------|----------|--------------------------------------------------|
| WR (R/W) | RD (DS)  |                           | CS       | ALE      |                                                  |
| 'High'   | 'High'   | Parallel                  | 'High'   | $V_{DD}$ | Motorola                                         |
|          |          |                           |          | $V_{SS}$ | Siemens/Intel Non-Mux                            |
|          |          |                           |          | edge     | Siemens/Intel Mux                                |
| $V_{SS}$ | $V_{SS}$ | Serial                    | 'High'   | $V_{SS}$ | Serial Control Interface(SCI)                    |
|          |          |                           | $V_{SS}$ | $V_{SS}$ | IOM <sup>®</sup> -2 MONITOR Channel (Slave Mode) |

Note: For a selected interface mode which does not require all pins (e.g. address pins) the unused pins must be tied to  $V_{DD}$ .

The microcontroller interface also consists of a microcontroller clock generation at pin MCLK, an interrupt request at pin  $\overline{\text{INT}}$ , a reset input pin  $\overline{\text{RST}}$  and a reset output pin  $\overline{\text{RSTO}}$ .

The interrupt request pin  $\overline{\text{INT}}$  (open drain output) becomes active if the T-SMINT<sup>®</sup>I requests an interrupt.

#### 2.1.1 Serial Control Interface (SCI)

The serial control interface (SCI) is compatible to the SPI interface of Motorola and to the Siemens C510 family of microcontrollers.

The SCI consists of 4 lines: SCLK, SDX, SDR and  $\overline{\text{CS}}$ . Data is transferred via the lines SDR and SDX at the rate given by SCLK. The falling edge of  $\overline{\text{CS}}$  indicates the beginning

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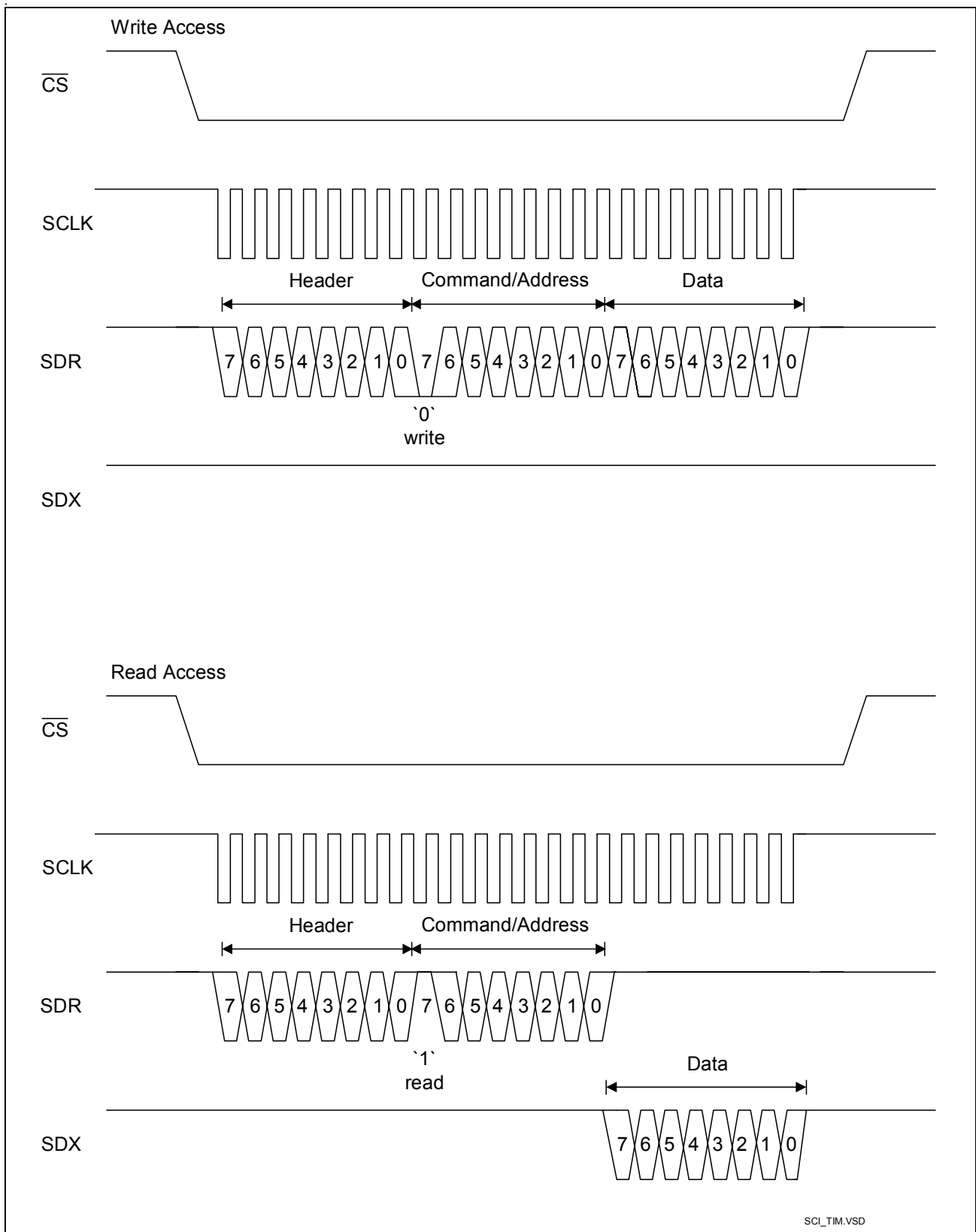
## Functional Description

of a serial access to the registers. The T-SMINT<sup>®</sup> latches incoming data at the rising edge of SCLK and shifts out at the falling edge of SCLK. Each access must be terminated by a rising edge of  $\overline{CS}$ . Data is transferred in groups of 8 bits with the MSB first.

Pad mode of SDX can be selected 'open drain' or 'push-pull' by programming MODE2.PPSDX.

**Figure 6** shows the timing of a one byte read/write access via the serial control interface.

## Functional Description

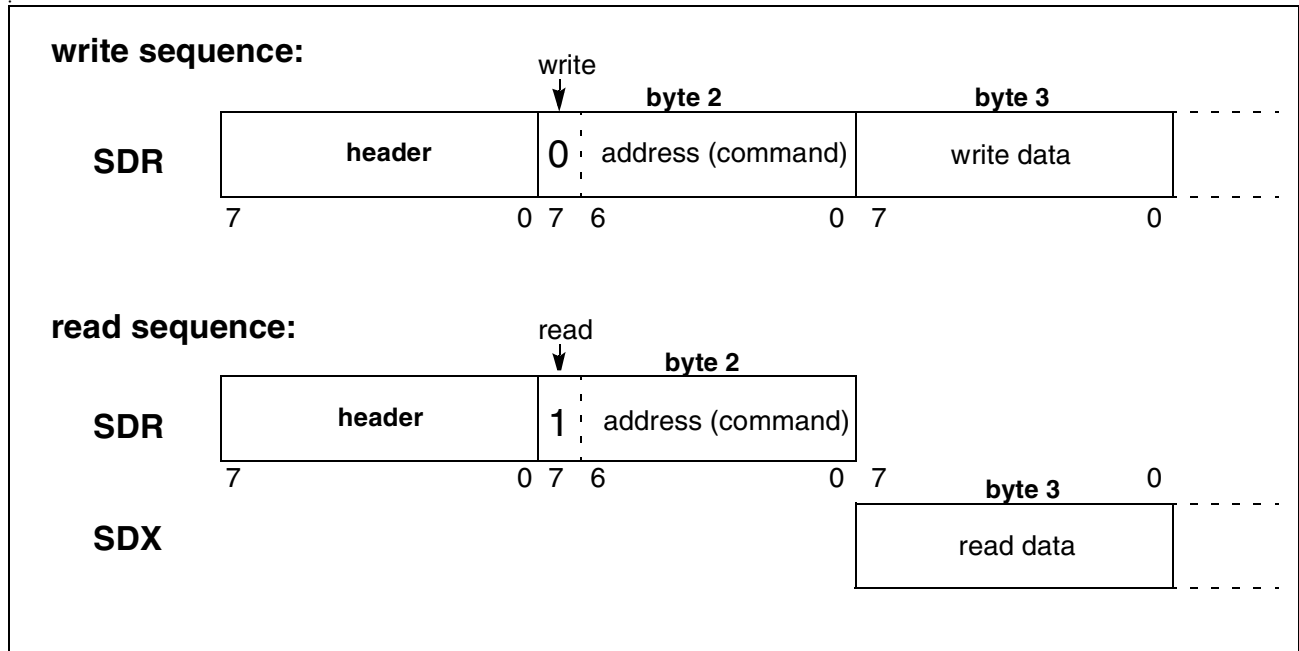


**Figure 6 Serial Control Interface Timing**

## Functional Description

### 2.1.1.1 Programming Sequences

The basic structure of a read/write access to the T-SMINT<sup>®</sup>I registers via the serial control interface is shown in **Figure 7**.



**Figure 7** Serial Command Structure

A new programming sequence starts with the transfer of a header byte. The header byte specifies different programming sequences allowing a flexible and optimized access to the individual functional blocks of the T-SMINT<sup>®</sup>I.

The possible sequences are listed in **Table 5** and are described after that.

**Table 5** Header Byte Code

| Header Byte     | Sequence           | Sequence Type    | Access to                                      |
|-----------------|--------------------|------------------|------------------------------------------------|
| 40 <sub>H</sub> | Adr-Data-Adr-Data  | non-interleaved  | Address Range 00 <sub>H</sub> -7F <sub>H</sub> |
| 48 <sub>H</sub> |                    | interleaved      |                                                |
| 43 <sub>H</sub> | Adr-Data-Data-Data | Read-/Write-only | Address Range 00 <sub>H</sub> -7F <sub>H</sub> |
| 41 <sub>H</sub> |                    | non-interleaved  |                                                |
| 49 <sub>H</sub> |                    | interleaved      |                                                |

#### Header 40<sub>H</sub>: Non-interleaved A-D-A-D Sequences

The non-interleaved A-D-A-D sequences give direct read/write access to the address range 00<sub>H</sub>-7F<sub>H</sub> and can have any length. In this mode SDX and SDR can be connected

## Functional Description

together allowing data transmission on one line.

Example for a read/write access with header 40<sub>H</sub>:

|     |        |       |        |       |        |       |        |       |        |  |
|-----|--------|-------|--------|-------|--------|-------|--------|-------|--------|--|
| SDR | header | wradr | wrdata | rdadr |        | rdadr |        | wradr | wrdata |  |
| SDX |        |       |        |       | rddata |       | rddata |       |        |  |

### Header 48<sub>H</sub>: Interleaved A-D-A-D Sequences

The interleaved A-D-A-D sequences give direct read/write access to the address range 00<sub>H</sub>-7F<sub>H</sub> and can have any length. This mode allows a time optimized access to the registers by interleaving the data on SDX and SDR.

Example for a read/write access with header 48<sub>H</sub>:

|     |        |       |        |       |        |        |        |  |  |  |
|-----|--------|-------|--------|-------|--------|--------|--------|--|--|--|
| SDR | header | wradr | wrdata | rdadr | rdadr  | wradr  | wrdata |  |  |  |
| SDX |        |       |        |       | rddata | rddata |        |  |  |  |

### Header 43<sub>H</sub>: Read-/Write- only A-D-D-D Sequence

Generally, it can be used for any register access to the address range 20<sub>H</sub>-7D<sub>H</sub>. The sequence can have any length and is terminated by the rising edge of  $\overline{CS}$ .

Example for a write access with header 43<sub>H</sub>:

|     |        |       |                   |                   |                   |                   |                   |                   |                   |  |
|-----|--------|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--|
| SDR | header | wradr | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) |  |
| SDX |        |       |                   |                   |                   |                   |                   |                   |                   |  |

Example for a read access with header 43<sub>H</sub>:

|     |        |       |                   |                   |                   |                   |                   |                   |                   |  |
|-----|--------|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--|
| SDR | header | rdadr |                   |                   |                   |                   |                   |                   |                   |  |
| SDX |        |       | rddata<br>(rdadr) | rddata<br>(rdadr) | rddata<br>(rdadr) | rddata<br>(rdadr) | rddata<br>(rdadr) | rddata<br>(rdadr) | rddata<br>(rdadr) |  |

### Header 41<sub>H</sub>: Non-interleaved A-D-D-D Sequence

This sequence (header 41<sub>H</sub>) allows in front of the A-D-D-D write access a non-interleaved A-D-A-D read access. Generally, it can be used for any register access to the address range 20<sub>H</sub>-7D<sub>H</sub>. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of  $\overline{CS}$ .

## Functional Description

Example for a read/write access with header 41<sub>H</sub>:

|     |        |       |        |       |        |       |                   |                   |                   |  |
|-----|--------|-------|--------|-------|--------|-------|-------------------|-------------------|-------------------|--|
| SDR | header | rdadr |        | rdadr |        | wradr | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) |  |
| SDX |        |       | rddata |       | rddata |       |                   |                   |                   |  |

### Header 49<sub>H</sub>: Interleaved A-D-D-D Sequence

This sequence (header 49<sub>H</sub>) allows in front of the A-D-D-D write access an interleaved A-D-A-D read access. Generally, it can be used for any register access to the address range 20<sub>H</sub>-7D<sub>H</sub>. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of  $\overline{CS}$ .

Example for a read/write access with header 49<sub>H</sub>:

|     |        |       |        |        |                   |                   |                   |  |  |  |
|-----|--------|-------|--------|--------|-------------------|-------------------|-------------------|--|--|--|
| SDR | header | rdadr | rdadr  | wradr  | wrdata<br>(wradr) | wrdata<br>(wradr) | wrdata<br>(wradr) |  |  |  |
| SDX |        |       | rddata | rddata |                   |                   |                   |  |  |  |

## 2.1.2 Parallel Microcontroller Interface

The 8-bit parallel microcontroller interface with address decoding on chip allows an easy and fast microcontroller access.

The parallel interface of the T-SMINT<sup>®</sup>I provides three types of  $\mu$ P busses which are selected via pin ALE. The bus operation modes with corresponding control pins are listed in [Table 6](#).

**Table 6 Bus Operation Modes**

|     | Bus Mode                      | Pin ALE         | Control Pins                                              |
|-----|-------------------------------|-----------------|-----------------------------------------------------------|
| (1) | Motorola                      | V <sub>DD</sub> | $\overline{CS}$ , R/ $\overline{W}$ , $\overline{DS}$     |
| (2) | Siemens/Intel non-multiplexed | V <sub>SS</sub> | $\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$       |
| (3) | Siemens/Intel multiplexed     | Edge            | $\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$ , ALE |

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Note: For a selected interface mode which does not require all pins (e.g. address pins) the unused pins must be tied to V<sub>DD</sub>.

A read/write access to the T-SMINT<sup>®</sup>I registers can be done in **multiplexed or non-multiplexed** mode.

In non-multiplexed mode the register address must be applied to the address bus (A0-A6) for the data access via the data bus (D0-D7).

## Functional Description

In multiplexed mode the address on the address bus (AD0-AD7) is latched in by ALE before a read/write access via the address/data bus is performed.

The T-SMINT<sup>®</sup>I provides two different ways to address the register contents which can be selected with the AMOD bit in the MODE2 register. The address mode after reset is the indirect address mode (AMOD = '0'). Reprogramming into the direct address mode (AMOD = '1') has to take place in the indirect address mode. **Figure 8** illustrates both register addressing modes.

**Direct address mode** (AMOD = '1'): The register address to be read or written is directly set in the way described above.

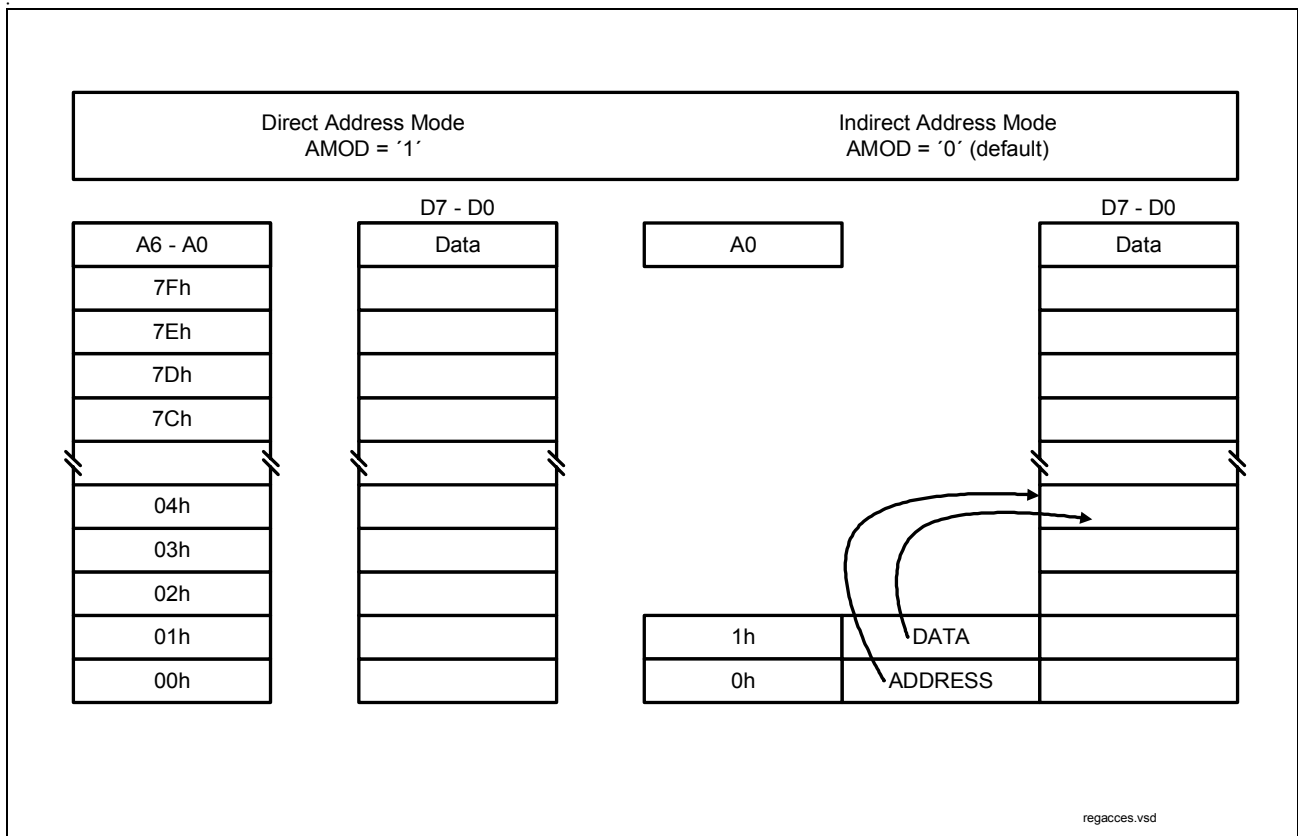
**Indirect address mode** (AMOD = '0'):

- non-muxed: only the LSB of the address bus (A0)
- muxed: only the LSB of the address-data bus (AD0)

gets evaluated to address a virtual ADDRESS (0<sub>H</sub>) and a virtual DATA (1<sub>H</sub>) register.

Every access to a target register consists of:

- a write access (muxed or non-muxed) to ADDRESS to store the target register's address, as well as
- a read access (muxed or non-muxed) from DATA to read from the target register or
- a write access (muxed or non-muxed) to DATA to write to the target register



**Figure 8 Direct/Indirect Register Address Mode**

## Functional Description

### 2.1.3 Microcontroller Clock Generation

The microcontroller clock is derived from the unregulated 15.36 MHz clock from the oscillator and provided by the pin MCLK. Five clock rates are selectable by a programmable prescaler which is controlled by the bits MODE1.MCLK and MODE1.CDS corresponding to the following table.

**Table 7 MCLK Frequencies**

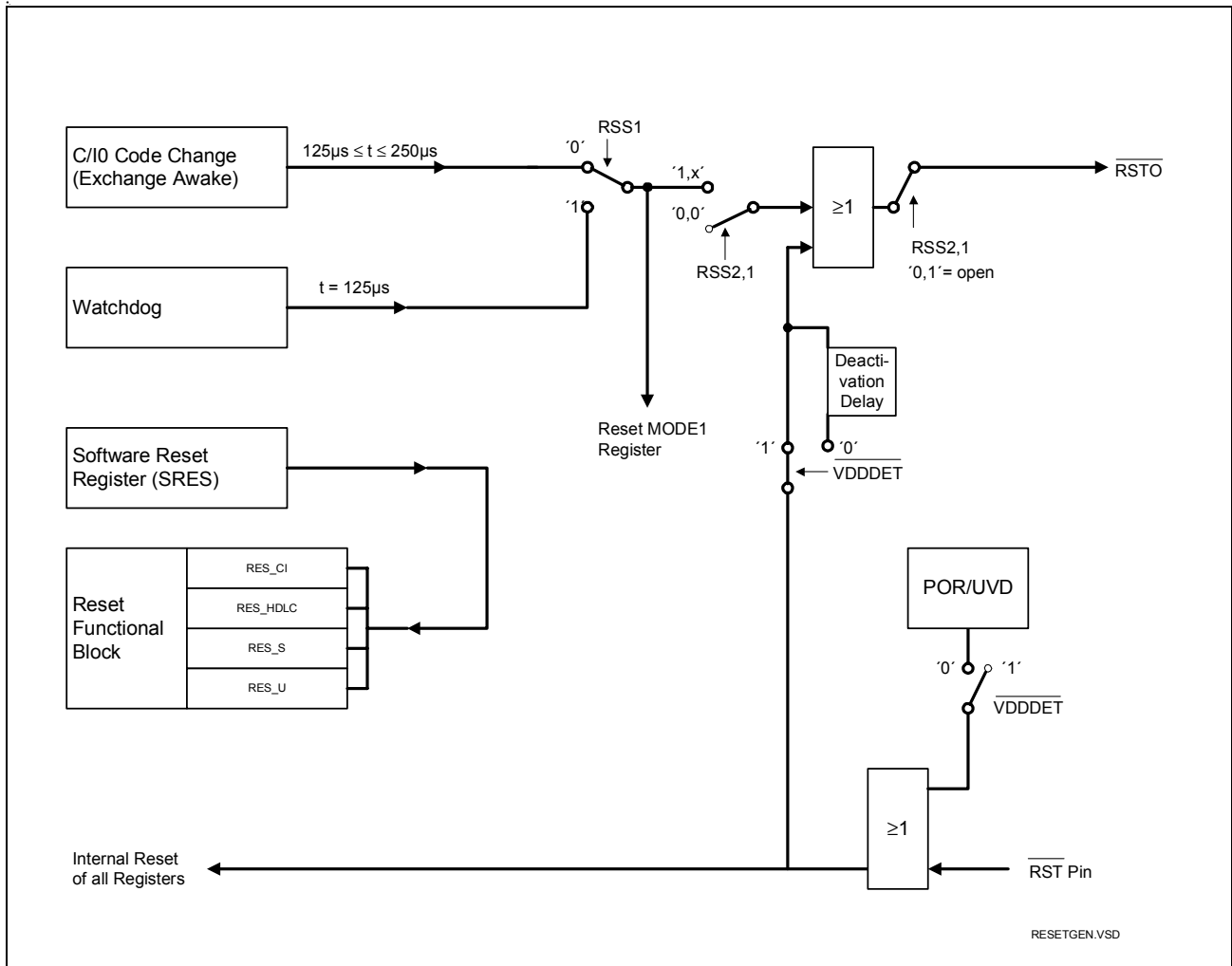
| MODE1.<br>MCLK<br>Bits |   | MCLK frequency<br>with<br>MODE1.CDS = '0' | MCLK frequency<br>with<br>MODE1.CDS = '1' |
|------------------------|---|-------------------------------------------|-------------------------------------------|
| 0                      | 0 | 3.84 MHz                                  | 7.68 MHz                                  |
| 0                      | 1 | 0.96 MHz                                  | 1.92 MHz                                  |
| 1                      | 0 | 7.68 MHz                                  | 15.36 MHz                                 |
| 1                      | 1 | disabled                                  | disabled                                  |

The clock rate is changed after  $\overline{CS}$  becomes inactive.

### 2.2 Reset Generation

**Figure 9** shows the organization of the reset generation of the T-SMINT®I.

## Functional Description



**Figure 9** Reset Generation of the T-SMINT® I¹)

### Reset Source Selection

The internal reset sources C/I code change and Watchdog timer can be output at the low active reset pin  $\overline{RSTO}$ . These reset sources can be selected with the RSS2,1 bits in the MODE1 register according to [Table 8](#).

¹) The 'OR'-gates shall illustrate in a symbolic way, that 'source A active' or 'source B active' is forwarded. The real polarity of the different sources is not considered.

## Functional Description

The internal reset sources set the MODE1 register to its reset value.

**Table 8 Reset Source Selection**

| RSS2<br>Bit 1 | RSS1<br>Bit 0 | C/I Code<br>Change                | Watchdog<br>Timer | POR/UVD <sup>1)</sup> and<br>$\overline{\text{RST}}$ |
|---------------|---------------|-----------------------------------|-------------------|------------------------------------------------------|
| 0             | 0             | --                                | --                | x                                                    |
| 0             | 1             | /RSTO disabled (= high impedance) |                   |                                                      |
| 1             | 0             | x                                 | --                | x                                                    |
| 1             | 1             | --                                | x                 | x                                                    |

<sup>1)</sup> POR/UVD can be enabled/disabled via pin  $\overline{\text{VDDDET}}$

- **C/I Code Change (Exchange Awake)**

A change in the downstream C/I channel (C/I0) generates a reset pulse of  $125 \mu\text{s} \leq t \leq 250 \mu\text{s}$ .

- **Watchdog Timer**

After the selection of the watchdog timer (RSS = '11') an internal timer is reset and started. During every time period of 128 ms the microcontroller has to program the WTC1- and WTC2 bits in the following sequence to reset and restart the watchdog timer:

|    | WTC1 | WTC2 |
|----|------|------|
| 1. | 1    | 0    |
| 2. | 0    | 1    |

Otherwise the timer expires and a WOV-interrupt (ISTA Register) together with a reset out pulse on pin  $\overline{\text{RSTO}}$  of  $125 \mu\text{s}$  is generated.

Deactivation of the watchdog timer is only possible with a hardware reset (including expiration of the watchdog timer).

As in the SCOUT-S, the watchdog timer is clocked with the IOM<sup>®</sup>-2 clocks and works only if the internal IOM<sup>®</sup>-2 clocks are active. Hence, the power consumption is minimized in state power down.

### Software Reset Register (SRES)

Several main functional blocks of the T-SMINT<sup>®</sup>I can be reset separately by software setting the corresponding bit in the SRES register. This is equivalent to a hardware reset of the corresponding functional block. The reset state is activated as long as the bit is set to '1'.

## Functional Description

### External Reset Input

At the  $\overline{\text{RST}}$  input an external reset can be applied forcing the T-SMINT<sup>®</sup>I in the reset state. This external reset signal is additionally fed to the  $\overline{\text{RSTO}}$  output.

After release of an external reset, the  $\mu\text{C}$  has to wait for min.  $t_{\mu\text{C}}$  before it starts read or write access to the T-SMINT<sup>®</sup>I (see [Table 37](#)).

### Reset Output

If  $\overline{\text{VDDDET}}$  is active, then the deactivation of a reset output on  $\overline{\text{RSTO}}$  is delayed by  $t_{\text{DEACT}}$  (see [Table 38](#)).

### Reset Generation

The T-SMINT<sup>®</sup>I has an on-chip reset generator based on a Power-On Reset (POR) and Under Voltage Detection (UVD) circuit (see [Table 38](#)). The POR/UVD requires no external components.

The POR/UVD circuit can be disabled via pin  $\overline{\text{VDDDET}}$ .

The requirements on  $V_{\text{DD}}$  ramp-up during power-on reset are described in [Chapter 5.6.5](#).

### Clocks and Data Lines During Reset

During reset the data clock (DCL), the bit clock (BCL), the microcontroller clock<sup>1)</sup> (MCLK) and the frame synchronization (FSC) keep running.

During reset DD and DU are high; with the exception of:

- The output C/I code from the U-Transceiver on DD IOM<sup>®</sup>-2 channel 0 is 'DR' = 0000 (Value after reset of register UCIR = '00<sub>H</sub>')  
(Value after reset of register UCIR = '00<sub>H</sub>')
- The output C/I code from the S-Transceiver on DU IOM<sup>®</sup>-2 channel 1 is 'TIM' = 0000.

<sup>1)</sup> during a Power-On/UVD Reset, the microcontroller clock MCLK is not running, but starts running as soon as timer  $t_{\text{DEAC}}$  is started.

## Functional Description

### 2.3 IOM<sup>®</sup>-2 Interface

The T-SMINT<sup>®</sup>I supports the IOM<sup>®</sup>-2 interface in terminal mode (DCL=1.536 MHz) according to the IOM<sup>®</sup>-2 Reference Guide [12].

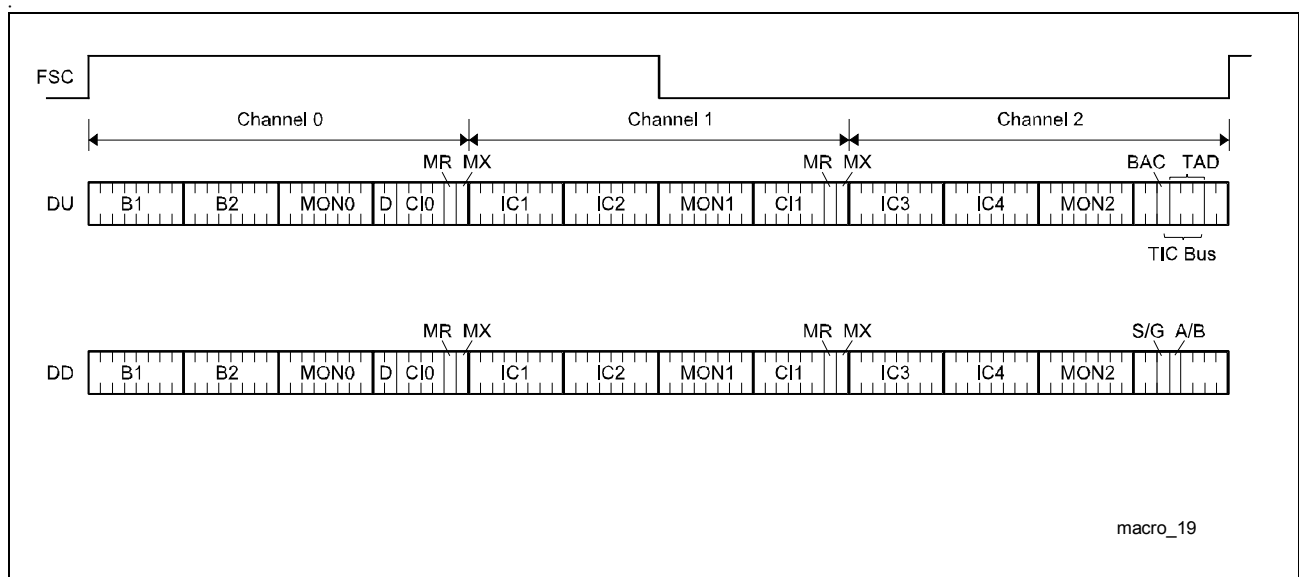
#### 2.3.1 IOM<sup>®</sup>-2 Functional Description

The IOM<sup>®</sup>-2 interface consists of four lines: FSC, DCL, DD, DU and optionally BCL. The rising edge of FSC indicates the start of an IOM<sup>®</sup>-2 frame. The DCL and the BCL clock signals synchronize the data transfer on both data lines DU and DD. The DCL is twice the bit rate, the BCL rate is equal to the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle and sampled at the falling edge of the second clock cycle. With BCL the bits are shifted out with the rising edge and sampled with the falling edge of the single clock cycle.

The IOM<sup>®</sup>-2 interface can be enabled/disabled with the DIS\_IOM bit in the IOM\_CR register. The FSC signal is an 8 kHz frame sync signal. The number of PCM timeslots on the receive and transmit lines is determined by the frequency of the DCL clock (or BCL), with the 1.536 MHz (BCL=768 kHz) clock 3 channels consisting of 4 timeslots each are available.

#### IOM<sup>®</sup>-2 Frame Structure of the T-SMINT<sup>®</sup>I

The frame structure on the IOM<sup>®</sup>-2 data ports (DU,DD) of the T-SMINT<sup>®</sup>I with a DCL clock of 1.536 MHz (or BCL=768 kHz) and if TIC bus is not disabled (IOM\_CR.TIC\_DIS) is shown in [Figure 10](#).



**Figure 10 IOM<sup>®</sup>-2 Frame Structure of the T-SMINT<sup>®</sup>I**

## Functional Description

The frame is composed of three channels:

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (MON0) and a command/indication channel (CI0) for control and programming of e.g. the U-transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels (IC), a MONITOR programming channel (MON1) and a command/indication channel (CI1) for control and programming of e.g. the S-transceiver.
- Channel 2 is used for D-channel access mechanism (TIC-bus, S/G bit). Additionally, channel 2 supports further IC and MON channels.

### 2.3.2 IOM<sup>®</sup>-2 Handler

The IOM<sup>®</sup>-2 handler offers a great flexibility for handling the data transfer between the different functional units of the T-SMINT<sup>®</sup>I and voice/data devices connected to the IOM<sup>®</sup>-2 interface. Additionally it provides a microcontroller access to all time slots of the IOM<sup>®</sup>-2 interface via the four controller data access registers (CDA).

The PCM data of the functional units

- S-transceiver (S) and the
- Controller data access (CDA)

can be configured by programming the time slot and data port selection registers (TSDP). With the TSS bits (Time Slot Selection) the PCM data of the functional units can be assigned to each of the 12 PCM time slots of the IOM<sup>®</sup>-2 frame. With the DPS bit (Data Port Selection) the output of each functional unit is assigned to DU or DD respectively. The input is assigned vice versa. With the control registers (CR) the access to the data of the functional units can be controlled by setting the corresponding control bits (EN, SWAP).

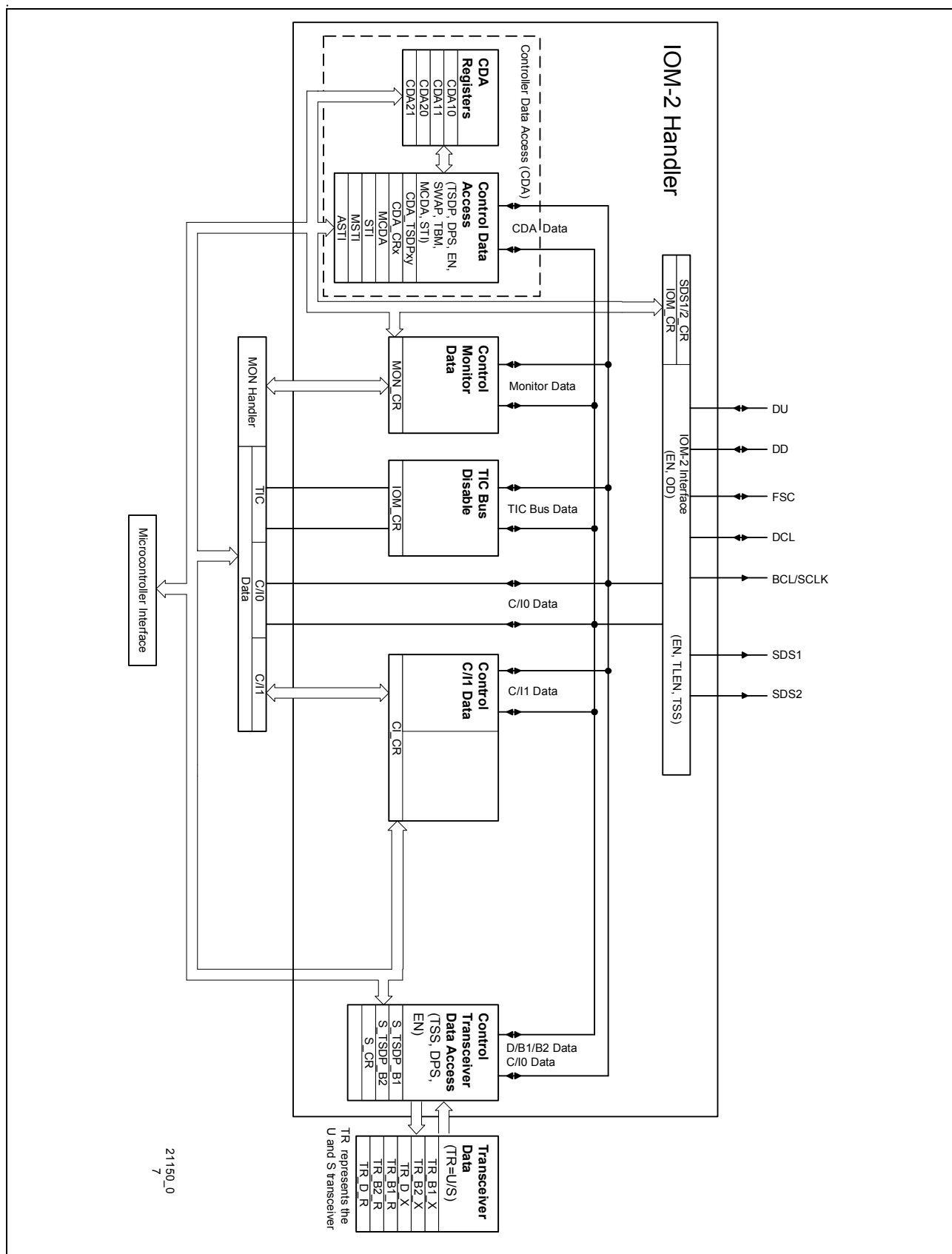
The IOM<sup>®</sup>-2 handler also provides access to the

- U and S transceiver
- MONITOR channel
- C/I channels (CI0, CI1)
- TIC bus (TIC)

The access to these channels is controlled by the registers S\_CR, CI\_CR and MON\_CR. The IOM<sup>®</sup>-2 interface with the two Serial Data Strokes (SDS1,2) is controlled by the control registers IOM\_CR, SDS1\_CR and SDS2\_CR.

The following **Figure 11** shows the architecture of the IOM<sup>®</sup>-2 handler.

## Functional Description



**Figure 11 Architecture of the IOM<sup>®</sup>-2 Handler**

## Functional Description

### 2.3.2.1 Controller Data Access (CDA)

The four controller data access registers (CDA10, CDA11, CDA20, CDA21) provide microcontroller access to the 12 IOM<sup>®</sup>-2 time slots and more:

- looping of up to four independent PCM channels from DU to DD or vice versa over the four CDA registers
- shifting or switching of two independent PCM channels to another two independent PCM channels on both data ports (DU, DD). Between reading and writing the data can be manipulated (processed with an algorithm) by the microcontroller. If this is not the case a switching function is performed.
- monitoring of up to four time slots on the IOM<sup>®</sup>-2 interface simultaneously
- microcontroller read and write access to each PCM channel

The access principle, which is identical for the two channel register pairs CDA10/11 and CDA20/21, is illustrated in [Figure 12](#). The index variables x,y used in the following description can be 1 or 2 for x, and 0 or 1 for y. The prefix 'CDA\_' from the register names has been omitted for simplification.

To each of the four CDAXy data registers a TSDPxxy register is assigned by which the time slot and the data port can be determined. With the TSS (Time Slot Selection) bits a time slot from 0...11 can be selected. With the DPS (Data Port Selection) bit the output of the CDAXy register can be assigned to DU or DD respectively. The time slot and data port for the output of CDAXy is always defined by its own TSDPxxy register. The input of CDAXy depends on the SWAP bit in the control registers CRx.

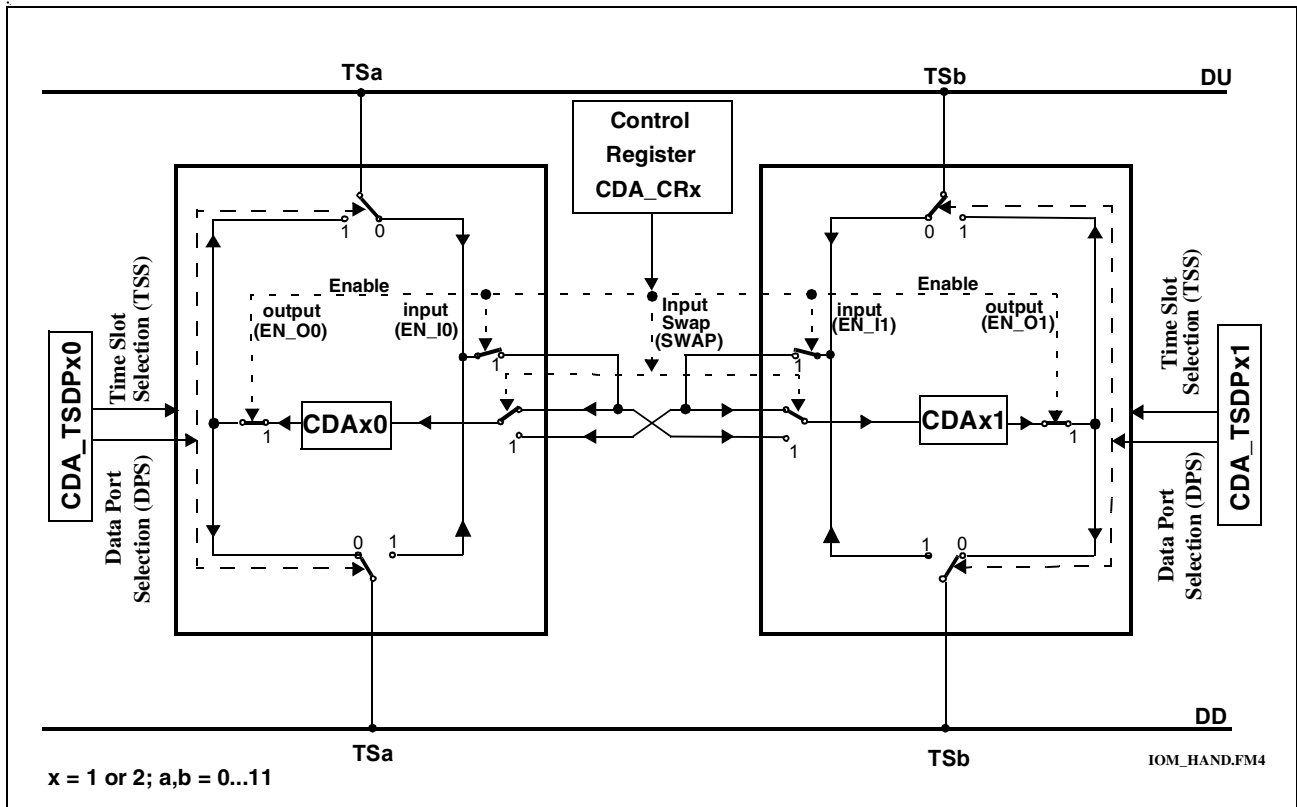
If the SWAP bit = '0' (swap is disabled) the time slot and data port for the input and output of the CDAXy register is defined by its own TSDPxxy register.

If the SWAP bit = '1' (swap is enabled) the input port and time slot of the CDAX0 is defined by the TSDP register of CDAX1 and the input port and time slot of CDAX1 is defined by the TSDP register of CDAX0. The input definition for time slot and data port CDAX0 are thus swapped to CDAX1 and for CDAX1 swapped to CDAX0. The output timeslots are not affected by SWAP.

The input and output of every CDAXy register can be enabled or disabled by setting the corresponding EN (-able) bit in the control register CDAX\_CR. If the input of a register is disabled the output value in the register is retained.

Usually one input and one output of a functional unit (transceiver, CDA register) is programmed to a timeslot on IOM<sup>®</sup>-2 (e.g. for B-channel transmission in upstream direction the S-transceiver writes data onto IOM<sup>®</sup>-2 and the U-transceiver reads data from IOM<sup>®</sup>-2). For monitoring data in such cases a CDA register is programmed as described below under "Monitoring Data". Besides that none of the IOM<sup>®</sup>-2 timeslots must be assigned more than one input and output of any functional unit.

## Functional Description



**Figure 12 Data Access via CDAX0 and CDAX1 register pairs**

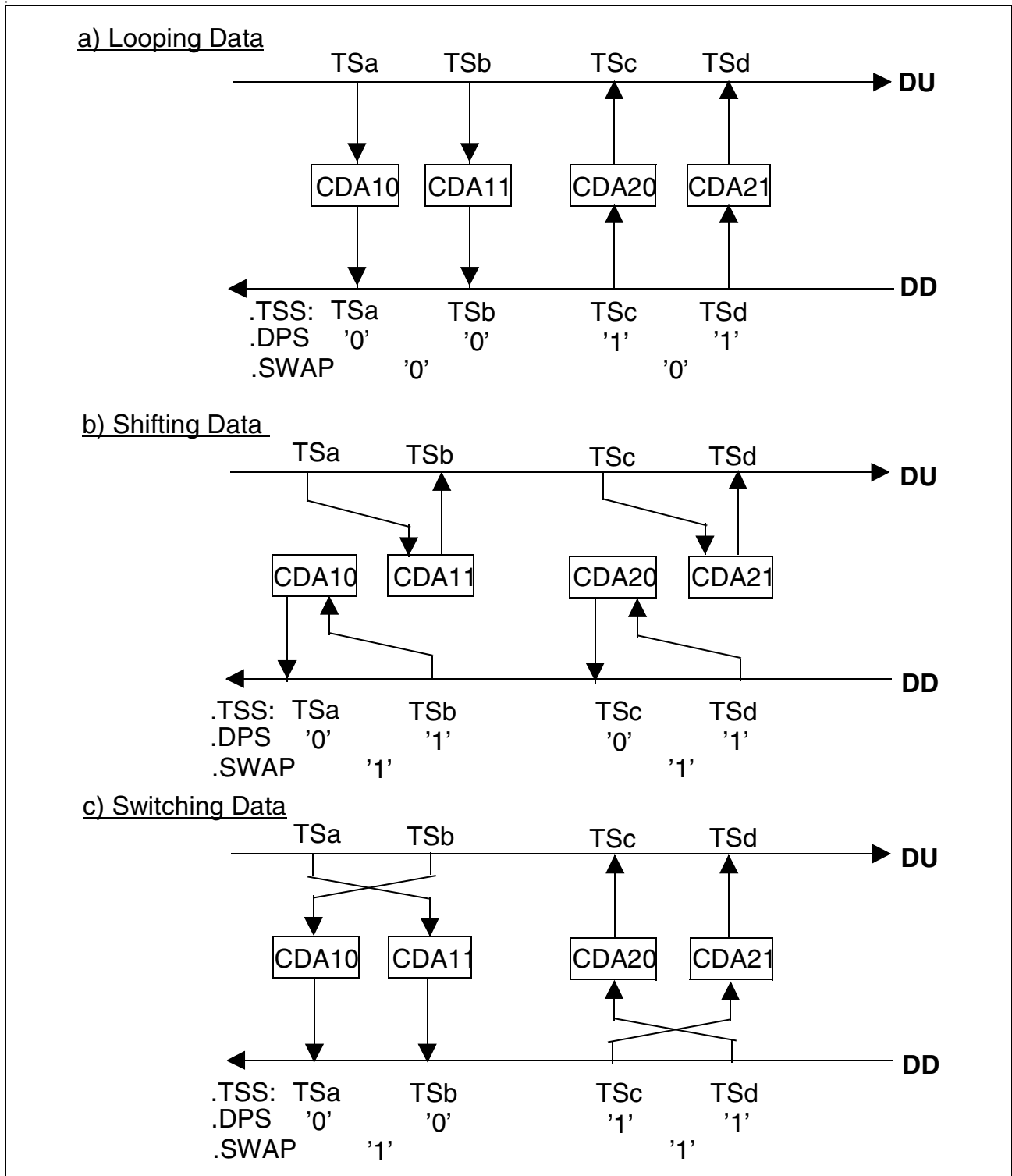
### Looping and Shifting Data

**Figure 13** gives examples for typical configurations with the above explained control and configuration possibilities with the bits TSS, DPS, EN and SWAP in the registers TSDPx<sub>y</sub> or CDAX<sub>CR</sub>:

- looping IOM<sup>®</sup>-2 time slot data from DU to DD or vice versa (SWAP = '0')
- shifting data from TSa to TSb and TSc to TSd in both transmission directions (SWAP = '1')
- switching data from TSa to TSb and looping from DU to DD or switching TSc to TSd and looping from DD to DU .

TSa is programmed in TSDP10, TSb in TSDP11, TSc in TSDP20 and TSd in TSDP21.

## Functional Description



**Figure 13 Examples for Data Access via CDAxy Registers**

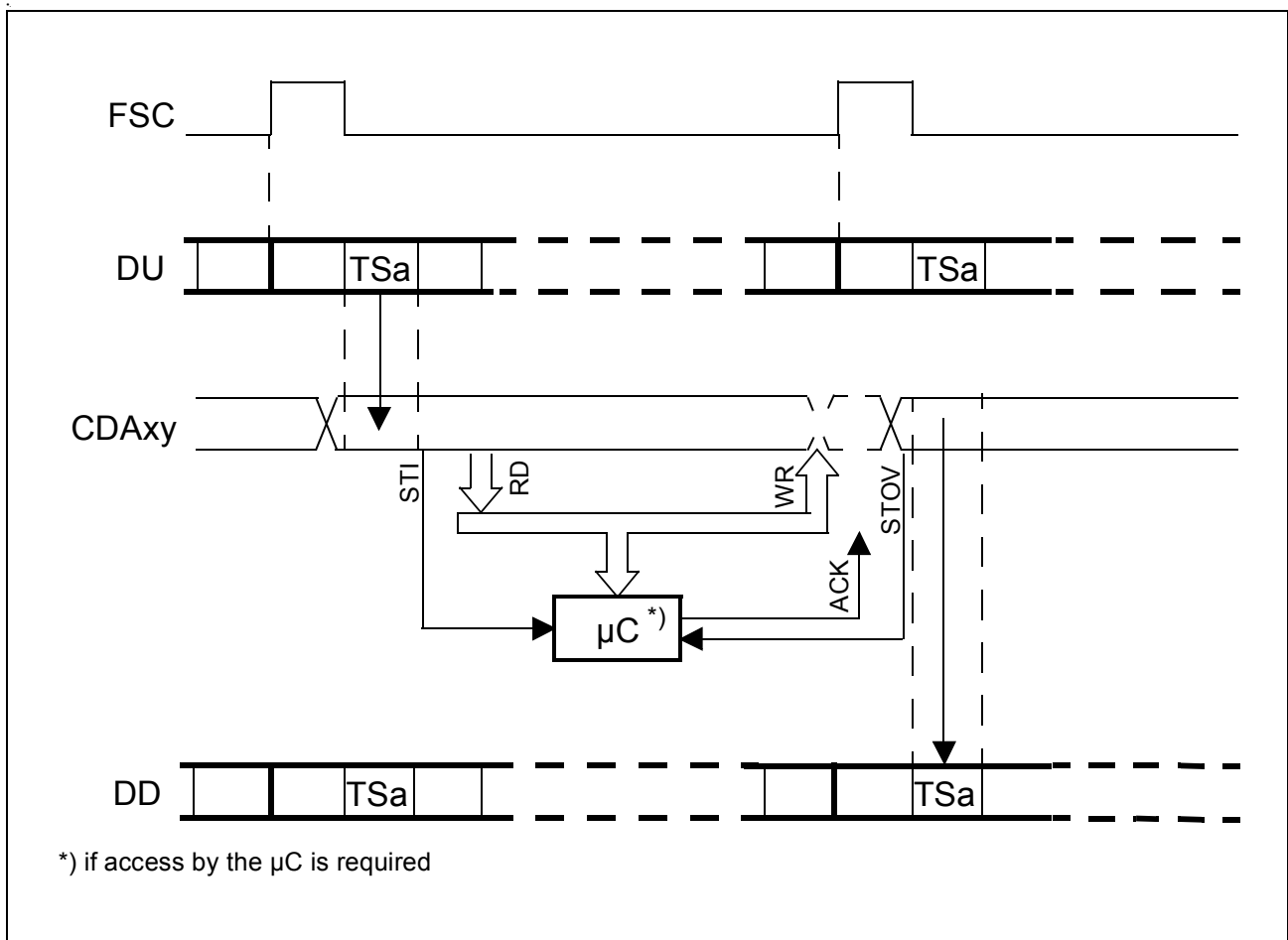
- a) Looping Data
- b) Shifting (Switching) Data
- c) Switching and Looping Data

## Functional Description

**Figure 14** shows the timing of looping TSa from DU to DD via CDAXy register. TSa is read in the CDAXy register from DU and is written one frame later on DD.

**Figure 15** shows the timing of shifting data from TSa to TSb on DU(DD). In **Figure 15a)** shifting is done in one frame because TSa and TSb didn't succeed directly one another ( $a = 0...9$  and  $b \geq a+2$ ). In **Figure 15b)** shifting is done from one frame to the following frame. This is the case when the time slots succeed one other ( $b = a+1$ ) or  $b$  is smaller than  $a$  ( $b < a$ ).

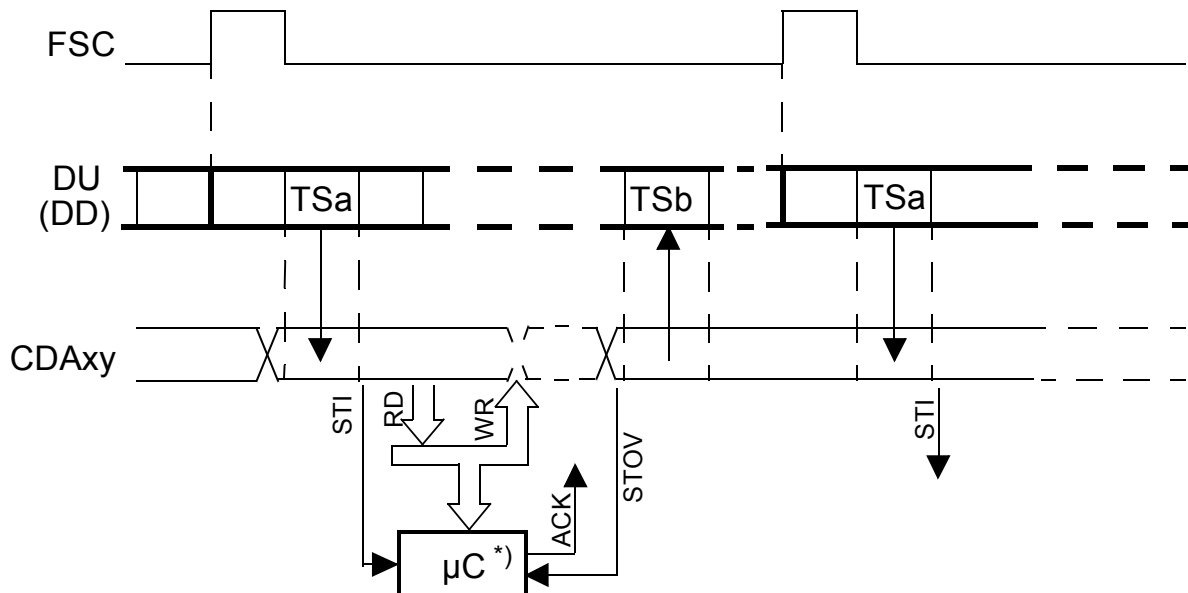
At looping and shifting the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the status overflow interrupt (STOV). STI and STOV are explained in the section 'Synchronous Transfer'. If there is no controller intervention the looping and shifting is done autonomously.



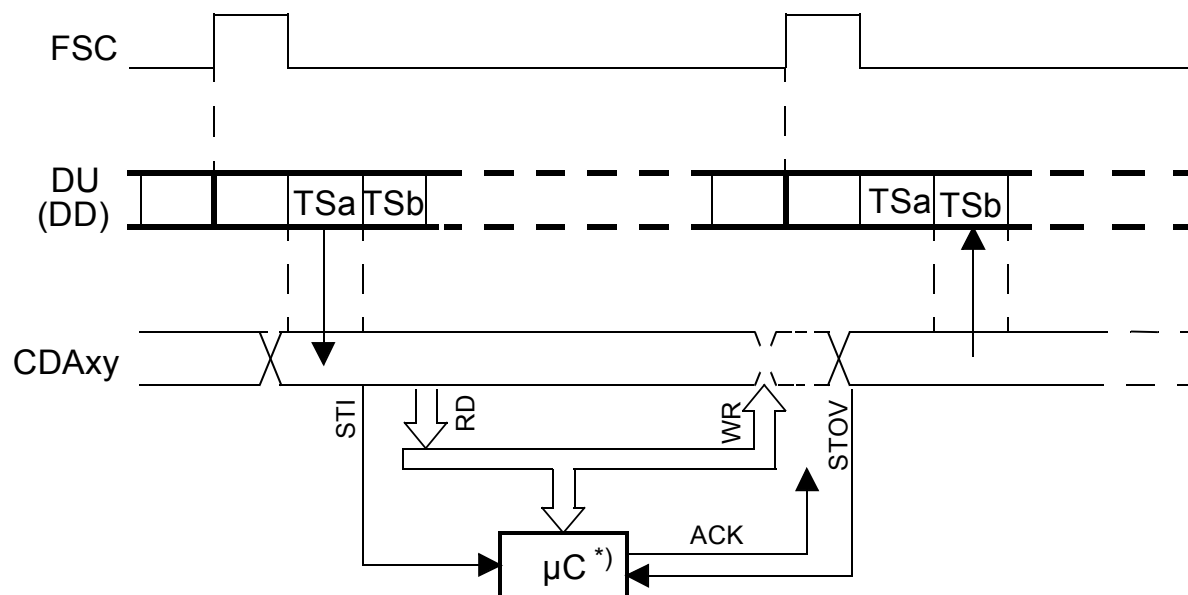
**Figure 14 Data Access when Looping TSa from DU to DD**

## Functional Description

- a) Shifting TSa → TSb within one frame**  
(a,b: 0...11 and  $b \geq a+2$ )



- b) Shifting TSa → TSb in the next frame**  
(a,b: 0...11 and ( $b = a+1$  or  $b < a$ ))



\*) if access by the  $\mu C$  is required

**Figure 15 Data Access when Shifting TSa to TSb on DU (DD)**

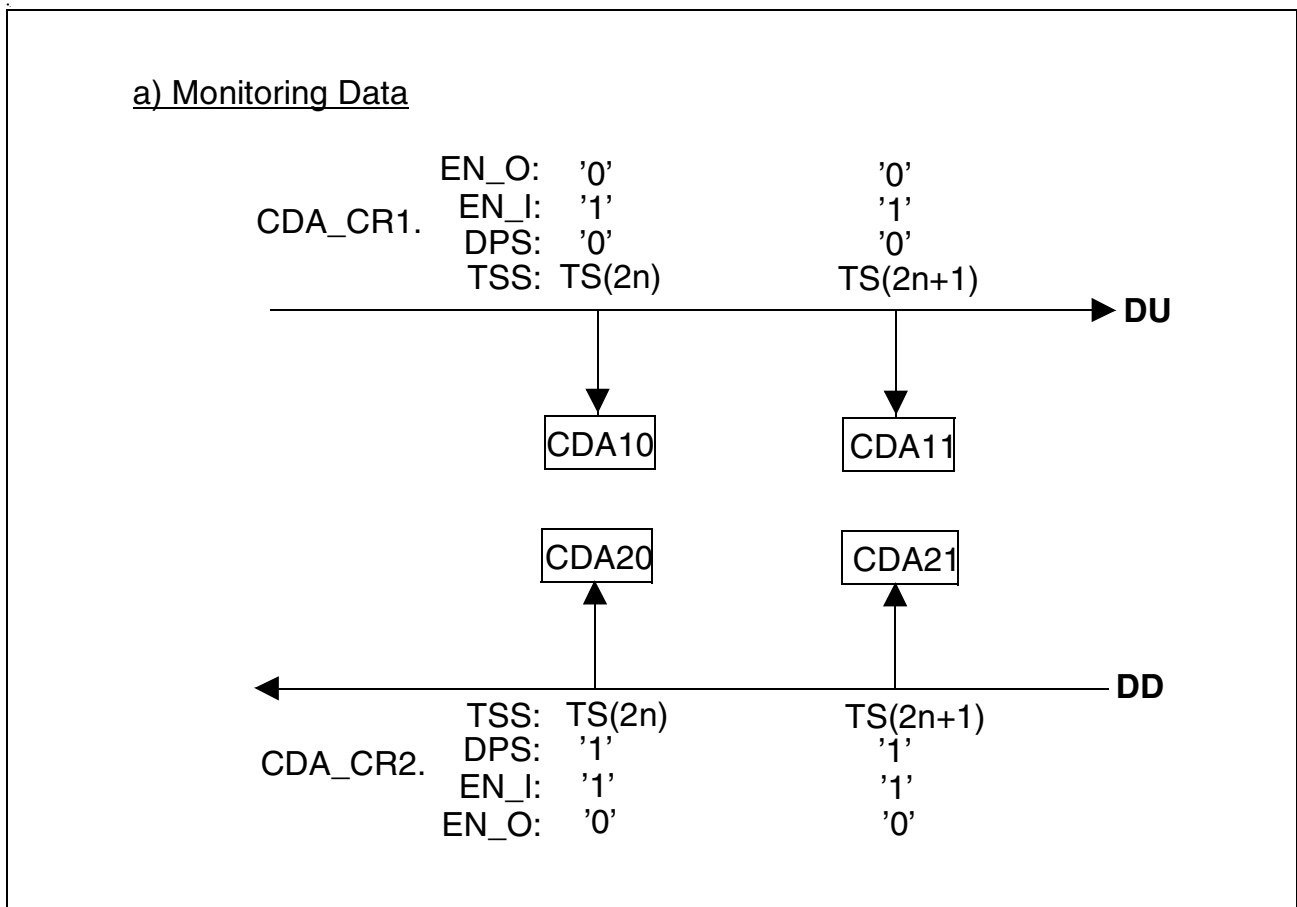
## Functional Description

### Monitoring Data

**Figure 16** gives an example for monitoring of two IOM<sup>®</sup>-2 time slots each on DU or DD simultaneously. For monitoring on DU and/or DD the channel registers with even numbers (CDA10, CDA20) are assigned to time slots with even numbers TS(2n) and the channel registers with odd numbers (CDA11, CDA21) are assigned to time slots with odd numbers TS(2n+1). The user has to take care of this restriction by programming the appropriate time slots.

This mode is only valid if two blocks (e.g. both transceivers) are programmed to these timeslots and communicating via IOM<sup>®</sup>-2.

However, if only one block is programmed to this timeslot the timeslots for CDAx0 and CDAx1 can be programmed completely independently.



**Figure 16 Example for Monitoring Data**

### Monitoring TIC Bus

Monitoring the TIC bus (TS11) is handled as a special case. The TIC bus can be monitored with the registers CDAx0 by setting the EN\_TBM (Enable TIC Bus Monitoring) bit in the control registers CRx. The TSDPx0 must be set to 08<sub>h</sub> for monitoring from DU

## Functional Description

or  $88_h$  for monitoring from DD. By this it is possible to monitor the TIC bus (TS11) and the odd numbered D-channel (TS3) simultaneously on DU and DD.

### Synchronous Transfer

While looping, shifting and switching the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the synchronous transfer overflow interrupt (STOV).

The microcontroller access to each of the CDA<sub>xy</sub> registers can be synchronized by means of four programmable synchronous transfer interrupts (STI<sub>xy</sub>)<sup>1)</sup> and synchronous transfer overflow interrupts (STOV<sub>xy</sub>)<sup>2)</sup> in the STI register.

Depending on the DPS bit in the corresponding TSDP<sub>xy</sub> register the STI<sub>xy</sub> is generated two (for DPS='0') or one (for DPS='1') BCL clock after the selected time slot (CDA\_TSDP<sub>xy</sub>.TSS). One BCL clock is equivalent to two DCL clocks.

In the following description the index  $xy_0$  and  $xy_1$  are used to refer to two different interrupt pairs (STI/STOV) out of the four CDA interrupt pairs (STI10/STOV10, STI11/STOV11, STI20/STOV20, STI21/STOV21).

A STOV<sub>xy<sub>0</sub></sub> is related to its STI<sub>xy<sub>0</sub></sub> and is only generated if STI<sub>xy<sub>0</sub></sub> is enabled and not acknowledged. However, if STI<sub>xy<sub>0</sub></sub> is masked, the STOV<sub>xy<sub>0</sub></sub> is generated for any other STI<sub>xy<sub>1</sub></sub> which is enabled and not acknowledged.

**Table 9** gives some examples for that. It is assumed that a STOV interrupt is only generated because a STI interrupt was not acknowledged before.

In example 1 only the STI<sub>xy<sub>0</sub></sub> is enabled and thus STI<sub>xy<sub>0</sub></sub> is only generated. If no STI is enabled, no interrupt will be generated even if STOV is enabled (example 2).

In example 3 STI<sub>xy<sub>0</sub></sub> is enabled and generated and the corresponding STOV<sub>xy<sub>0</sub></sub> is disabled. STI<sub>xy<sub>1</sub></sub> is disabled but its STOV<sub>xy<sub>1</sub></sub> is enabled, and therefore STOV<sub>xy<sub>1</sub></sub> is generated due to STI<sub>xy<sub>0</sub></sub>. In example 4 additionally the corresponding STOV<sub>xy<sub>0</sub></sub> is enabled, so STOV<sub>xy<sub>0</sub></sub> and STOV<sub>xy<sub>1</sub></sub> are both generated due to STI<sub>xy<sub>0</sub></sub>.

In example 5 additionally the STI<sub>xy<sub>1</sub></sub> is enabled with the result that STOV<sub>xy<sub>0</sub></sub> is only generated due to STI<sub>xy<sub>0</sub></sub> and STOV<sub>xy<sub>1</sub></sub> is only generated due to STI<sub>xy<sub>1</sub></sub>.

Compared to the previous example STOV<sub>xy<sub>0</sub></sub> is disabled in example 6, so STOV<sub>xy<sub>0</sub></sub> is not generated and STOV<sub>xy<sub>1</sub></sub> is only generated for STI<sub>xy<sub>1</sub></sub> but not for STI<sub>xy<sub>0</sub></sub>.

<sup>1)</sup> In order to enable the STI interrupts the input of the corresponding CDA register has to be enabled. This is also valid if only a synchronous write access is wanted. The enabling of the output alone does not effect an STI interrupt.

<sup>2)</sup> In order to enable the STOV interrupts the output of the corresponding CDA register has to be enabled. This is also valid if only a synchronous read access is wanted. The enabling of the input alone does not effect an interrupt.

## Functional Description

**Table 9 Examples for Synchronous Transfer Interrupts**

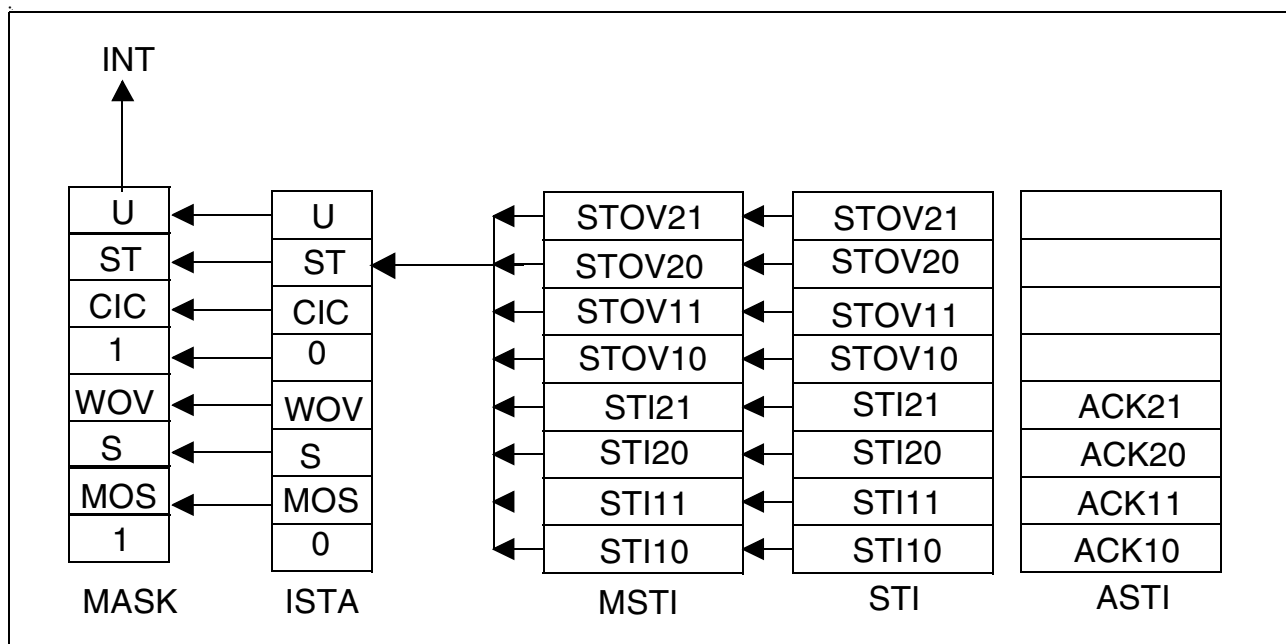
| Enabled Interrupts<br>(Register MSTI) |                                                     | Generated Interrupts<br>(Register STI) |                                                                        |           |
|---------------------------------------|-----------------------------------------------------|----------------------------------------|------------------------------------------------------------------------|-----------|
| STI                                   | STOV                                                | STI                                    | STOV                                                                   |           |
| xy <sub>0</sub>                       | -                                                   | xy <sub>0</sub>                        | -                                                                      | Example 1 |
| -                                     | xy <sub>0</sub>                                     | -                                      | -                                                                      | Example 2 |
| xy <sub>0</sub>                       | xy <sub>1</sub>                                     | xy <sub>0</sub>                        | xy <sub>1</sub>                                                        | Example 3 |
| xy <sub>0</sub>                       | xy <sub>0</sub> ; xy <sub>1</sub>                   | xy <sub>0</sub>                        | xy <sub>0</sub> ; xy <sub>1</sub>                                      | Example 4 |
| xy <sub>0</sub> ; xy <sub>1</sub>     | xy <sub>0</sub> ; xy <sub>1</sub>                   | xy <sub>0</sub><br>xy <sub>1</sub>     | xy <sub>0</sub><br>xy <sub>1</sub>                                     | Example 5 |
| xy <sub>0</sub> ; xy <sub>1</sub>     | xy <sub>1</sub>                                     | xy <sub>0</sub><br>xy <sub>1</sub>     | -<br>xy <sub>1</sub>                                                   | Example 6 |
| xy <sub>0</sub> ; xy <sub>1</sub>     | xy <sub>0</sub> ; xy <sub>1</sub> ; xy <sub>2</sub> | xy <sub>0</sub><br>xy <sub>1</sub>     | xy <sub>0</sub> ; xy <sub>2</sub><br>xy <sub>1</sub> ; xy <sub>2</sub> | Example 7 |

Compared to example 5 in example 7 a third STOVxy<sub>2</sub> is enabled and thus STOVxy<sub>2</sub> is generated additionally for both STIxy<sub>0</sub> and STIxy<sub>1</sub>.

A STOV interrupt is not generated if all stimulating STI interrupts are acknowledged.

A STIxy must be acknowledged by setting the ACKxy bit in the ASTI register two BCL clock (for DPS='0') or one BCL clocks (for DPS='1') before the time slot which is selected for the appropriate STIxy. The interrupt structure of the synchronous transfer is shown in [Figure 17](#).

## Functional Description



**Figure 17** Interrupt Structure of the Synchronous Data Transfer

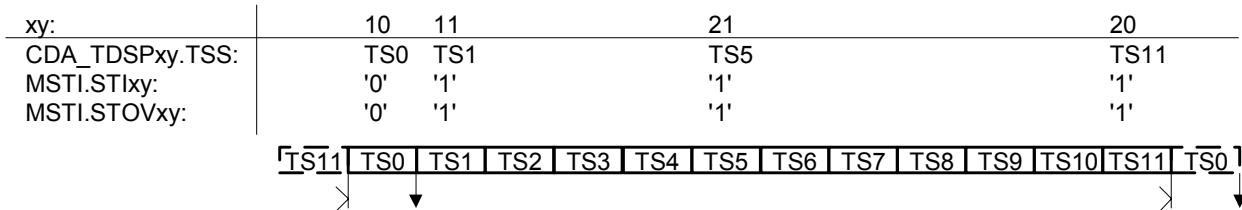
**Figure 18** shows some examples based on the timeslot structure. Figure a) shows at which point in time a STI and STOV interrupt is generated for a specific timeslot. Figure b) is identical to example 3 above, figure c) corresponds to example 5 and figure d) shows example 4.

## Functional Description

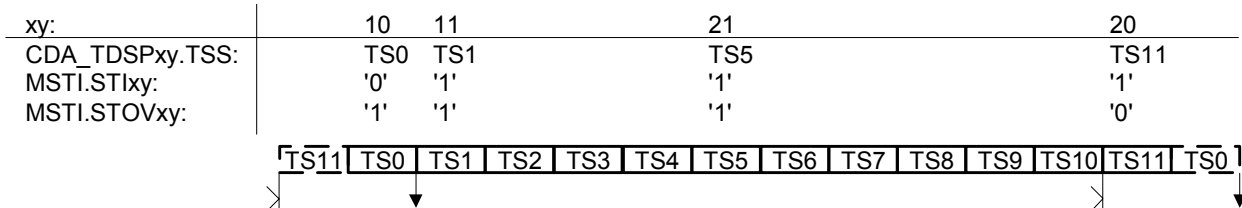
↓ : STI interrupt generated

⌋ : STOV interrupt generated for a not acknowledged STI interrupt

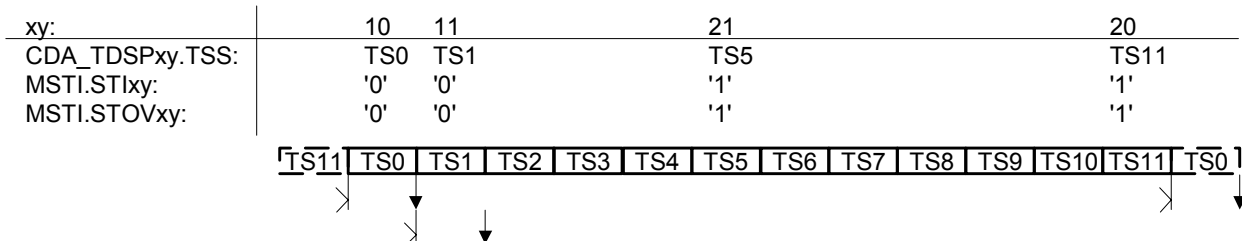
a) Interrupts for data access to time slot 0 (B1 after reset), MSTI.STI10 and MSTI.STOV10 enabled



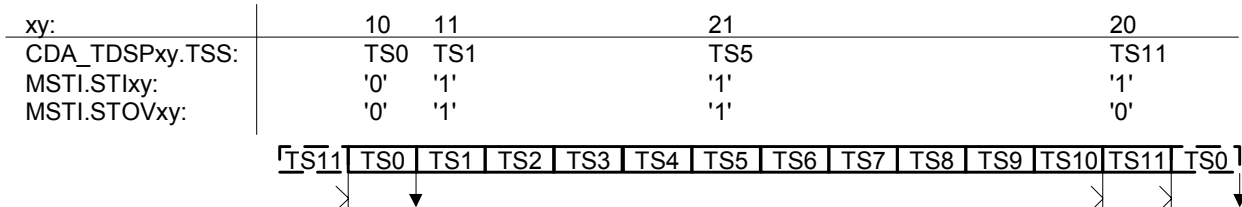
b) Interrupts for data access to time slot 0 (B1 after reset), STOV interrupt used as flag for "last possible CDA access"; MSTI.STI10 and MSTI.STOV20 enabled



c) Interrupts for data access to time slot 0 and 1 (B1 and B2 after reset), MSTI.STI10, MSTI.STOV10, MSTI.STI11 and MSTI.STOV11 enabled



d) Interrupts for data access to time slot 0 (B1 after reset), STOV20 interrupt used as flag for "last possible CDA access", STOV10 interrupt used as flag for "CDA access failed"; MSTI.STI10, MSTI.STOV10 and MSTI.STOV20 enabled



sti\_stov.vsd

**Figure 18 Examples for the Synchronous Transfer Interrupt Control with one STIxy enabled**

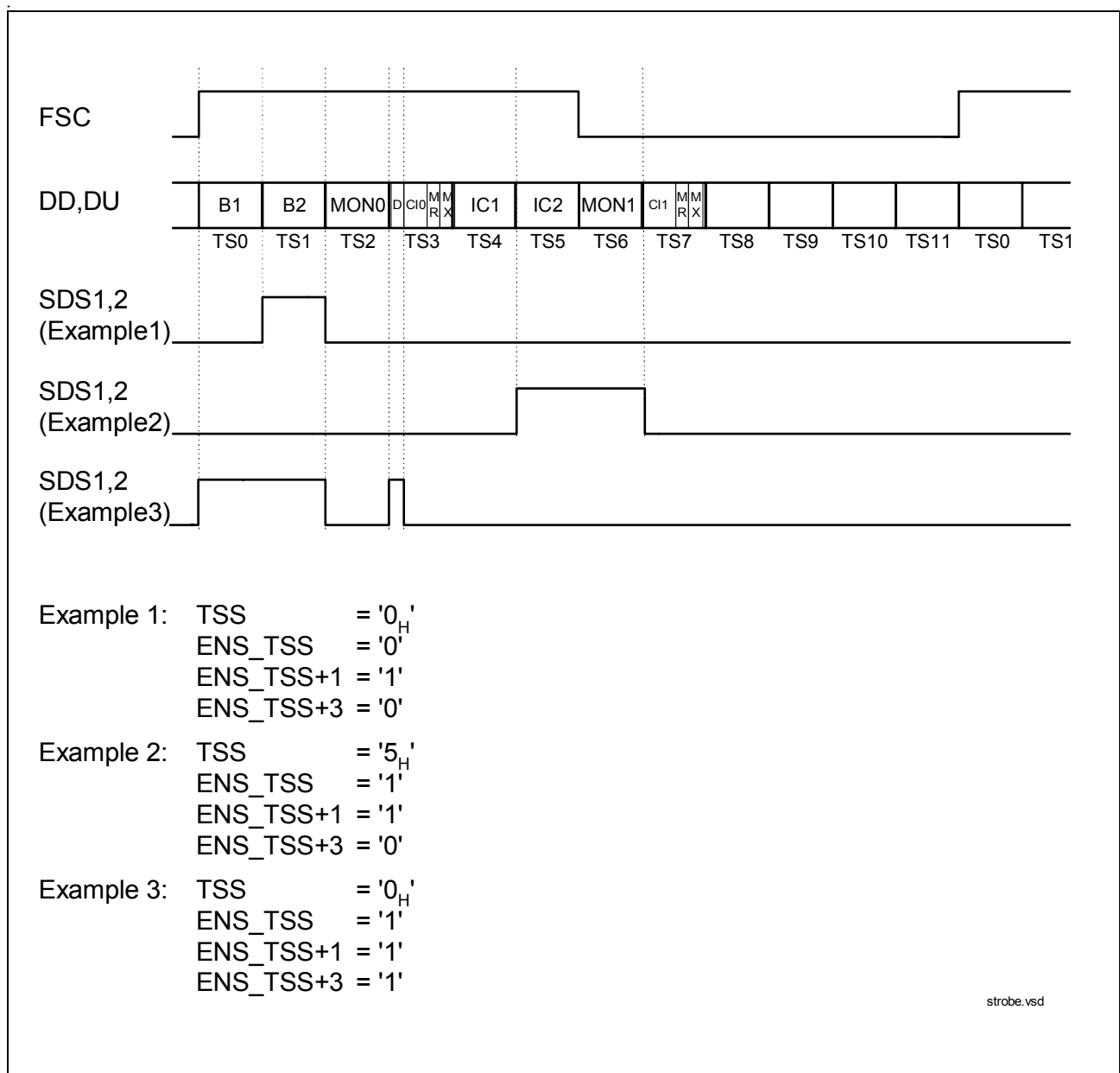
## Functional Description

### 2.3.2.2 Serial Data Strobe Signal

For time slot oriented standard devices at the IOM<sup>®</sup>-2 interface, the T-SMINT<sup>®</sup>I provides two independent data strobe signals SDS1 and SDS2.

The two strobe signals can be generated with every 8-kHz-frame and are controlled by the registers SDS1/2\_CR. By programming the TSS bits and three enable bits (ENS\_TSS, ENS\_TSS+1, ENS\_TSS+3) a data strobe can be generated for the IOM<sup>®</sup>-2 time slots TS, TS+1 and TS+3 (bit7,6) and the combinations of them.

The data strobes for TS and TS+1 are always 8 bits long (bit7 to bit0) whereas the data strobe for TS+3 is always 2 bits long (bit7, bit6).



**Figure 19 Data Strobe Signal Generation**

## Functional Description

**Figure 19** shows three examples for the generation of a strobe signal. In example 1 the SDS is active during channel B2 on IOM<sup>®</sup>-2, whereas in the second example during IC2 and MON1. The third example shows a strobe signal for 2B+D channels which is used e.g. at an IDSL (144 kbit/s) transmission.

### 2.3.3 IOM<sup>®</sup>-2 Monitor Channel

The IOM<sup>®</sup>-2 MONITOR channel is utilized for information exchange between the T-SMINT<sup>®</sup>I and other devices in the MONITOR channel.

The MONITOR channel data can be controlled by the bits in the MONITOR control register (MON\_CR). For the transmission of the MONITOR data one of the 3 IOM<sup>®</sup>-2 channels can be selected by setting the MONITOR channel selection bits (MCS) in the MONITOR control register (MON\_CR).

The DPS bit in the same register selects between an output on DU or DD respectively and with EN\_MON the MONITOR data can be enabled/disabled. The default value is MONITOR channel 0 (MON0) enabled and transmission on DD.

The MONITOR channel of the T-SMINT<sup>®</sup>I can be used in the following applications (refer also to and ):

- As a **master device** the T-SMINT<sup>®</sup>I can program and control other devices (e.g. PSB 2161) attached to the IOM<sup>®</sup>-2, which therefore, do not need a microcontroller interface.
- As a **slave device** the T-SMINT<sup>®</sup>I is programmed and controlled from a master device on IOM<sup>®</sup>-2 (e.g. UTAH). This is used in applications where no microcontroller is connected directly to the T-SMINT<sup>®</sup>I.

The MONITOR channel operates according to the IOM<sup>®</sup>-2 Reference Guide [12].

Note: In contrast to the NTC-T, the T-SMINT<sup>®</sup>I does neither issue nor react on Monitor commands (MON0,1,2,8). Instead, the T-SMINT<sup>®</sup>I operated in IOM<sup>®</sup>-2 slave mode must be programmed via new MONITOR channel concept (see [Chapter 2.3.3.4](#)), which provides full register access. The Monitor time out procedure is available. Reporting of the T-SMINT<sup>®</sup>I is performed via interrupts.

#### 2.3.3.1 Handshake Procedure

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR) and MONITOR Channel Transmit (MX) bits. Data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted once per 8-kHz frame until the transfer is acknowledged via the MR bit.

## Functional Description

The MONITOR channel protocol is described in the following section and [Figure 22](#) shall illustrate this. The relevant control and status bits for transmission and reception are listed in [Table 10](#) and [Table 11](#).

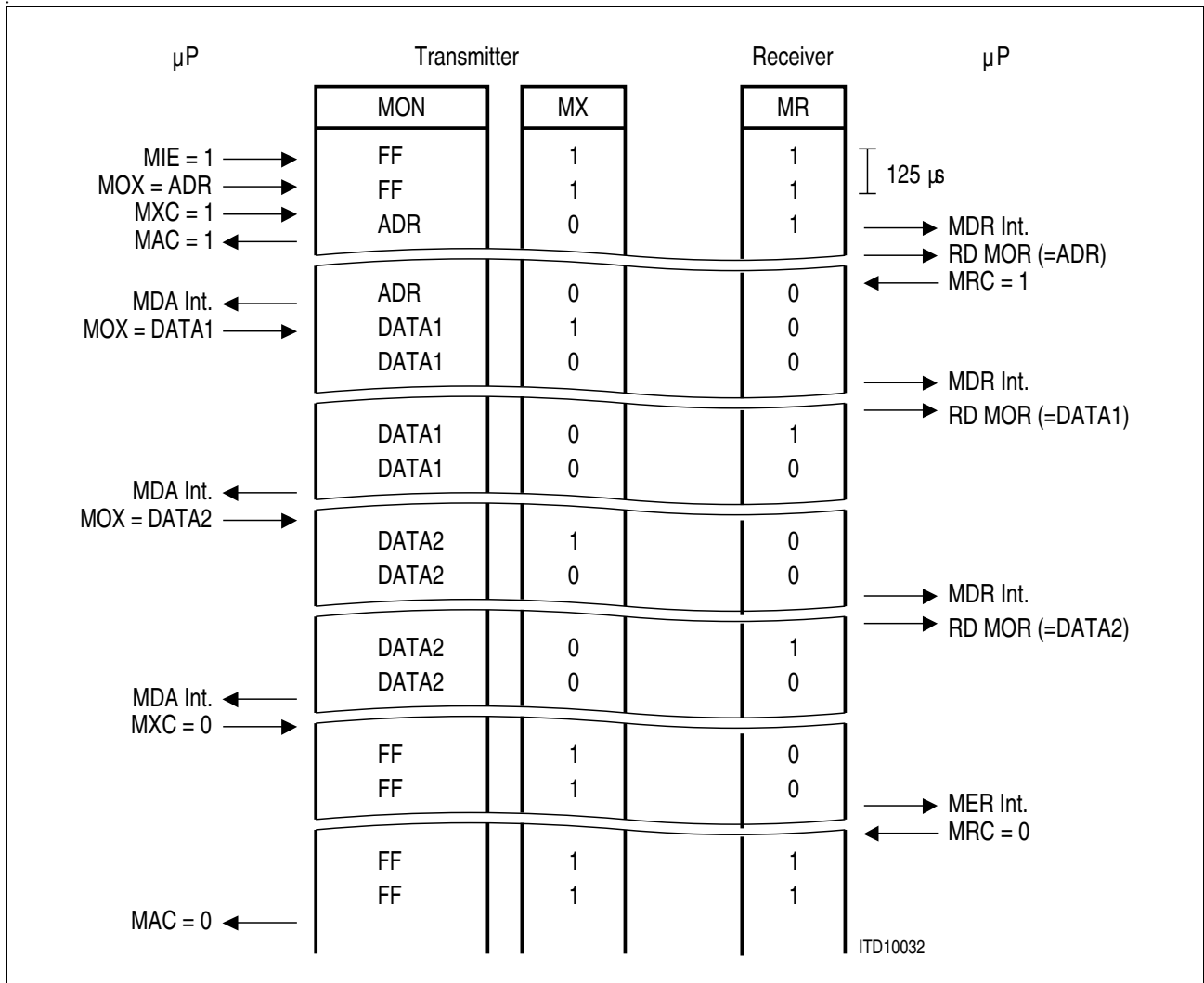
**Table 10 Transmit Direction**

| Control/<br>Status Bit | Register | Bit | Function                                  |
|------------------------|----------|-----|-------------------------------------------|
| Control                | MOCR     | MXC | MX Bit Control                            |
|                        |          | MIE | Transmit Interrupt (MDA, MAB, MER) Enable |
| Status                 | MOSR     | MDA | Data Acknowledged                         |
|                        |          | MAB | Data Abort                                |
|                        | MSTA     | MAC | Transmission Active                       |

**Table 11 Receive Direction**

| Control/<br>Status Bit | Register | Bit | Function                       |
|------------------------|----------|-----|--------------------------------|
| Control                | MOCR     | MRC | MR Bit Control                 |
|                        |          | MRE | Receive Interrupt (MDR) Enable |
| Status                 | MOSR     | MDR | Data Received                  |
|                        |          | MER | End of Reception               |

## Functional Description



**Figure 20 MONITOR Channel Protocol (IOM®-2)**

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a '0' in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to '1'. This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates a MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to '1' to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition,

## Functional Description

it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable (MIE) to '1'.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to '0'. This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to '0'. This enforces an inactive ('1') state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to '0'.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to '0'. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.

The MONITOR transfer protocol rules are summarized in the following section

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an **idle state** or an **end of transmission**.
- A **start of a transmission** is initiated by the transmitter by setting the MXC bit to '1' enabling the internal MX control. The receiver acknowledges the received first byte by setting the MR control bit to '1' enabling the internal MR control.
- The internal MX, MR control indicates or acknowledges a new byte in the MON slot by toggling MX, MR from the active to the inactive state for one frame.
- Two frames with the MR-bit set to inactive indicate a receiver request for **abort**.
- The transmitter can **delay a transmission** sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM<sup>®</sup>-2 frame following the first byte occurrence. Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.

## Functional Description

- Since a **double last-look criterion** is implemented the receiver is able to receive the MON slot data at least twice (in two consecutive frames), the receiver waits for the acknowledge of the reception of two identical bytes in two successive frames.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a **collision check** per bit on the transmitted MONITOR data and the MX bit.
- Monitor data will be transmitted repeatedly until its reception is acknowledged or the transmission time-out timer expires.
- Two frames with the MX bit in the inactive state indicates the **end of a message** (EOM).
- Transmission and reception of monitor messages can be performed simultaneously. This feature is used by the device to send back the response before the transmission from the controller is completed (the device does not wait for EOM from controller).

### 2.3.3.2 Error Treatment

In case the device does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the device will wait until two identical bytes are received in succession.

A transmission is aborted by the device if

- an error in the MR handshaking occurs
- a collision on the IOM<sup>®</sup>-2 bus of the MONITOR data or MX bit occurs
- the transmission time-out timer expires

A reception is aborted by the device if

- an error in the MX handshaking occurs or
- an abort request from the opposite device occurs

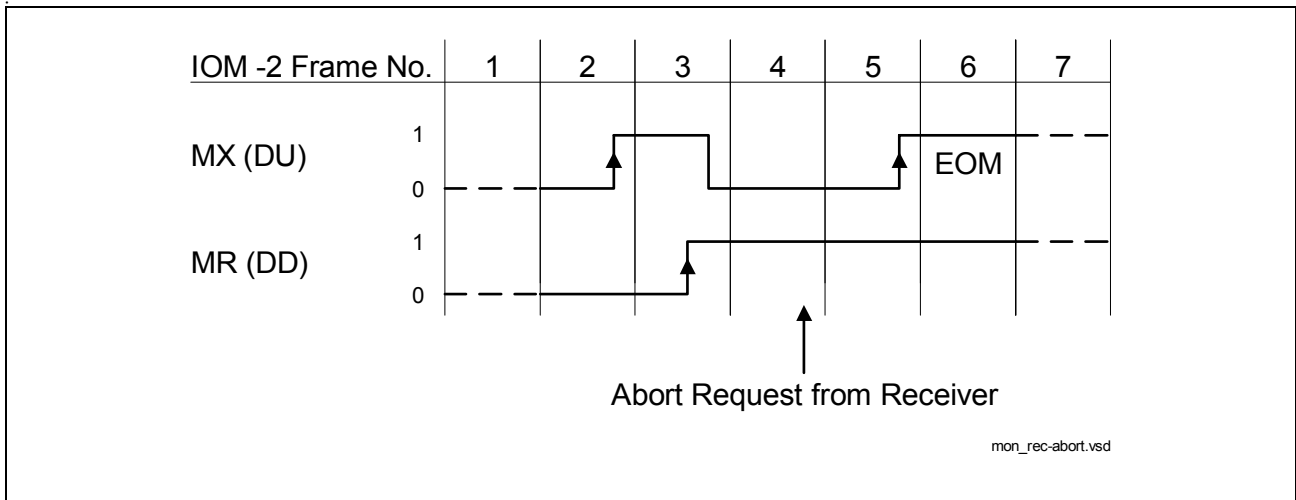
#### MX/MR Treatment in Error Case

In the master mode the MX/MR bits are under control of the microcontroller through MXC or MRC, respectively. An abort is indicated by an MAB interrupt or MER interrupt, respectively.

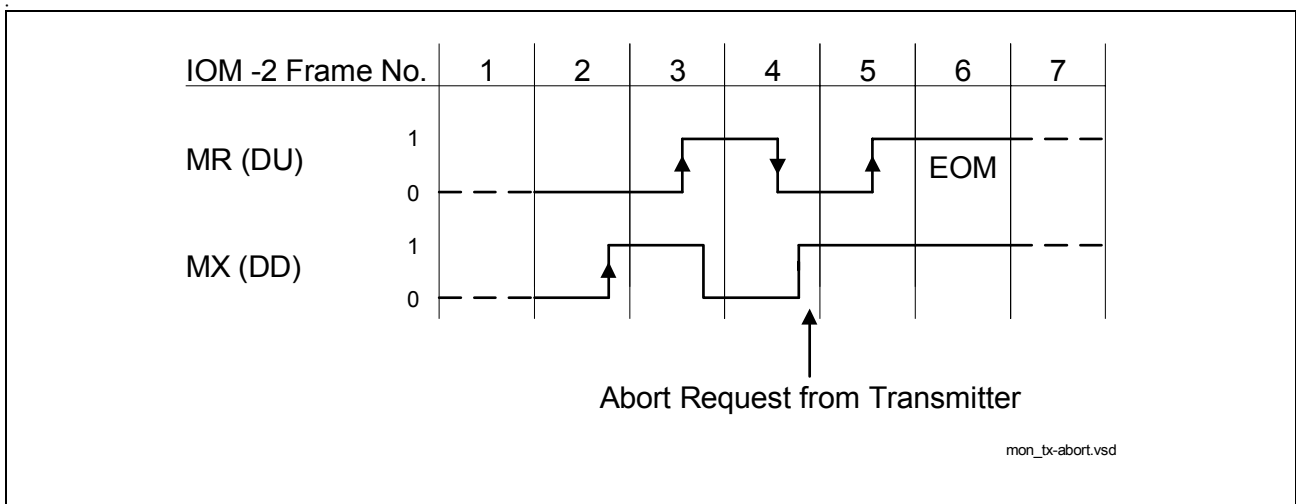
In the slave mode the MX/MR bits are under control of the device. An abort is always indicated by setting the MX/MR bit inactive for two or more IOM<sup>®</sup>-2 frames. The controller must react with EOM.

**Figure 21** shows an example for an abort requested by the receiver, **Figure 22** shows an example for an abort requested by the transmitter and **Figure 23** shows an example for a successful transmission.

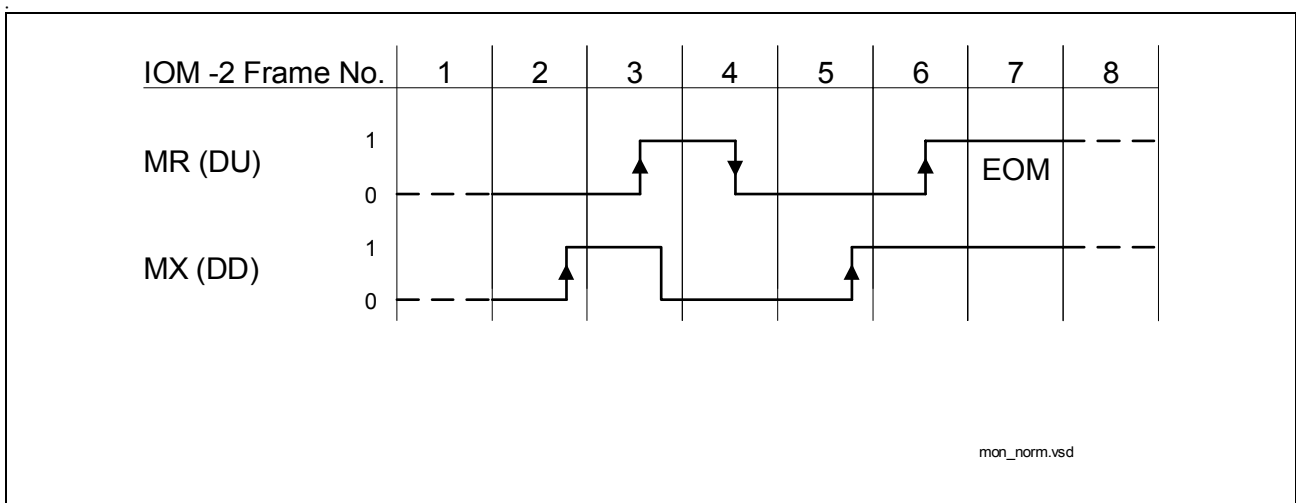
## Functional Description



**Figure 21 Monitor Channel, Transmission Abort requested by the Receiver**



**Figure 22 Monitor Channel, Transmission Abort requested by the Transmitter**



**Figure 23 Monitor Channel, Normal End of Transmission**

## Functional Description

### 2.3.3.3 MONITOR Channel Programming as a Master Device

The master mode is selected by default if one of the microcontroller interfaces is selected. The monitor data is written by the microcontroller in the MOX register and transmitted via IOM<sup>®</sup>-2 DD(DU) line to the programmed/controlled device e.g. ARCOFI-BA PSB 2161. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR.

### 2.3.3.4 MONITOR Channel Programming as a Slave Device

MONITOR slave mode can be selected by pinstrapping the microcontroller interface pins according to [Table 4](#). All programming data required by the device is received in the MONITOR time slot on the IOM<sup>®</sup>-2 and is transferred to the MOR register. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous [Chapter 2.3.3.1](#).

The first byte of the MONITOR message must contain in the higher nibble the MONITOR channel address code which is '1000' for the T-SMINT<sup>®</sup>I. The lower nibble distinguishes between a programming command and an identification command.

#### Identification Command

In order to be able to identify unambiguously different hardware designs of the T-SMINT<sup>®</sup>I by software, the following identification command is used:

|                   |   |   |   |   |   |   |   |   |
|-------------------|---|---|---|---|---|---|---|---|
| DU 1st byte value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DU 2nd byte value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The T-SMINT<sup>®</sup>I responds to this identification sequence by sending a identification sequence:

|                   |   |   |        |   |   |   |         |   |
|-------------------|---|---|--------|---|---|---|---------|---|
| DD 1st byte value | 1 | 0 | 0      | 0 | 0 | 0 | 0       | 0 |
| DD 2nd byte value | 0 | 0 | DESIGN |   |   |   | <IDENT> |   |

DESIGN: six bit code, specific for each device in order to identify differences in operation (see [“ID - Identification Register” on Page 139](#)).

This identification sequence is usually done once, when the T-SMINT<sup>®</sup>I is connected for the first time. This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

#### Programming Sequence

The programming sequence is characterized by a '1' being sent in the lower nibble of the received address code. **The data structure after this first byte is equivalent to the structure of the serial control interface described in chapter [Chapter 2.1.1](#).**

## Functional Description

|                         |             |                              |   |   |   |   |   |   |
|-------------------------|-------------|------------------------------|---|---|---|---|---|---|
| DU 1st byte value       | 1           | 0                            | 0 | 0 | 0 | 0 | 0 | 1 |
| DU 2nd byte value       | Header Byte |                              |   |   |   |   |   |   |
| DU 3rd byte value       | R/W         | Command/<br>Register Address |   |   |   |   |   |   |
| DU 4th byte value       | Data 1      |                              |   |   |   |   |   |   |
| DU (nth + 3) byte value | Data n      |                              |   |   |   |   |   |   |

All registers can be read back when setting the R/W bit to '1'. The T-SMINT<sup>®</sup>I responds by sending his IOM<sup>®</sup>-2 specific address byte (81<sub>h</sub>) followed by the requested data.

Note: Application Hint:

It is not allowed to disable the MX- and MR-control in the programming device at the same time! First, the MX-control must be disabled, then the  $\mu$ C has to wait for an End of Reception before the MR-control may be disabled. Otherwise, the T-SMINT<sup>®</sup>I does not recognize an End of Reception.

### 2.3.3.5 Monitor Time-Out Procedure

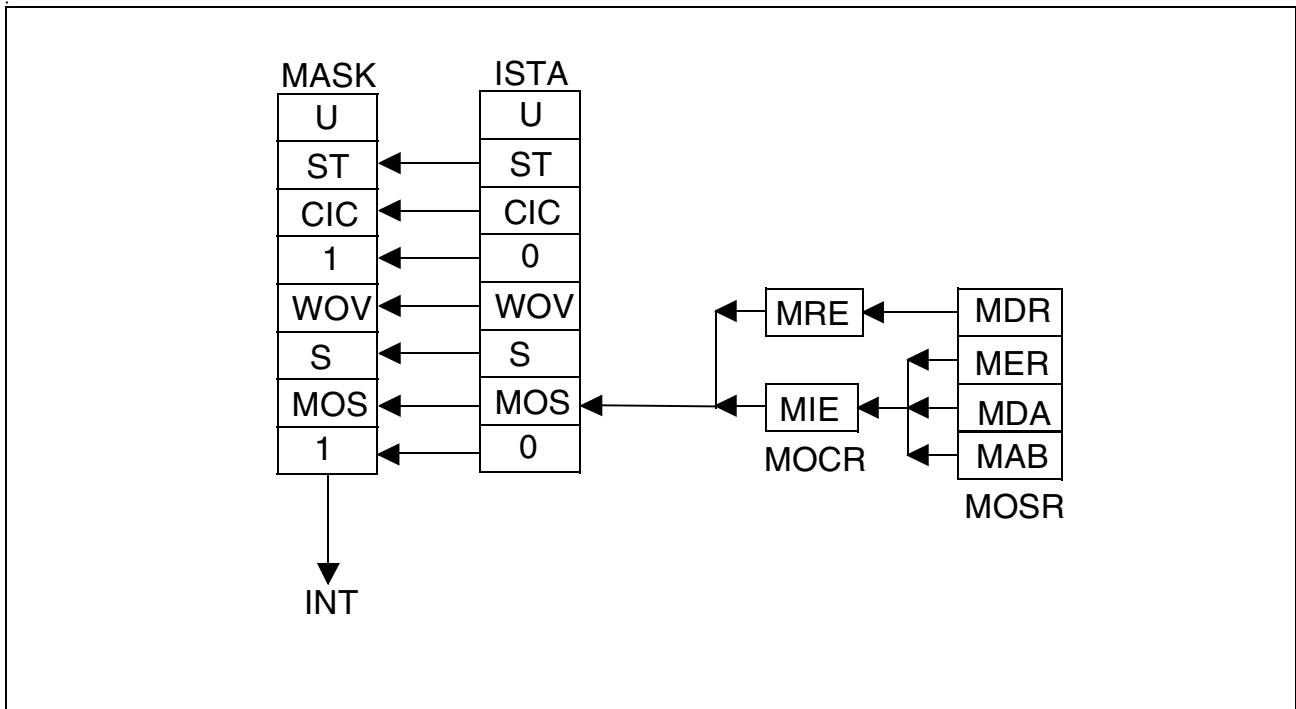
To prevent lock-up situations in a MONITOR transmission a time-out procedure can be enabled by setting the time-out bit (TOUT) in the MONITOR configuration register (MCONF). An internal timer is always started when the transmitter must wait for the reply of the addressed device or for transmit data from the microcontroller. After 40 IOM<sup>®</sup>-2 frames (5 ms) without reply the timer expires and the transmission will be aborted with an EOM (End of Message) command by setting the MX bit to '1' for two consecutive IOM<sup>®</sup>-2 frames.

### 2.3.3.6 MONITOR Interrupt Logic

**Figure 24** shows the interrupt structure of the MONITOR handler. The MONITOR Data Receive interrupt status MDR has two enable bits, MONITOR Receive interrupt Enable (MRE) and MR bit Control (MRC). The MONITOR channel End of Reception MER, MONITOR channel Data Acknowledged MDA and MONITOR channel Data Abort MAB interrupt status bits have a common enable bit MONITOR Interrupt Enable MIE.

MRE set to "0" prevents the occurrence of MDR status, including when the first byte of a packet is received. When MRE is set to "1" but MRC is set to "0", the MDR interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are set to "1", MDR is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. Additionally, a MRC set to "1" enables the control of the MR handshake bit according to the MONITOR channel protocol.

## Functional Description



**Figure 24 MONITOR Interrupt Structure**

### 2.3.4 C/I Channel Handling

The Command/Indication channel carries real-time status information between the T-SMINT<sup>®</sup>I and another device connected to the IOM<sup>®</sup>-2.

1) C/I0 channel lies in IOM<sup>®</sup>-2 channel 0 and access may be arbitrated via the TIC bus access protocol. In this case the arbitration is done in IOM<sup>®</sup>-2 channel 2.

The C/I0 channel is accessed via register CIR0 (received C/I0 data from DD) and register CIX0 (transmitted C/I0 data to DU). The C/I0 code is four bits long.

In the receive direction, the code from layer-1 is continuously monitored, with an interrupt being generated any time a change occurs (ISTA.CIC).

C/I0 only: a new code must be found in two consecutive IOM<sup>®</sup>-2 frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) lies in IOM<sup>®</sup>-2 channel 1 and is used to convey real time status information of the on-chip S-transceiver or an external device. The C/I1 channel consists of four or six bits in each direction. The width can be changed from 4 bit to 6 bit by setting bit CIX1.CICW.

## Functional Description

In 4-bit mode 6-bits are written whereby the higher 2 bits must be set to “1” and 6-bits are read whereby only the 4 LSBs are used for comparison and interrupt generation (i.e. the higher two bits are ignored).

The C/I1 channel is accessed via registers CIR1 and CIX1. The connection of CIR1 and CIX1 to DD and DU, respectively, can be selected by setting bit CI\_CR.DPS\_CI1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

### CIC Interrupt Logic

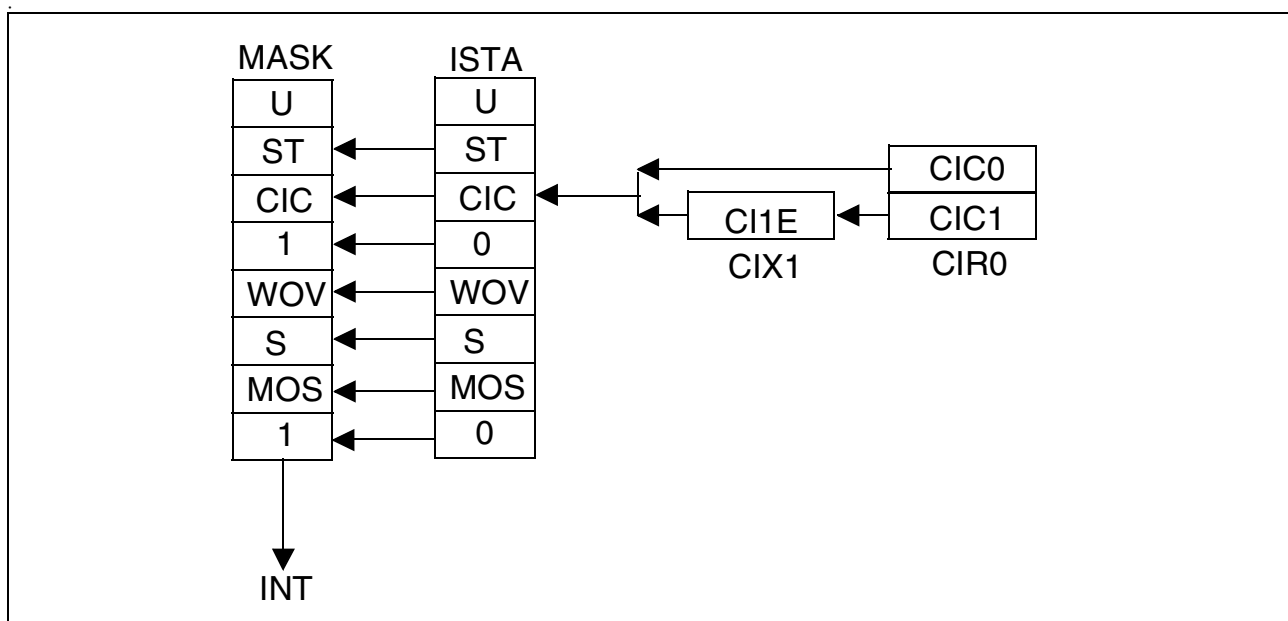
**Figure 25** shows the CIC interrupt structure.

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E in the CIX1 register. In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.

Bits CIC0 and CIC1 are cleared by a read of CIR0.

An interrupt status is indicated every time a valid new code is loaded in CIR0 or CIR1. The CIR0 is buffered with a FIFO size of two. If a second code change occurs in the received C/I channel 0 before the first one has been read, immediately after reading of CIR0 a new interrupt will be generated and the new code will be stored in CIR0. If several consecutive codes are detected, only the first and the last code are obtained at the first and second register read, respectively.

For CIR1 no FIFO is available. The actual code of the received C/I channel 1 is always stored in CIR1.



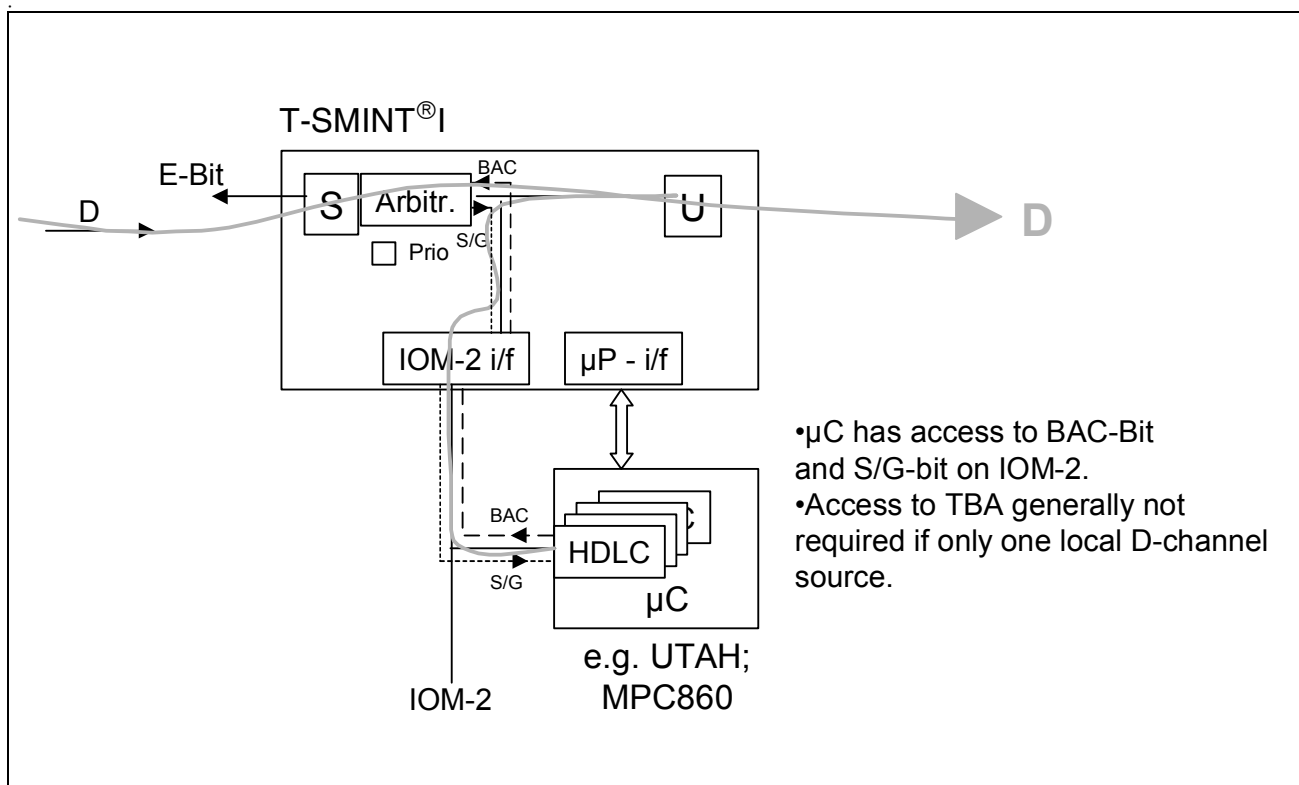
**Figure 25**     **CIC Interrupt Structure**

### 2.3.5 D-Channel Access Control

The upstream D-channel is arbitrated between the S-bus and external HDLC controllers via the TIC bus (S/G, BAC, TBA bits) according to the IOM<sup>®</sup>-2 Reference Guide<sup>1)</sup>. Further to the implementation in the INTC-Q it is possible, to set the priority (8 or 10) of all HDLC-controllers connected to IOM<sup>®</sup>-2, which is particularly useful for use of the T-SMINT<sup>®</sup>I together with the UTAH.

### 2.3.5.1 Application Examples for D-Channel Access Control

**Figure 26** and **Figure 27** show different scenarios for the local D-channel arbitration between the S-bus and the microcontroller.



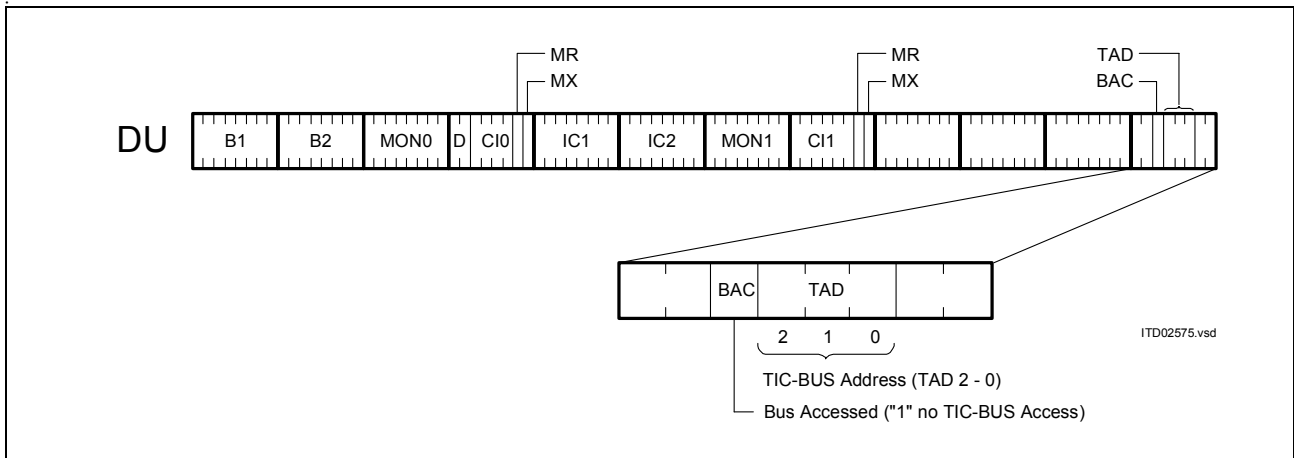
### Figure 26 D-Channel Arbitration: $\mu$ C with HDLC and Direct Access to TIC Bus

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<sup>1)</sup> The A/B-bit is not supported by the U-transceiver



## Functional Description



**Figure 28 Structure of Last Octet of Ch2 on DU**

When the TIC bus is seized by the T-SMINT<sup>®</sup>I, the bus is identified to other devices as occupied via the DU Ch2 Bus Accessed-bit state '0' until the access request is withdrawn. After a successful bus access, the T-SMINT<sup>®</sup>I is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM<sup>®</sup>-2 interface request access to the D and C/I0 channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I0 channels.

Note: Bit BAC (CI0 register) should be reset by the  $\mu$ C when access is no more requested, to grant other devices access to the D and C/I0 channels.

### 2.3.5.3 Stop/Go Bit Handling

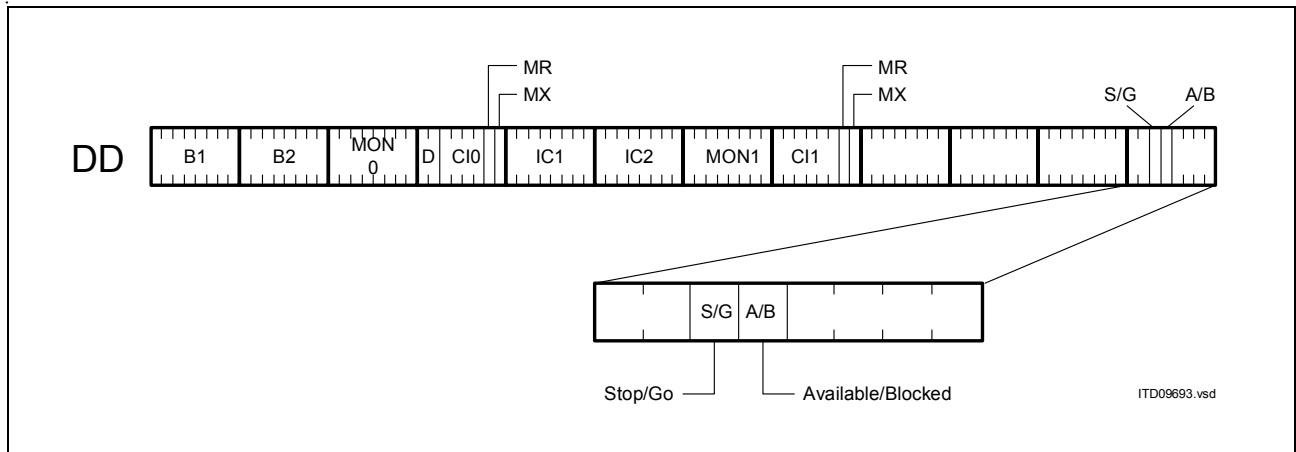
The availability of the DU D channel is indicated in bit 5 "Stop/Go" (S/G) of the last octet in DD channel 2 ([Figure 29](#)). The arbitration mechanism must be activated by setting MODEH.DIM2-0=0x1.

S/G = 1 : stop

S/G = 0 : go

The Stop/Go bit is available to other layer-2 devices connected to the IOM<sup>®</sup>-2 interface to determine if they can access the D channel in upstream direction.

## Functional Description



**Figure 29 Structure of Last Octet of Ch2 on DD**

### 2.3.5.4 D-Channel Arbitration

In intelligent NT applications (selected via register S\_MODE.MODE2-0) the T-SMINT<sup>®</sup>I has to share the upstream D-channel with one or more D-channel controllers on the IOM<sup>®</sup>-2 interface and with all connected TEs on the S interface.

The S-transceiver incorporates an elaborate state machine for D-channel priority handling on IOM<sup>®</sup>-2 ([Chapter 2.3.5.5](#)). For the access to the D-channel a similar arbitration mechanism as on the S interface (writing D-bits, reading back E-bits) is performed for all D-channel sources on IOM<sup>®</sup>-2. Due to this an equal and fair access is guaranteed for all D-channel sources on both the S interface and the IOM<sup>®</sup>-2 interface. The access to the upstream D-channel is handled via the S/G bit for the HDLC controllers and via E-bit for all connected terminals on S (E-bits are inverted to block the terminals on S). Furthermore, if more than one HDLC source is requesting D-channel access on IOM<sup>®</sup>-2 the TIC bus mechanism is used (see [Chapter 2.3.5.2](#)).

The arbiter permanently counts the “1s” in the upstream D-channel on IOM<sup>®</sup>-2. If the necessary number of “1s” is counted and an HDLC controller on IOM<sup>®</sup>-2 requests upstream D-channel access (BAC bit is set to 0), the arbiter allows this D-channel controller immediate access and blocks other TEs on S (E-bits are inverted). Similar as on the S-interface the priority for D-channel access on IOM<sup>®</sup>-2 can be configured to 8 or 10 (S\_CMD.DPRIO).

The configuration settings of the T-SMINT<sup>®</sup>I in intelligent NT applications are summarized in [Table 12](#).

## Functional Description

**Table 12 T-SMINT<sup>®</sup>I Configuration Settings in Intelligent NT Applications**

| Functional Block | Configuration Description             | Configuration Setting                                                                                                                                          |
|------------------|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Layer 1          | Select Intelligent NT mode            | S-Transceiver Mode Register:<br>S_MODE.MODE0 = 0 (NT state machine)<br>or<br>S_MODE.MODE0 = 1 (LT-S state machine)<br><br>S_MODE.MODE1 = 1<br>S_MODE.MODE2 = 1 |
| Layer 2          | Enable S/G bit and TIC bus evaluation | D-channel Mode Register:<br>MODEH.DIM2-0 = 001                                                                                                                 |

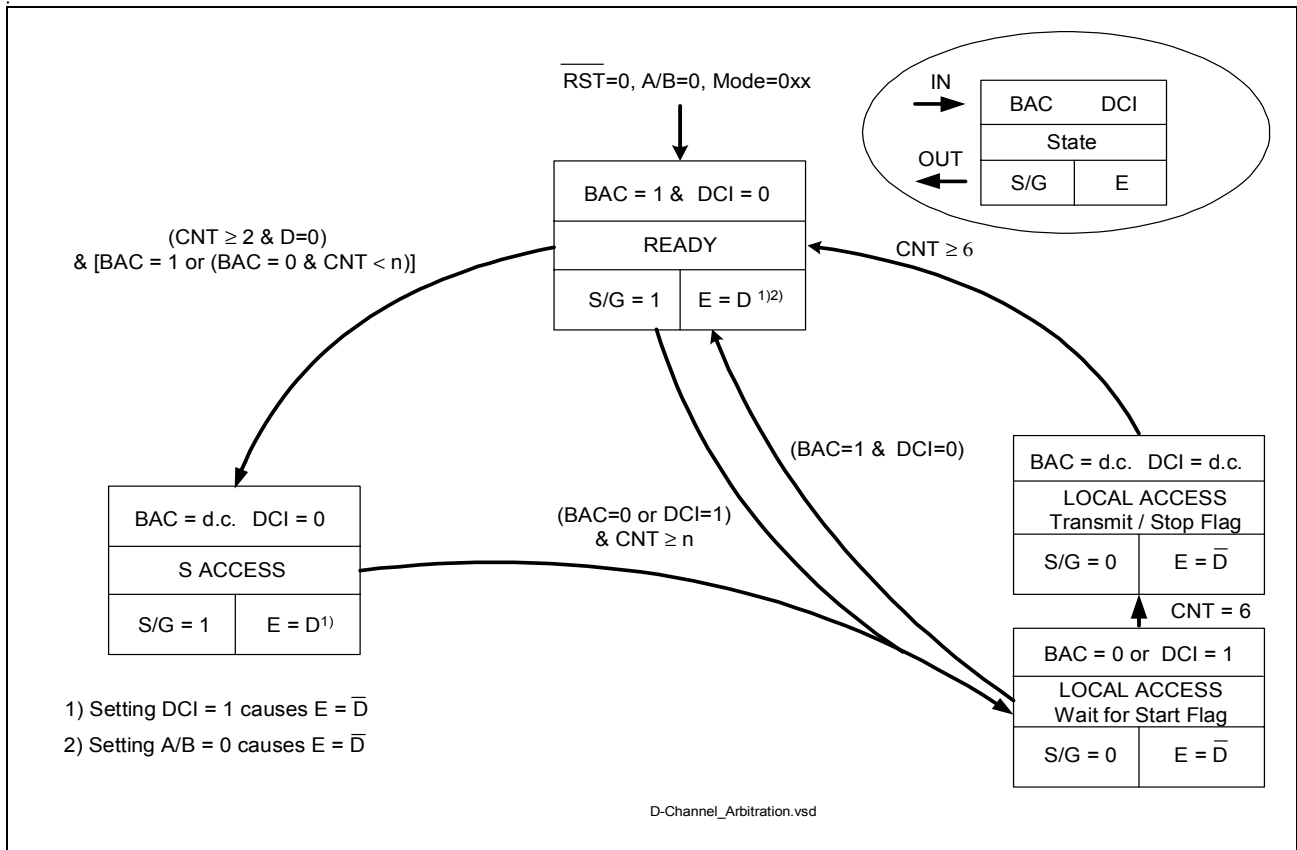
Note: For mode selection in the S\_MODE register the MODE1/2 bits are used to select intelligent NT mode, MODE0 selects NT or LT-S state machine.

With the configuration settings shown above the T-SMINT<sup>®</sup>I in intelligent NT applications provides for equal access to the D-channel for terminals connected to the S-interface and for D-channel sources on IOM<sup>®</sup>-2.

### 2.3.5.5 State Machine of the D-Channel Arbiter

**Figure 30** gives a simplified view of the state machine of the D-channel arbiter. CNT is the number of '1' on the IOM<sup>®</sup>-2 D-channel and BAC corresponds to the BAC-bit on IOM<sup>®</sup>-2. The number n depends on configuration settings (selected priority 8 or 10) and the condition of the previous transmission, i.e. if an abort was seen (n = 8 or 10, respectively) or if the last transmission was successful (n = 9 or 11, respectively).

## Functional Description



**Figure 30 State Machine of the D-Channel Arbiter (Simplified View)<sup>1)</sup>**

### 1. Local D-Channel Controller Transmits Upstream

In the initial state ('Ready' state) neither the local D-channel sources nor any of the terminals connected to the S-bus transmit in the D-channel.

The T-SMINT<sup>®</sup>I S-transceiver thus receives BAC = "1" (IOM<sup>®</sup>-2 DU line) and transmits S/G = "1" (IOM<sup>®</sup>-2 DD line). The access will then be established according to the following procedure:

- Local D-channel source verifies that BAC bit is set to ONE (currently no bus access).
- Local D-channel source issues TIC bus address and verifies that no controller with higher priority requests transmission (TIC bus access must always be performed even if no other D-channel sources are connected to IOM<sup>®</sup>-2).
- Local D-channel source issues BAC = "0" to block other sources on IOM<sup>®</sup>-2 and to announce D-channel access.
- T-SMINT<sup>®</sup>I S-transceiver pulls S/G bit to ZERO ('Local Access' state) as soon as CNT ≥ n (see note) to allow sending D-channel data from the entitled source.

<sup>1)</sup> If the S-transceiver is reset by SRES.RES\_S = '1' or disabled by S\_CONF0.DIS\_TR = '1', then the D-channel arbiter is in state Ready (S/G = '1'), too. The S/G evaluation of the HDLC has to be disabled in this case; otherwise, the HDLC is not able to send data.

## Functional Description

T-SMINT<sup>®</sup>I S-transceiver transmits inverted echo channel (E bits) on the S-bus to block all connected S-bus terminals ( $E = \bar{D}$ ).

- Local D-channel source commences with D data transmission on IOM<sup>®</sup>-2 as long as it receives S/G = "0".
- After D-channel data transmission is completed the controller sets the BAC bit to ONE.
- T-SMINT<sup>®</sup>I S-transceiver transmits non-inverted echo ( $E = D$ ).
- T-SMINT<sup>®</sup>I S-transceiver pulls S/G bit to ONE ('Ready' state) to block the D-channel controller on IOM<sup>®</sup>-2.

Note: If right after D-data transmission the D-channel arbiter goes to state 'Ready' and the local D-channel source wants to transmit again, then it may happen that the leading '0' of the start flag is written into the D-channel before the D-channel source recognizes that the S/G bit is pulled to '1' and stops transmission. In order to prevent unintended transitions to state 'S-Access', the additional condition  $CNT \geq 2$  is introduced. As soon as  $CNT \geq n$ , the S/G bit is set to '0' and the D-channel source may start transmission again (if TIC bus is occupied). This allows an equal access for D-channel sources on IOM<sup>®</sup>-2 and on the S interface.

## 2. Terminal Transmits D-Channel Data Upstream

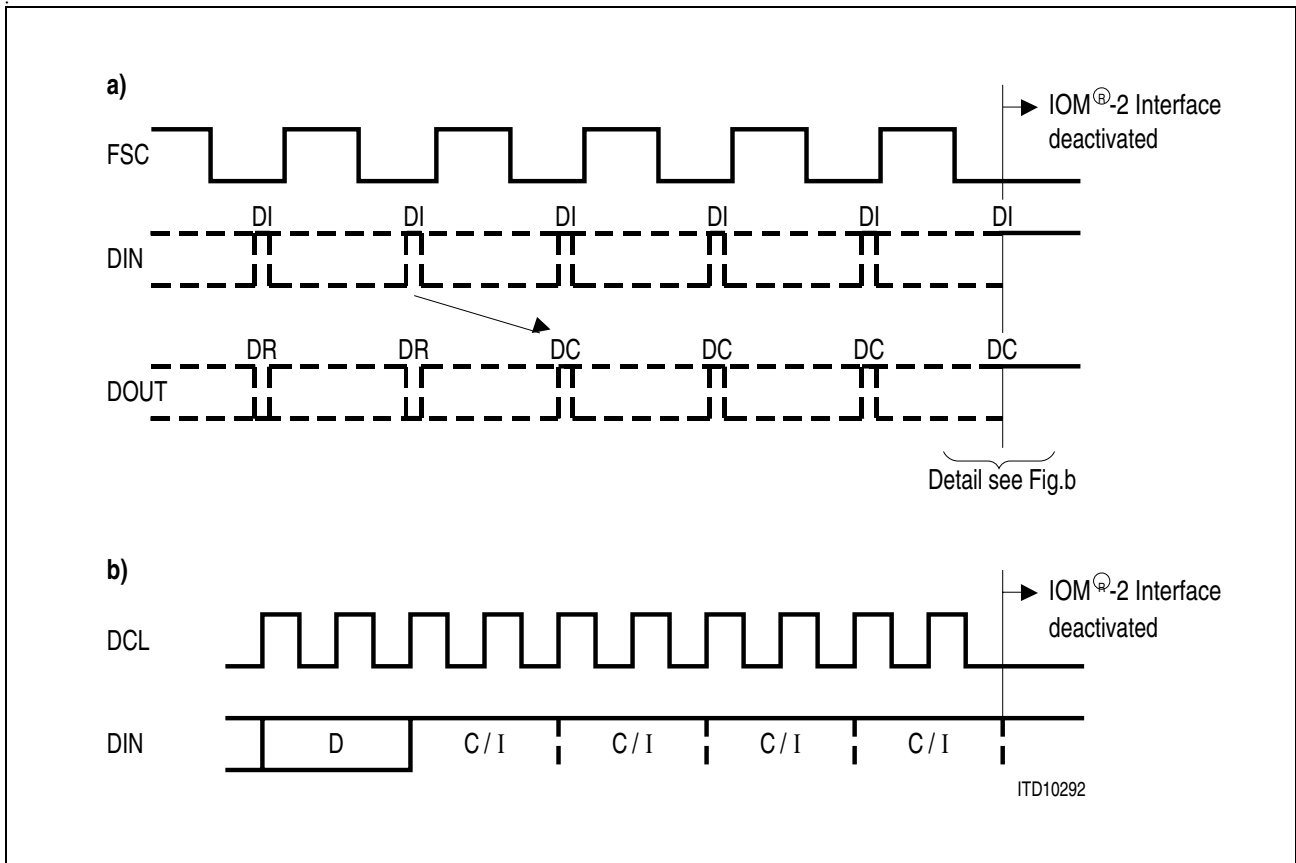
The initial state is identical to that described in the last paragraph. When one of the connected S-bus terminals needs to transmit in the D-channel, access is established according to the following procedure:

- S-transceiver recognizes that the D-channel on the S-bus is active via  $D = '0'$ .
- S-transceiver transfers S-bus D-channel data transparently through to the upstream IOM<sup>®</sup>-2 bus.

### 2.3.6 Activation/Deactivation of IOM<sup>®</sup>-2 Interface

The deactivation procedure of the IOM<sup>®</sup>-2 interface is shown in Figure 31. After detecting the code DI (Deactivation Indication) the T-SMINT<sup>®</sup>I responds by transmitting DC (Deactivation Confirmation) during subsequent frames and stops the timing signals after the fourth frame. The clocks stop at the end of the C/I-code in IOM<sup>®</sup>-2 channel 0.

## Functional Description



**Figure 31 Deactivation of the IOM<sup>®</sup>-2 Clocks**

### Conditions for Power-Down

If none of the following conditions is true, the IOM<sup>®</sup>-2 interface can be switched off, reducing power consumption to a minimum.

- S-transceiver is not in state 'Deactivated'
- Signal  $\overline{\text{INFO0}}$  on the S-interface
- Uk0-transceiver is not in state 'Deactivated'
- Pin DU is low (either at the IOM<sup>®</sup>-2 interface or via IOM\_CR.SPU)
- External pin  $\overline{\text{EAW}}$  External Awake is low
- Bit MODE 1.CFS = '0'
- Stop on the correct place in the IOM<sup>®</sup>-2 frame. DCL must be low during power down (stop on falling edge of DCL) (see [Figure 31](#)).

A deactivated IOM<sup>®</sup>-2 can be reactivated by one of the following methods:

- Pulling pin DU line low:
  - directly at the IOM<sup>®</sup>-2 interface
  - via the  $\mu\text{P}$  interface with "Software Power Up" (IOM\_CR:SPU bit)
- Pulling pin  $\overline{\text{EAW}}$  'External Awake' low
- Setting 'Configuration Select' MODE1:CFS bit = '0'
- Level detection at the S-interface

---

**Functional Description**

- Activation from the U-interface

## **2.4 U-Transceiver**

The statemachine of the U-Transceiver is compatible to the NT state machine in the PEB 8090 documentation [9], but includes some minor changes for simplification and compliance to Ref. [1].

The U-transceiver is configured and controlled via the registers described in [Chapter](#) . The U-transceiver is always in IOM<sup>®</sup>-2 channel 0.

### **2.4.1 4B3T Frame Structure**

The 4B3T U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI TS 102 080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance shall be such, that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock
  - 1 kHz Frame
  - Activation
  - 1 kbit/s Transparent Channel (M symbol), (not implemented)
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops (M symbol)
- From NT to LT side:
  - Indication of monitored code violations (M symbol)

### **Performance Requirements according to FTZ 1 TR 220 (August 1991):**

On the U-interface, the following transmission ranges are achieved without additional signal regeneration on the loop (bit error rate  $\leq 10^{-7}$ ):

- with noise:  $\geq 4.2$  km on wires of 0.4 mm diameter and  $\geq 8$  km on 0.6 mm wires
- without noise:  $\geq 5$  km on wires of 0.4 mm diameter and  $\geq 10$  km on 0.6 mm wires

*Note: Typical attenuation of FTZ wires of 0.4 mm diameter is about 7dB/km in contrast to ETSI wires of 0.4 mm with about 8dB/km.*

The transmission ranges can be doubled by inserting a repeater for signal regeneration.

## Functional Description

Performance requirements according to ETSI TS 102 080 are met, too.

1 ms frames are transmitted via the U-interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B1 + B2 + D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM<sup>®</sup>-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different syncwords are used for each direction:

- Downstream from LT to NT    + + + - - - + - - + -
- Upstream from NT to LT       - + - - + - - - + + +

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

|                 |                                                           |
|-----------------|-----------------------------------------------------------|
| $D_1 \dots D_8$ | Ternary 2B + D data of IOM <sup>®</sup> -2 frames 1 ... 8 |
| M               | Maintenance symbol                                        |
| +, -            | Syncword                                                  |

## Functional Description

**Table 13 Frame Structure A for Downstream Transmission LT to NT**

|                  |                  |                  |                  |                  |                  |                  |                  |                  |                |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------|------------------|------------------|
| 1                | 2                | 3                | 4                | 5                | 6                | 7                | 8                | 9                | 10             | 11               | 12               |
| D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub>   | D <sub>1</sub> | D <sub>1</sub>   | D <sub>1</sub>   |
| 13               | 14               | 15               | 16               | 17               | 18               | 19               | 20               | 21               | 22             | 23               | 24               |
| D <sub>1/2</sub> | D <sub>1/2</sub> | D <sub>1/2</sub> | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub> | D <sub>2</sub>   | D <sub>2</sub>   |
| 25               | 26               | 27               | 28               | 29               | 30               | 31               | 32               | 33               | 34             | 35               | 36               |
| D <sub>2</sub>   | D <sub>2</sub>   | D <sub>2</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub> | D <sub>3</sub>   | D <sub>3</sub>   |
| 37               | 38               | 39               | 40               | 41               | 42               | 43               | 44               | 45               | 46             | 47               | 48               |
| D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3</sub>   | D <sub>3/4</sub> | D <sub>3/4</sub> | D <sub>3/4</sub> | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub> | D <sub>4</sub>   | D <sub>4</sub>   |
| 49               | 50               | 51               | 52               | 53               | 54               | 55               | 56               | 57               | 58             | 59               | 60               |
| D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>4</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub> | D <sub>5</sub>   | D <sub>5</sub>   |
| 61               | 62               | 63               | 64               | 65               | 66               | 67               | 68               | 69               | 70             | 71               | 72               |
| D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5</sub>   | D <sub>5/6</sub> | D <sub>5/6</sub> | D <sub>5/6</sub> | D <sub>6</sub> | D <sub>6</sub>   | D <sub>6</sub>   |
| 73               | 74               | 75               | 76               | 77               | 78               | 79               | 80               | 81               | 82             | 83               | 84               |
| D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>6</sub>   | D <sub>7</sub> | D <sub>7</sub>   | D <sub>7</sub>   |
| 85               | 86               | 87               | 88               | 89               | 90               | 91               | 92               | 93               | 94             | 95               | 96               |
| <b>M</b>         | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub>   | D <sub>7</sub> | D <sub>7/8</sub> | D <sub>7/8</sub> |
| 97               | 98               | 99               | 100              | 101              | 102              | 103              | 104              | 105              | 106            | 107              | 108              |
| D <sub>7/8</sub> | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub>   | D <sub>8</sub> | D <sub>8</sub>   | D <sub>8</sub>   |
| 109              | 110              | 111              | 112              | 113              | 114              | 115              | 116              | 117              | 118            | 119              | 120              |
| D <sub>8</sub>   | +                | +                | +                | -                | -                | -                | +                | -                | -              | +                | -                |

## Functional Description

**Table 14**      **Frame Structure B for Upstream Transmission NT to LT**

|                  |                  |                  |                |                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 1                | 2                | 3                | 4              | 5                | 6                | 7                | 8                | 9                | 10               | 11               | 12               |
| U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub> | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   | U <sub>1</sub>   |
| 13               | 14               | 15               | 16             | 17               | 18               | 19               | 20               | 21               | 22               | 23               | 24               |
| U <sub>1/2</sub> | U <sub>1/2</sub> | U <sub>1/2</sub> | U <sub>2</sub> | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub>   |
| 25               | 26               | 27               | 28             | 29               | 30               | 31               | 32               | 33               | 34               | 35               | 36               |
| <b>M</b>         | U <sub>2</sub>   | U <sub>2</sub>   | U <sub>2</sub> | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   |
| 37               | 38               | 39               | 40             | 41               | 42               | 43               | 44               | 45               | 46               | 47               | 48               |
| U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub>   | U <sub>3</sub> | U <sub>3/4</sub> | U <sub>3/4</sub> | U <sub>3/4</sub> | U <sub>4</sub>   | U <sub>4</sub>   | U <sub>4</sub>   | U <sub>4</sub>   | U <sub>4</sub>   |
| 49               | 50               | 51               | 52             | 53               | 54               | 55               | 56               | 57               | 58               | 59               | 60               |
| U <sub>4</sub>   | -                | +                | -              | -                | +                | -                | -                | -                | +                | +                | +                |
| 61               | 62               | 63               | 64             | 65               | 66               | 67               | 68               | 69               | 70               | 71               | 72               |
| U <sub>4</sub>   | U <sub>4</sub>   | U <sub>4</sub>   | U <sub>4</sub> | U <sub>4</sub>   | U <sub>4</sub>   | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub>   |
| 73               | 74               | 75               | 76             | 77               | 78               | 79               | 80               | 81               | 82               | 83               | 84               |
| U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5</sub> | U <sub>5</sub>   | U <sub>5</sub>   | U <sub>5/6</sub> | U <sub>5/6</sub> | U <sub>5/6</sub> | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub>   |
| 85               | 86               | 87               | 88             | 89               | 90               | 91               | 92               | 93               | 94               | 95               | 96               |
| U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub> | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>6</sub>   | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub>   |
| 97               | 98               | 99               | 100            | 101              | 102              | 103              | 104              | 105              | 106              | 107              | 108              |
| U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub> | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7</sub>   | U <sub>7/8</sub> | U <sub>7/8</sub> | U <sub>7/8</sub> |
| 109              | 110              | 111              | 112            | 113              | 114              | 115              | 116              | 117              | 118              | 119              | 120              |
| U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub> | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   | U <sub>8</sub>   |

U<sub>1</sub> ... U<sub>8</sub>      Ternary 2B + D data of IOM<sup>®</sup>-2 frames 1... 8

M                  Maintenance symbol

+, -                Syncword

## Functional Description

### 2.4.2 Maintenance Channel

The 4B3T frame structure provides a 1 kbit/s M(aintenance)-channel for the transfer of remote loopback commands and error indications.

#### Loopback Commands

The LT station uses the M-channel to request remote loopbacks. Loopback commands are coded with a series of '0' and '+' symbols.

- A continuous series of '+' requests for loopback 2 activation in the NT
- A continuous series of '0' requests for deactivation of any loopback

The NT station reacts as soon as the pattern has been detected in 8 consecutive symbols.

#### Error Indications

The NT U-transceiver reports line code violations via the M-channel to the exchange by setting one M-Bit to '+' polarity.

#### Transparent Messages

The exchange of Transparent Messages via the Transparent Channel is not supported by the T-SMINT<sup>®</sup>I.

### 2.4.3 Coding from Binary to Ternary Data

Each 4 bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to [Table 15](#).

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

**Table 15 MMS 43 Coding Table**

|         | S1      | S2      | S3      | S4      |
|---------|---------|---------|---------|---------|
| t →     | t →     | t →     | t →     | t →     |
| 0 0 0 1 | 0 - + 1 | 0 - + 2 | 0 - + 3 | 0 - + 4 |
| 0 1 1 1 | - 0 + 1 | - 0 + 2 | - 0 + 3 | - 0 + 4 |
| 0 1 0 0 | - + 0 1 | - + 0 2 | - + 0 3 | - + 0 4 |
| 0 0 1 0 | + - 0 1 | + - 0 2 | + - 0 3 | + - 0 4 |
| 1 0 1 1 | + 0 - 1 | + 0 - 2 | + 0 - 3 | + 0 - 4 |
| 1 1 1 0 | 0 + - 1 | 0 + - 2 | 0 + - 3 | 0 + - 4 |
| 1 0 0 1 | + - + 2 | + - + 3 | + - + 4 | - - - 1 |

## Functional Description

**Table 15 MMS 43 Coding Table**

|         | S1      | S2      | S3      | S4      |
|---------|---------|---------|---------|---------|
| 0 0 1 1 | 0 0 + 2 | 0 0 + 3 | 0 0 + 4 | – – 0 2 |
| 1 1 0 1 | 0 + 0 2 | 0 + 0 3 | 0 + 0 4 | – 0 – 2 |
| 1 0 0 0 | + 0 0 2 | + 0 0 3 | + 0 0 4 | 0 – – 2 |
| 0 1 1 0 | – + + 2 | – + + 3 | – – + 2 | – – + 3 |
| 1 0 1 0 | + + – 2 | + + – 3 | + – – 2 | + – – 3 |
| 1 1 1 1 | + + 0 3 | 0 0 – 1 | 0 0 – 2 | 0 0 – 3 |
| 0 0 0 0 | + 0 + 3 | 0 – 0 1 | 0 – 0 2 | 0 – 0 3 |
| 0 1 0 1 | 0 + + 3 | – 0 0 1 | – 0 0 2 | – 0 0 3 |
| 1 1 0 0 | + + + 4 | – + – 1 | – + – 2 | – + – 3 |

### 2.4.4 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in [Table 16](#).

As in the encoding table, the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

**Table 16 4B3T Decoding Table**

| Ternary Block       | Binary Block |
|---------------------|--------------|
| 0 0 0, + 0 +, 0 – 0 | 0 0 0 0      |
| 0 – +               | 0 0 0 1      |
| + – 0               | 0 0 1 0      |
| 0 0 +, – – 0        | 0 0 1 1      |
| – + 0               | 0 1 0 0      |
| 0 + +, – 0 0        | 0 1 0 1      |
| – + +, – – +        | 0 1 1 0      |
| – 0 +               | 0 1 1 1      |
| + 0 0, 0 – –        | 1 0 0 0      |
| + – +, – – –        | 1 0 0 1      |
| + + –, + – –        | 1 0 1 0      |
| + 0 –               | 1 0 1 1      |
| + + +, – + –        | 1 1 0 0      |

## Functional Description

**Table 16**      **4B3T Decoding Table**

|        |       |   |   |   |   |
|--------|-------|---|---|---|---|
| 0 + 0, | – 0 – | 1 | 1 | 0 | 1 |
| 0 + –  |       | 1 | 1 | 1 | 0 |
| + + 0, | 0 0 – | 1 | 1 | 1 | 1 |

### 2.4.4.1 Monitoring of Code Violations

The running digital sum monitor (RDSM) computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, –1). At the end of each block, the running digital sum is supposed to reflect the number of the next column in [Table 15](#).

A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0 (three user symbols with zero polarity) is found in the received data.

If at the end of a ternary block no error was found, the running digital sum retains its current value. If the counter value is greater than 4, it is set to 4 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDSM synchronizes itself within a period depending on the received data pattern. Note there are some transmission errors which do not cause a code violation.

### 2.4.4.2 Block Error Counter (RDS Error Counter)

The T-SMINT<sup>®</sup>I provides a block error counter. This feature allows monitoring the transmission quality on the U-interface.

On the NT side a block error is given, if a U-frame with at least one code violation has been detected (near-end block error). In the following frame the NT transmits a positive M-symbol upstream.

On the LT side a block error is given, if a U-frame with at least one code violation has been detected (near-end block error) or a positive M-symbol has been received from the NT (far-end block error).

The current status of the block error counter can be retrieved by the system interface. When the block error counter is read (register RDS), it is automatically reset. The counter is enabled in all states listed in [Table 17](#) and reset in all other states. The counter is saturated at its maximum value (255).

**Table 17**      **Active States**

|                   |
|-------------------|
| SBC Synchronizing |
| Wait for INFO U4H |
| Transparent       |

## Functional Description

Note that every frame with a detected code violation causes about 10 to 20 binary bit errors on average. So a bit error rate of  $10^{-7}$  in both directions is equivalent to 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M-symbol).

### 2.4.5 Scrambler / Descrambler

#### Scrambler

The binary transmit data from the IOM<sup>®</sup>-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambler polynomial is::

$$z^{-23} + z^{-18} + 1$$

#### Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is forwarded to the IOM<sup>®</sup>-2 interface. The descrambler is self synchronized after 23 symbols. The descrambler polynomial is::

$$z^{-23} + z^{-5} + 1$$

The scrambling / descrambling process is controlled fully by the T-SMINT<sup>®</sup>I. Hence, no influence can be taken by the user.

### 2.4.6 Command/Indication Codes

Both commands and indications depend on the data direction. [Table 18](#) presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM<sup>®</sup>-2 frames (double last-look criterion).

Note: Unconditional C/I-commands must be applied for at least 4 IOM<sup>®</sup>-2 frames for reliable recognition by the U-transceiver.

Indications are strictly state orientated. Refer to the state diagrams in the following sections for commands and indications applicable in various states.

**Table 18 C/I Codes**

| Code | IN  | OUT |
|------|-----|-----|
| 0000 | TIM | DR  |
| 0001 | —   | —   |
| 0010 | —   | —   |

## Functional Description

|      |                        |     |
|------|------------------------|-----|
| 0011 | LTD                    | –   |
| 0100 | –                      | RSY |
| 0101 | SSP                    | –   |
| 0110 | DT                     | –   |
| 0111 | –                      | –   |
| 1000 | AR                     | AR  |
| 1001 | reserved <sup>1)</sup> | –   |
| 1010 | –                      | ARL |
| 1011 | –                      | –   |
| 1100 | AI                     | AI  |
| 1101 | RES                    | –   |
| 1110 | –                      | AIL |
| 1111 | DI                     | DC  |

<sup>1)</sup> C/I code '1010' must not be input to the U-transceiver.

|     |                               |     |                              |
|-----|-------------------------------|-----|------------------------------|
| AI  | Activation Indication         | DI  | Deactivation Indication.     |
| AIL | Activation Indication Loop 2  | DR  | Deactivation Request         |
| AR  | Activation Request            | LTD | LT Disable                   |
| ARL | Activation Request Local Loop | RES | Reset                        |
| DT  | Data Through Mode             | RSY | Resynchronization Indication |
| DC  | Deactivation Confirmation     | SSP | Send-Single-Pulses           |
|     |                               | TIM | Timing Request               |

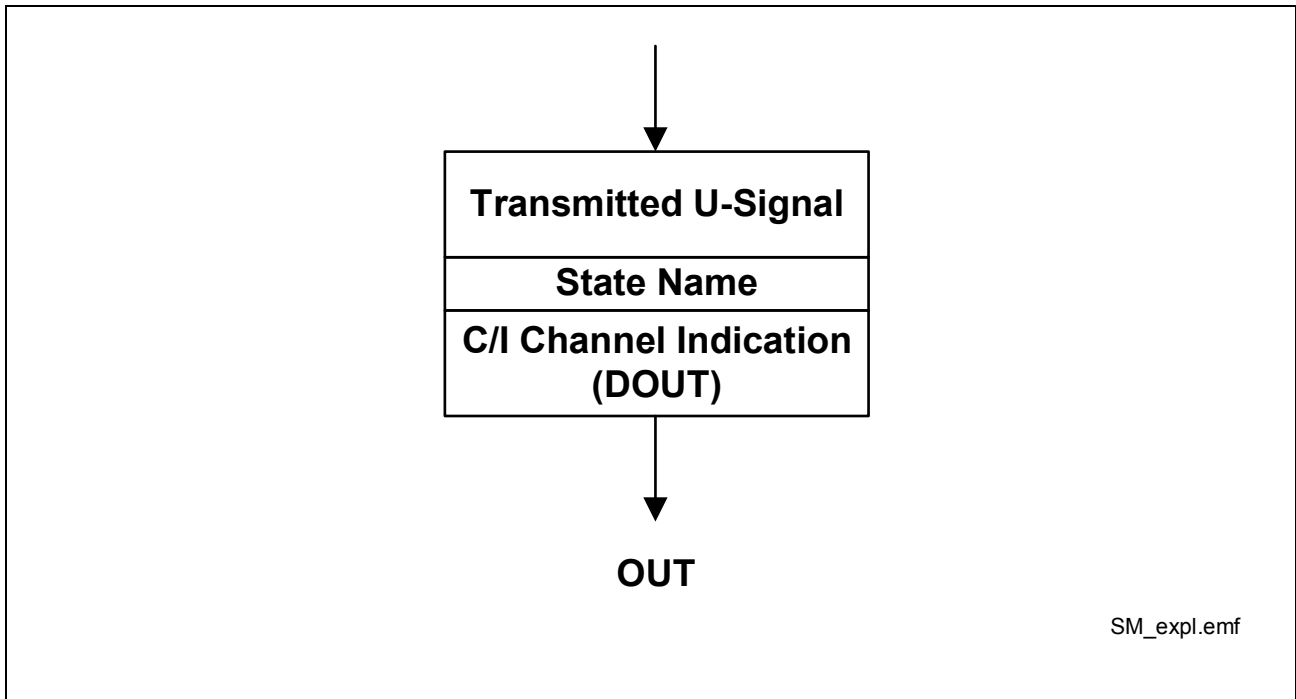
## 2.4.7 State Machine for Activation and Deactivation

### 2.4.7.1 State Machine Notation

The following state diagram describes all the actions/reactions resulting from any command or detected signal and resulting from the various operating modes.

The states with its inputs and outputs are interpreted as shown below:

## Functional Description



**Figure 32 State Diagram Example**

Each state has one or more transitions to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions exist.

At some transitions, an internal timer is started. The start of a timer is indicated by TxS ('x' is the timer number). Transitions that are caused if a timer has expired are labelled by TxE.

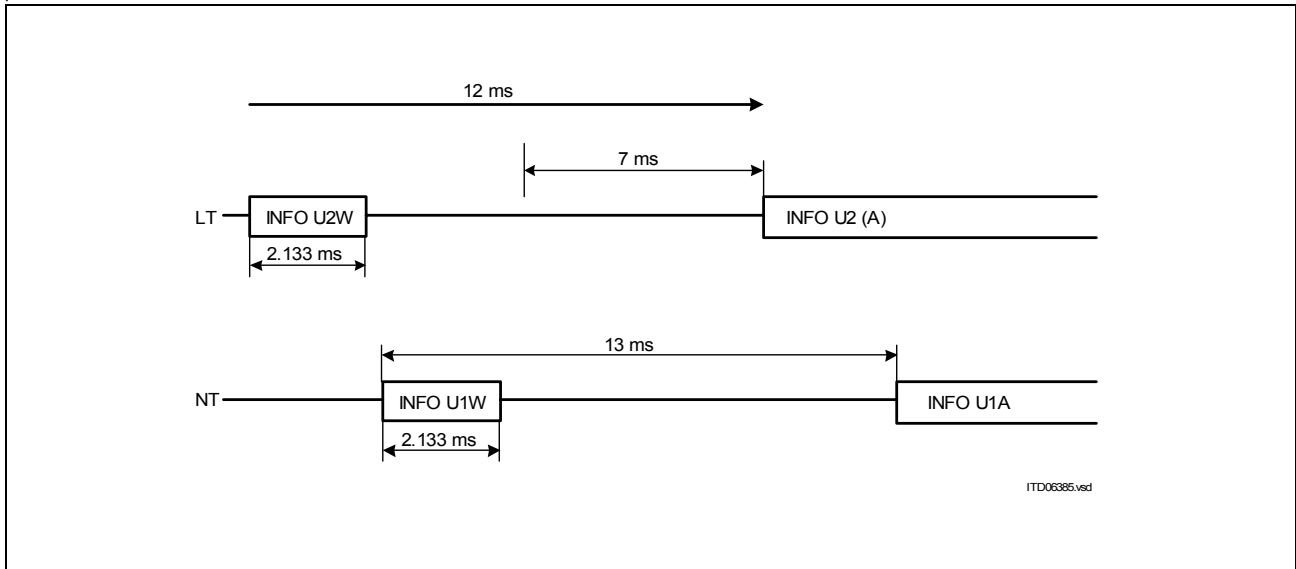
Some conditions lead to the same target state. To reduce the number of lines and the complexity of the figures, a state named "ANY STATE" acts on behalf of all state.

The state machines are designed to cope with all ISDN devices with IOM<sup>®</sup>-2 standard interfaces. Undefined situations are excluded. In any case, the involved devices will enter defined conditions as soon as the line is deactivated.

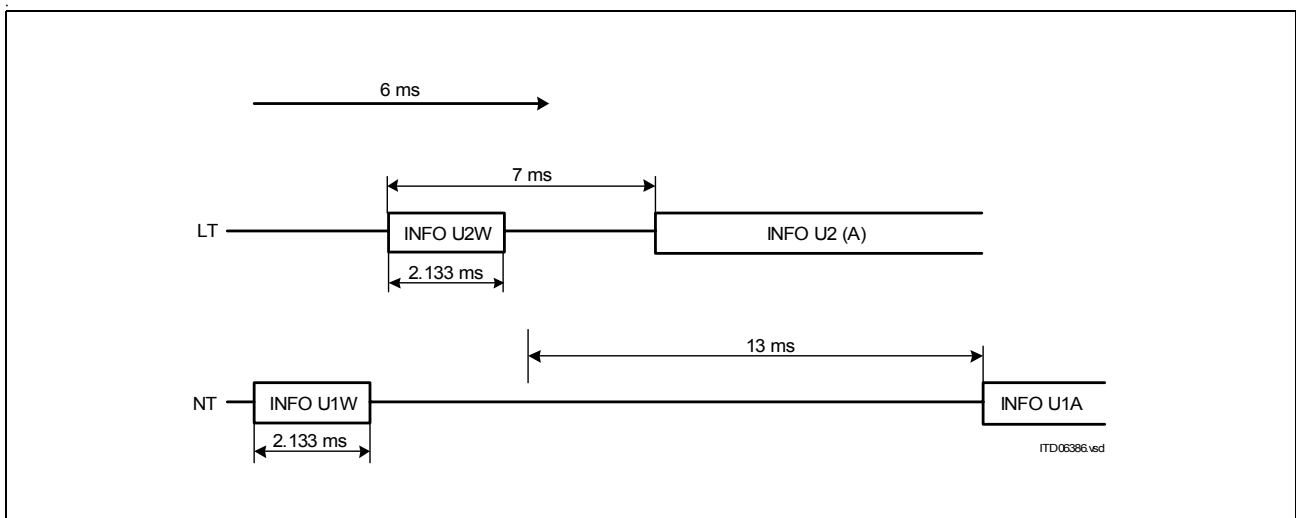
### 2.4.7.2 Awake Protocol

For the awake process two signals are defined 'U1W' and 'U2W'. Depending on the call direction (up-, downstream) U1W and U2W are interpreted as awake or acknowledge signals (see figures below).

## Functional Description



**Figure 33** Awake Procedure initiated by the LT



**Figure 34** Awake Procedure initiated by the NT

### Acting as Calling Station

After sending the awake signal, the awaking U-transceiver waits for the acknowledge. After 12 ms, the awake signal is repeated, if no acknowledge has been recognized.

If an acknowledge signal has been recognized, the U-transceiver waits for its possible repetition (in case of previous coincidence of two awake signals). If no repetition was detected, the U-transceiver starts transmitting U2 with a delay of 7 ms.

If such a repetition is detected, the U-transceiver interprets it as an awake signal and behaves like a device awoken by the far end.

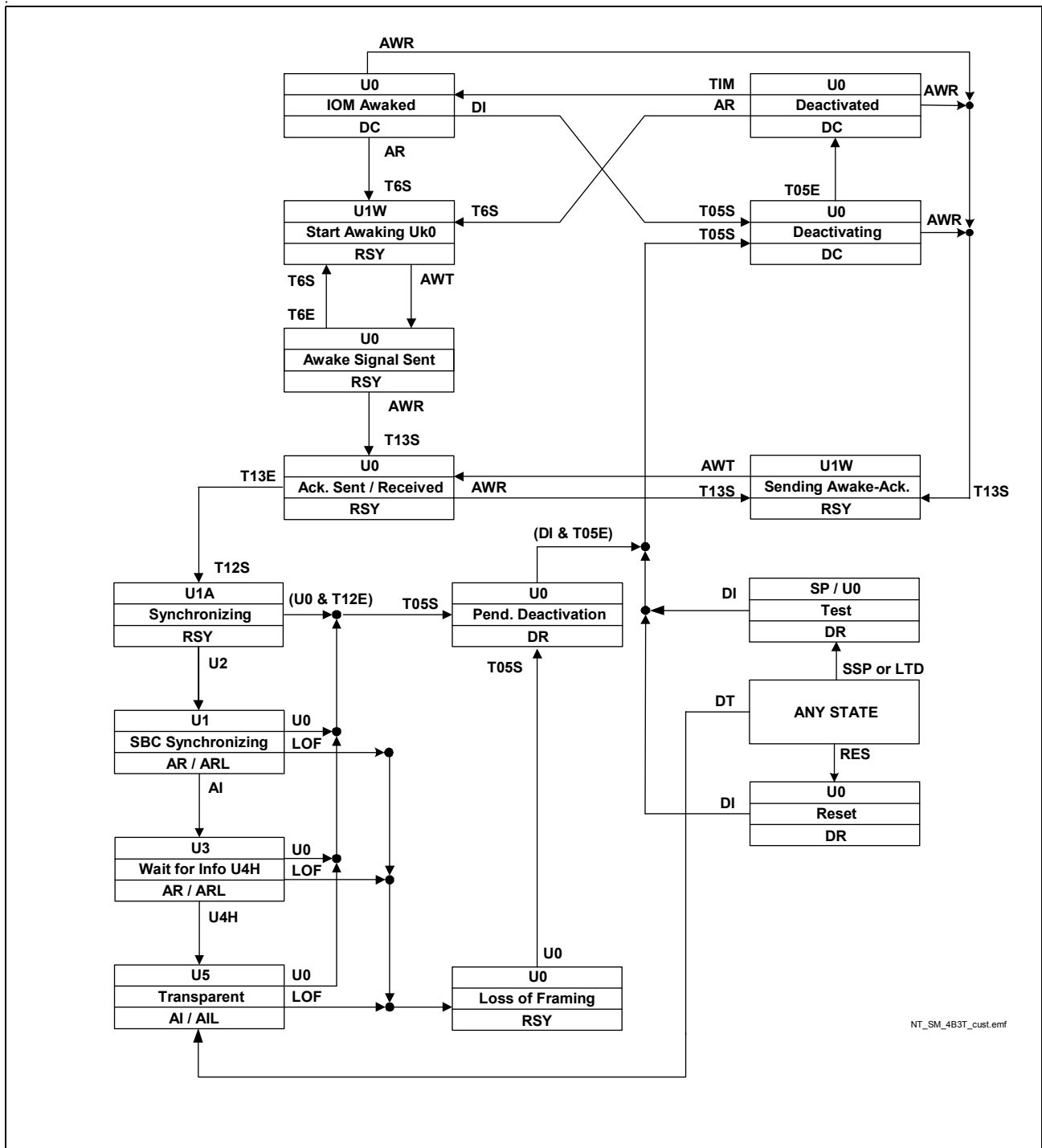
---

**Functional Description****Acknowledging a Wake-Up Call**

If a deactivated device detects an awake signal on U, an acknowledge signal is sent out. After that, the U-transceiver waits for a possible repetition of the awake signal (in case the acknowledge hasn't been recognized).

If no repetition is found, the awoken U-transceiver starts sending U2 after 7 ms from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken U-transceiver starts again.

### 2.4.7.3 NT State Machine (IEC-T / NTC-T Compatible)



### Figure 35 NT State Machine (IEC-T/NTC-T Compatible)

Note: The test modes 'Data Through' (DT) and 'Send Single Pulses' (SSP) are invoked via C/I codes 'DT' and 'SSP' according to [Table 18](#). Setting SRES.RES\_U to '1' forces the U-transceiver into test mode 'Quiet Mode' (QM), i.e. the U-transceiver is hardware reset.

## Functional Description

**Table 19 Differences to the former NT-SM of the IEC-T/NTC-T**

| No. | State/ Signal               | Change                                                                                                                                              | Comment                                                       |
|-----|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| 1.  | State 'Deact. Request Rec.' | split into 3 states<br>- 'Pend. Deactivation 1'<br>- 'Reset' State<br>- 'Test' State                                                                | simplifies SM implementation                                  |
| 2.  | State 'Loss of Framing'     | new inserted,<br>results in different behavior<br>in state 'Transparent',<br>no return to normal<br>transmission possible after<br>detection of LOF | compliance to ETSI TS 102 080,<br>corresponds to state NT1.10 |
| 3.  | C/I-code LTD                | new inserted                                                                                                                                        |                                                               |
| 4.  | State 'Power Down'          | renamed to state 'Deactivated'                                                                                                                      | for consistency reasons to 2B1Q                               |
| 5.  | State 'Data Transmission'   | renamed to state 'Transparent'                                                                                                                      |                                                               |
| 6.  | Timer variables introduced  | Name Duration                                                                                                                                       | see <a href="#">Table 20</a>                                  |

### 2.4.7.4 Inputs to the U-Transceiver

#### C/I-Commands

- AI**      Activation Indication  
The downstream device issues this indication to announce that layer 1 is available. The U-transceiver in turn informs the LT side by transmitting U3.
- AR**      Activation Request  
The U-transceiver is requested to start the activation process (if not already done) by sending the wake-up signal U1W.
- DI**      Deactivation Indication  
This indication is used during a deactivation procedure to inform the U-transceiver that it may enter the 'Deactivated' (power-down) state.
- DT**      Data Through Test Mode  
This unconditional command is used for test purposes only and forces the U-transceiver into state 'Transparent'.

## Functional Description

|     |                                                                                                                                           |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| LTD | LT Disable<br>This unconditional command forces the U-transceiver to state 'Test', where it transmits U0. No further action is initiated. |
| RES | Reset<br>Unconditional command which resets the U-transceiver.                                                                            |
| SSP | Send Single Pulses<br>Unconditional command which requests the transmission of single pulses on the U-interface.                          |
| TIM | Timing<br>The U-transceiver is requested to enter state 'IOM Awaked'.                                                                     |

### U-Interface Events

|     |                                                                                                                                                                                   |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U0  | U0 detected<br>U0 is recognized after 120 symbols (1ms) with zero level in a row. Detection may last up to 2 ms.                                                                  |
| U2  | U2 detected<br>The U-transceiver detects U2 if continuous binary 0's are found after descrambling and LOF = 0 for at least 8 subsequent U-frames. U2 is detected after 8 to 9 ms. |
| U4H | U4H detected<br>U4H is recognized, if the U-transceiver detects 16 subsequent binary 1's after descrambling.                                                                      |
| AWR | Awake signal (U2W) detected                                                                                                                                                       |
| AWT | Awake signal (U1W) has been sent out                                                                                                                                              |
| LOF | Loss of Framing on U-interface                                                                                                                                                    |
| TxE | Timer ended, the started timer has expired                                                                                                                                        |

### Timers

The start of timers is indicated by TxS, the expiry by TxE. The following table shows which timers are used.

**Table 20 Timers**

| Timer | Duration (ms) | Function                  | State                            |
|-------|---------------|---------------------------|----------------------------------|
| T05   | 0.5           | C/I code recognition      | Pend. Deactivation, Deactivating |
| T6    | 6             | Supervises U1W repetition | Start Awakening Uk0              |

**Functional Description**
**Table 20 Timers (cont'd)**

| Timer | Duration (ms) | Function                                                                                                                    | State                                      |
|-------|---------------|-----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|
| T12   | 12            | Prevents the U-transceiver in state Synchronizing from immediate transition to state 'Pend. Deactivation' if U0 is detected | Synchronizing                              |
| T13   | 13            | Supervises U2W repetition                                                                                                   | Ack. sent / received<br>Sending awake-ack. |

**2.4.7.5 Outputs of the U-Transceiver**

Below the signals and indications are summarized that are issued on IOM<sup>®</sup>-2 (C/I indications) and on the U-interface (predefined U-signals).

**C/I Indications**

- AI**      Activation Indication  
The U-transceiver has established transparency of transmission. The downstream device is requested to establish layer-1 functionality.
- AIL**     Activation Indication Loop-back  
The U-transceiver has established transparency of transmission. The downstream device is requested to establish a loopback #2.
- AR**      Activation Request  
The downstream device is requested to start the activation procedure.
- ARL**     Activation Request Loop-back  
The U-transceiver has detected a loop-back 2 command in the M-channel and has established transparency of transmission in the direction IOM<sup>®</sup> to U-interface. The downstream device is requested to start the activation procedure and to establish a loopback #2.
- DC**      Deactivation Confirmation  
Idle code on the IOM<sup>®</sup>-2 interface.
- DR**      Deactivation Request  
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation. The downstream device is requested to start the deactivation procedure.
- RSY**     Resynchronizing Indication  
RSY informs the downstream device that the U-transceiver is not synchronous.

## Functional Description

### Signals on U-Interface

The signals U0, U1W, U1A, U1, U3, U5 and SP are transmitted on the U-interface. They are defined in [Table 25](#).

### Signals on IOM<sup>®</sup>-2

The Data (B+B+D) is set to all '1's in all states besides the states listed in [Table 17](#).

### Dependence of Outputs

The M-symbol output in states with valid M-symbol output its value is set according to [Table 21](#)

**Table 21 M Symbol Output**

|                        |              |          |
|------------------------|--------------|----------|
| <b>RDS Error</b>       | not detected | detected |
| <b>M Symbol Output</b> | '0'          | '+'      |

**Table 22 Signal Output on Uk0 in State Test**

|                             |                      |                                |
|-----------------------------|----------------------|--------------------------------|
| <b>Input</b>                | C/I-Code SSP applied | all other except C/I-Code 'DI' |
| <b>Signal Output on Uk0</b> | SP                   | U0                             |

**Table 23 C/I-Code Output**

| <b>Loopback Command</b> | <b>SBC Synchronizing</b> | <b>Wait for Info U4H</b> | <b>Transparent</b> |
|-------------------------|--------------------------|--------------------------|--------------------|
| not received            | AR                       | AR                       | AI                 |
| received                | ARL                      | ARL                      | AIL                |

### 2.4.7.6 NT-States

In this section each state is described with its function.

#### Acknowledge Sent / Receive

After having sent the awake signal, the U-transceiver has received the acknowledge wake tone. If being awoken the U-transceiver has sent the acknowledge. In both cases the U-transceiver waits for possible repetition or time-out.

---

## Functional Description

### **Awake Signal Sent**

The NT has sent out the awake signal U1W and waits now for a response. If the LT does not react in time timer T6 expires and the NT repeats its wake-up call.

### **Deactivated**

Only in “Deactivated” state the device may enter the power-down mode.

### **Deactivating**

State Deactivating assures that the C/I-channel code DC is issued four times before entering the 'Deactivated' state.

### **IOM<sup>®</sup> Awaked**

The U-transceiver is deactivated, but may not enter the power-down mode.

### **Loss of Framing**

This state is entered on loss of framing (LOF). No signal is transmitted on the U-interface. A receiver-reset is performed by.

Note that there is no return to the 'Transparent' state that has been possible before in the former IEC-T based state machine.

### **Pending Deactivation**

The U-transceiver has received U0. The U-transceiver remains at least 0.5ms in this state before it accepts DI.

### **SBC Synchronizing**

The NT is now synchronized and indicates this by AR/ARL towards the downstream device. The NT waits for the acknowledge 'AI' from the downstream device.

### **Sending Awake-Ack.**

On the receipt of the awake signal U2W the U-transceiver responds with the transmission of U1W.

### **Start Awakening Uk0**

On the receipt of AR in the C/I-channel the U-transceiver sends the awake signal U1W to start an activation.

---

## Functional Description

### Synchronizing

After the successful awake procedure the U-transceiver trains its receiver coefficients until it is able to detect the signals U2.

### Reset

In state 'Reset' a software-reset is performed.

### Test

State "Test" is entered when the unconditional commands C/I=SSP is applied. The test signal SSP is issued as long as pin SSP is active or C/I=SSP is applied.

### Transparent

The transmission line is fully activated. User data is transparently exchanged by U4/U5. Transparent state is entered in the case of a loopback 2. The downstream device is informed by C/I code AI that the transparent state has been reached

Note that in contrast to the former IEC-T state machine there is no resynchronization mechanism. Once loss of framing (LOF) has been detected a deactivation is initiated.

### Wait for Info U4H

The NT is synchronized and waits now for the permission (U4H) to go to the 'Transparent' state.

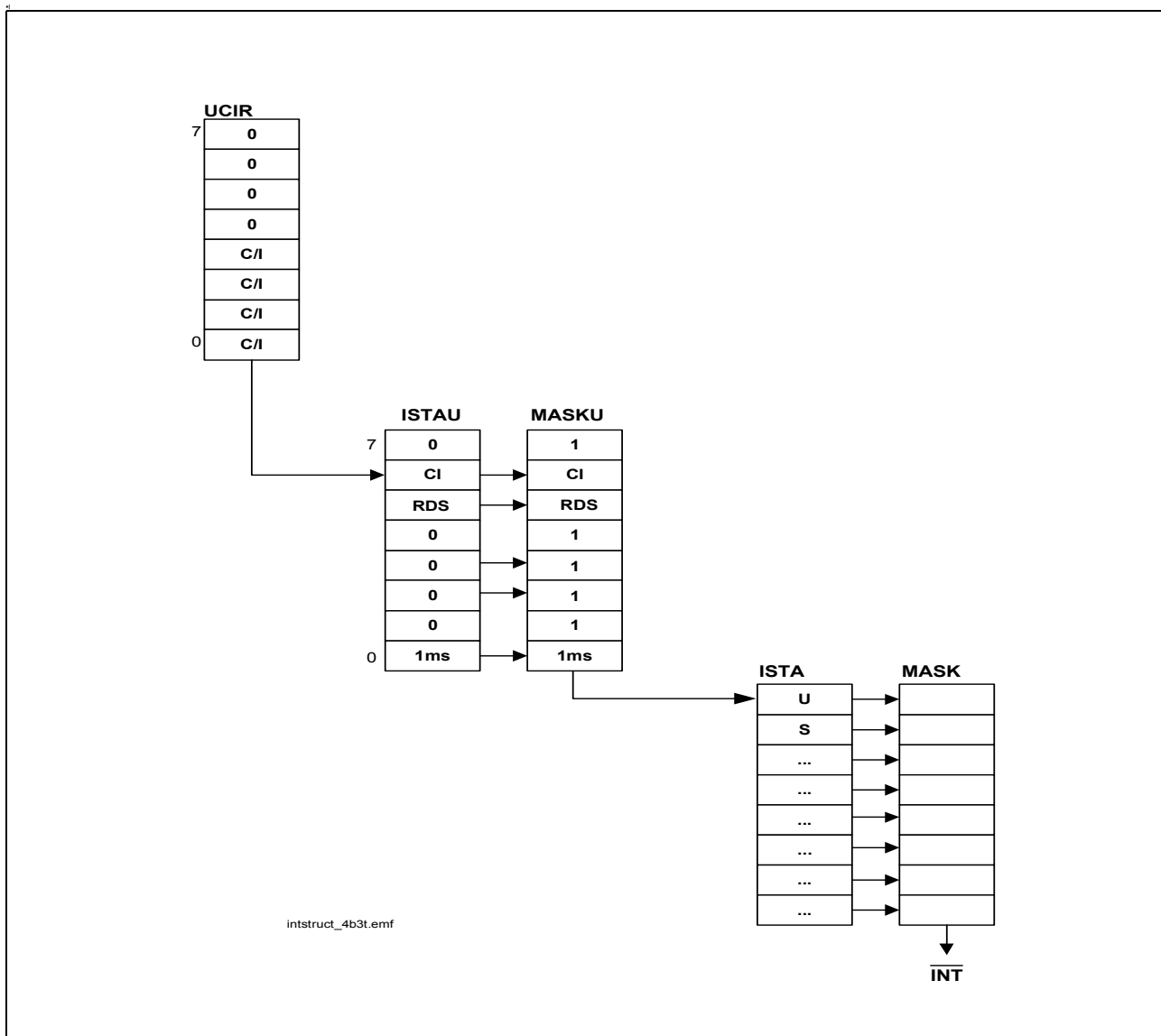
## 2.4.8 U-Transceiver Interrupt Structure

The U-Interrupt Status register (ISTAU) contains the interrupt sources of the U-Transceiver (**Figure 36**). Each source can be masked by setting the corresponding bit of the U-Interrupt Mask register (MASKU) to '1'. Such masked interrupt status bits are not indicated when ISTAU is read and do not generate an interrupt request.

The ISTAU register is cleared on read access. The interrupt sources of the ISTAU register (UCIR, RDS, 1ms) need not be evaluated.

When at time t1 an interrupt source generates an interrupt, all further interrupts are collected. Reading the ISTAU register clears all interrupts set before t1, even if masked. All interrupts, which are flagged after t1 remain active. After the ISTAU read access, the next unmasked interrupt will generate the next interrupt at time t2. After t2 it is possible to reprogram the MASKU register, so that all interrupts, which arrived between t1 and t2 are accessible.

## Functional Description



**Figure 36** Interrupt Structure U-Transceiver

## Functional Description

### 2.5 S-Transceiver

The S-Transceiver offers the NT and LT-S mode state machines described in the User's Manual V3.4 [8].

The S-transceiver lies in IOM<sup>®</sup>-2 channel 1 (default) and is configured and controlled via the registers described in [Chapter 4.5](#). The state machine is set to NT mode (default) but can be set to LT-S mode via register programming.

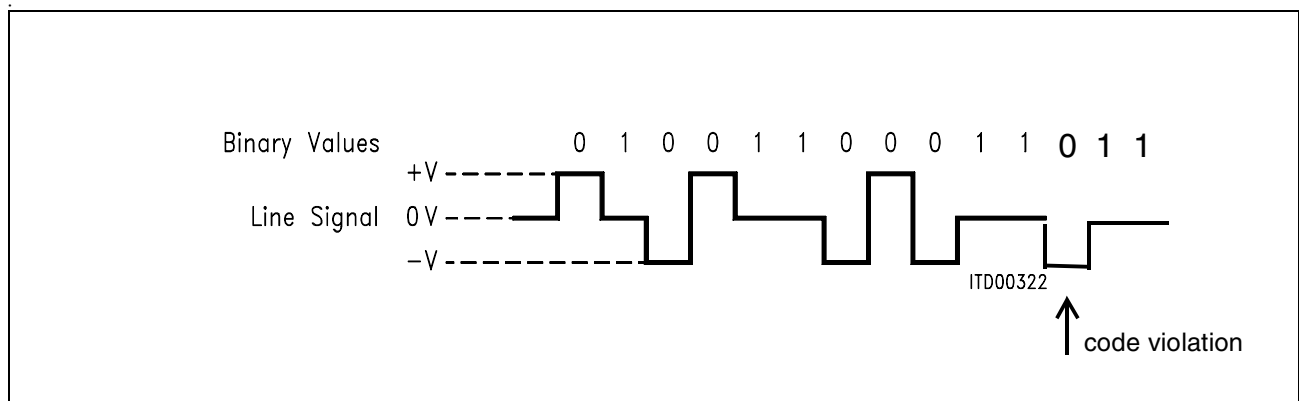
The TE mode (S-transceiver TE mode, U-transceiver disabled) is not supported.

#### 2.5.1 Line Coding, Frame Structure

##### Line Coding

The following figure illustrates the line code. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:

For the required frame structure a code violation is indicated by two consecutive pulses of the same polarity. These two pulses can be adjacent or separated by binary ONES. In bus configurations a binary ZERO always overwrites a binary ONE.



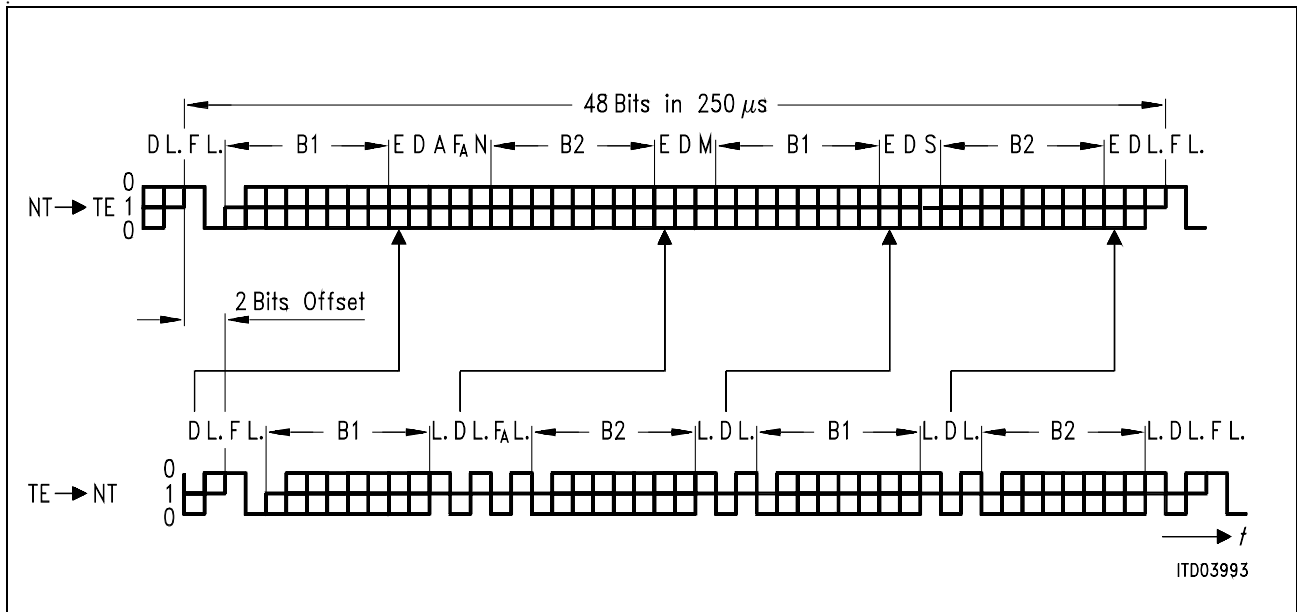
**Figure 37 S/T-Interface Line Code**

##### Frame Structure

Each S/T frame consists of 48 bits at a nominal bit rate of 192 kbit/s. For user data (B1+B2+D) the frame structure applies to a data rate of 144 kbit/s (see [Figure 37](#)).

In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

## Functional Description



**Figure 38** Frame Structure at Reference Points S and T (ITU I.430)

|                  |                       |                                                                                |
|------------------|-----------------------|--------------------------------------------------------------------------------|
| – F              | Framing Bit           | F = (0b) → identifies new frame (always positive pulse, always code violation) |
| – L.             | D.C. Balancing Bit    | L. = (0b) → number of binary ZEROs sent after the last L. bit was odd          |
| – D              | D-Channel Data Bit    | Signaling data specified by user                                               |
| – E              | D-Channel Echo Bit    | E = D → received E-bit is equal to transmitted D-bit                           |
| – F <sub>A</sub> | Auxiliary Framing Bit | See section 6.3 in ITU I.430                                                   |
| – N              |                       | $N = \overline{F_A}$                                                           |
| – B1             | B1-Channel Data Bit   | User data                                                                      |
| – B2             | B2-Channel Data Bit   | User data                                                                      |
| – A              | Activation Bit        | A = (0b) → INFO 2 transmitted<br>A = (1b) → INFO 4 transmitted                 |
| – S              | S-Channel Data Bit    | S <sub>1</sub> channel data (see note below)                                   |
| – M              | Multiframing Bit      | M = (1b) → Start of new multi-frame                                            |

Note: The ITU I.430 standard specifies S1 - S5 for optional use.

## Functional Description

### 2.5.2 S/Q Channels, Multiframe

According to ITU recommendation I.430 a multi-frame provides extra layer-1 capacity in the TE-to-NT direction through the use of an extra channel between the TE and NT (Q-channel). The Q bits are defined to be the bits in the  $F_A$  bit position.

In the NT-to-TE direction the S-channel bits are used for information transmission.

The S- and Q-channels are accessed via  $\mu C$  by reading/writing the SQR or SQX bits in the S/Q channel registers (SQRR, SQXR).

**Table 24** shows the S and Q bit positions within the multi-frame.

**Table 24 S/Q-Bit Position Identification and Multi-Frame Structure**

| Frame Number | NT-to-TE<br>$F_A$ Bit Position | NT-to-TE<br>M Bit | NT-to-TE<br>S Bit | TE-to-NT<br>$F_A$ Bit Position |
|--------------|--------------------------------|-------------------|-------------------|--------------------------------|
| 1            | ONE                            | ONE               | S11               | Q1                             |
| 2            | ZERO                           | ZERO              | S21               | ZERO                           |
| 3            | ZERO                           | ZERO              | S31               | ZERO                           |
| 4            | ZERO                           | ZERO              | S41               | ZERO                           |
| 5            | ZERO                           | ZERO              | S51               | ZERO                           |
| 6            | ONE                            | ZERO              | S12               | Q2                             |
| 7            | ZERO                           | ZERO              | S22               | ZERO                           |
| 8            | ZERO                           | ZERO              | S32               | ZERO                           |
| 9            | ZERO                           | ZERO              | S42               | ZERO                           |
| 10           | ZERO                           | ZERO              | S52               | ZERO                           |
| 11           | ONE                            | ZERO              | S13               | Q3                             |
| 12           | ZERO                           | ZERO              | S23               | ZERO                           |
| 13           | ZERO                           | ZERO              | S33               | ZERO                           |
| 14           | ZERO                           | ZERO              | S43               | ZERO                           |
| 15           | ZERO                           | ZERO              | S53               | ZERO                           |
| 16           | ONE                            | ZERO              | S14               | Q4                             |
| 17           | ZERO                           | ZERO              | S24               | ZERO                           |
| 18           | ZERO                           | ZERO              | S34               | ZERO                           |
| 19           | ZERO                           | ZERO              | S44               | ZERO                           |
| 20           | ZERO                           | ZERO              | S54               | ZERO                           |
| 1            | ONE                            | ONE               | S11               | Q1                             |
| 2            | ZERO                           | ZERO              | S21               | ZERO                           |

The S-transceiver starts multiframeing if SQXR1.MFEN is set.

After multi-frame synchronization has been established in the TE, the Q data will be inserted at the upstream (TE  $\rightarrow$  NT)  $F_A$  bit position by the TE in each 5th S/T frame, the

---

## Functional Description

S data will be inserted at the downstream (NT → TE) S bit position in each 5th S/T frame (see [Table 24](#)). Access to S2-S5-channel is not supported.

### Interrupt Handling for Multi-Framing

To trigger the microcontroller for a multi-frame access an interrupt can be generated once per multi-frame (SQW) or if the received Q-channel have changed (SQC). In both cases the microcontroller has access to the multiframe within the duration of one multiframe (5 ms).

The start of a multiframe can not be synchronized to an external signal.

### 2.5.3 Data Transfer between IOM<sup>®</sup>-2 and S<sub>0</sub>

In the state G3 (Activated) or if the internal layer-1 statemachine is disabled and XINF of register S\_CMD is programmed to '011' the B1, B2 and D bits are transferred transparently from the S/T to the IOM<sup>®</sup>-2 interface and vice versa. In all other states '1's are transmitted to the IOM<sup>®</sup>-2 interface.

Note: In intelligent NT or intelligent LT-S mode the D-channel access can be blocked by the IOM<sup>®</sup>-2 D-channel handler.

### 2.5.4 Loopback 2

C/I commands ARL and AIL close the analog loop as close to the S-interface as possible. ETSI refers to this loop under 'loopback 2'. ETSI requires, that B1, B2 and D channels have the same propagation delay when being looped back.

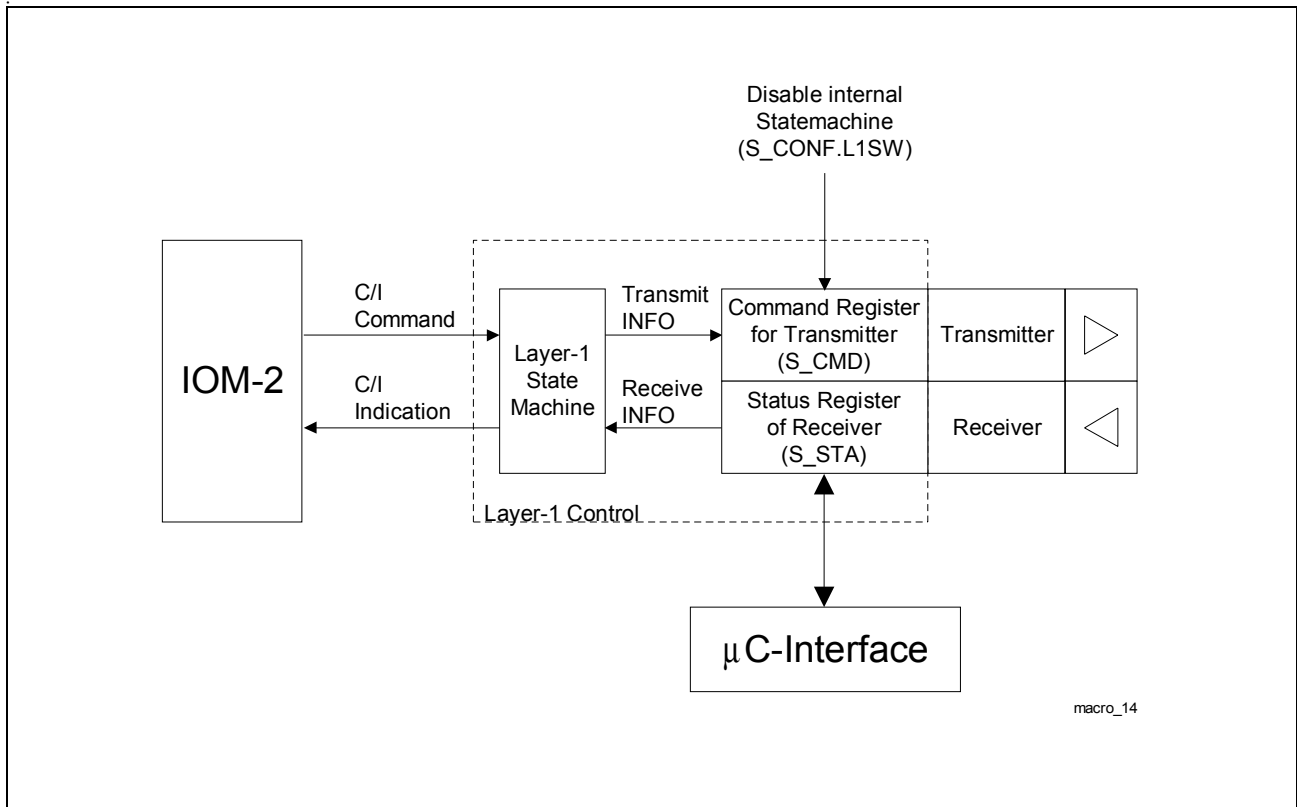
The D-channel Echo bit is set to bin. 0 during an analog loopback (i.e. loopback 2). The loop is transparent.

Note: After C/I-code AIL has been recognized by the S-transceiver, zeros are looped back in the B and D-channels (DU) for four frames.

### 2.5.5 Control of S-Transceiver / State Machine

The S-transceiver activation/ deactivation can be controlled by an internal statemachine via the IOM<sup>®</sup>-2 C/I-channel or by software via the  $\mu$ C interface directly. In the default state the internal layer-1 statemachine of the S-transceiver is used. By setting the L1SW bit in the S\_CONF0 register the internal statemachine can be disabled and the layer-1 transmit commands, which are normally generated by the internal statemachine can be written directly into the S\_CMD register or the received status read out from the S\_STA register, respectively. The S-transceiver layer-1 control flow is shown in [Figure 39](#).

## Functional Description



**Figure 39 S-Transceiver Control**

The state diagram notation is given in [Figure 40](#).

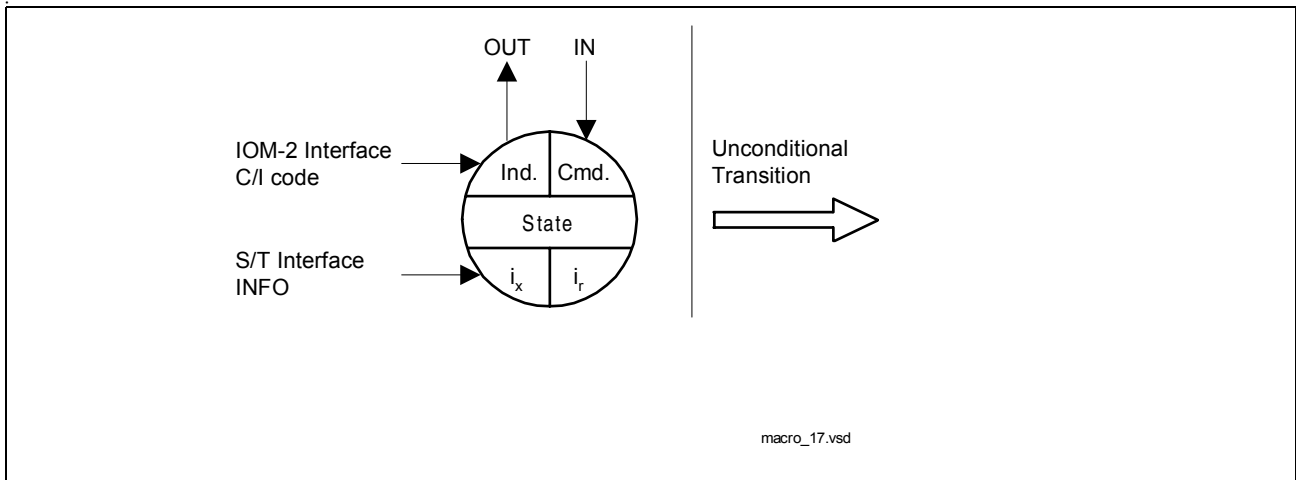
The information contained in the state diagrams are:

- state name
- Signal received from the line interface (INFO)
- Signal transmitted to the line interface (INFO)
- C/I code received (commands)
- C/I code transmitted (indications)
- transition criteria

The transition criteria are grouped into:

- C/I commands
- Signals received from the line interface (INFOs)
- Reset

## Functional Description



**Figure 40 State Diagram Notation**

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “\*” stands for a logical AND combination. And a “+” indicates a logical OR combination.

### Test Signals

- 2 kHz Single Pulses (TM1)  
One pulse with a width of one bit period per frame with alternating polarity.
- 96 kHz Continuous Pulses (TM2)  
Continuous pulses with a pulse width of one bit period.

Note: The test signals TM1 and TM2 are invoked via C/I codes ‘TM1’ and ‘TM2’ according to [Chapter 2.5.5.1](#).

### External Layer-1 Statemachine

Instead of using the integrated layer-1 statemachine it is also possible to implement the layer-1 statemachine completely in software.

The internal layer-1 statemachine can be disabled by setting the L1SW bit in the S\_CONF0 register to ‘1’.

The transmitter is completely under control of the microcontroller via register S\_CMD.

The status of the receiver is stored in register S\_STA and has to be evaluated by the microcontroller. This register is updated continuously. If not masked a RIC interrupt is generated by any change of the register contents. The interrupt is cleared after a read access to this register.

### Reset States

After an active signal on the reset pin  $\overline{\text{RST}}$  the S-transceiver state machine is in the reset state.

## Functional Description

### C/I Codes in Reset State

In the reset state the C/I code 0000 (TIM) is issued. This state is entered either after a hardware reset ( $\overline{\text{RST}}$ ) or with the C/I code RES.

### C/I Codes in Deactivated State

If the S-transceiver is in state 'Deactivated' and receives  $\overline{\text{i0}}$ , the C/I code 0000 (TIM) is issued until expiration of the 8 ms timer. Otherwise, the C/I code 1111 (DI) is issued.

### 2.5.5.1 C/I Codes

The table below presents all defined C/I0 codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in the following sections for commands and indications applicable in various states.

| Code    | LT-S |     | NT  |     |
|---------|------|-----|-----|-----|
|         | Cmd  | Ind | Cmd | Ind |
| 0 0 0 0 | DR   | TIM | DR  | TIM |
| 0 0 0 1 | RES  | –   | RES | –   |
| 0 0 1 0 | TM1  | –   | TM1 | –   |
| 0 0 1 1 | TM2  | –   | TM2 | –   |
| 0 1 0 0 | –    | RSY | RSY | RSY |
| 0 1 0 1 | –    | –   | –   | –   |
| 0 1 1 0 | –    | –   | –   | –   |
| 0 1 1 1 | –    | –   | –   | –   |
| 1 0 0 0 | AR   | AR  | AR  | AR  |
| 1 0 0 1 | –    | –   | –   | –   |
| 1 0 1 0 | ARL  | –   | ARL | –   |
| 1 0 1 1 | –    | CVR | –   | CVR |
| 1 1 0 0 | –    | AI  | AI  | AI  |
| 1 1 0 1 | –    | –   | –   | –   |
| 1 1 1 0 | –    | –   | AIL | –   |
| 1 1 1 1 | DC   | DI  | DC  | DI  |

---

**Functional Description****Receive Infos on S/T**

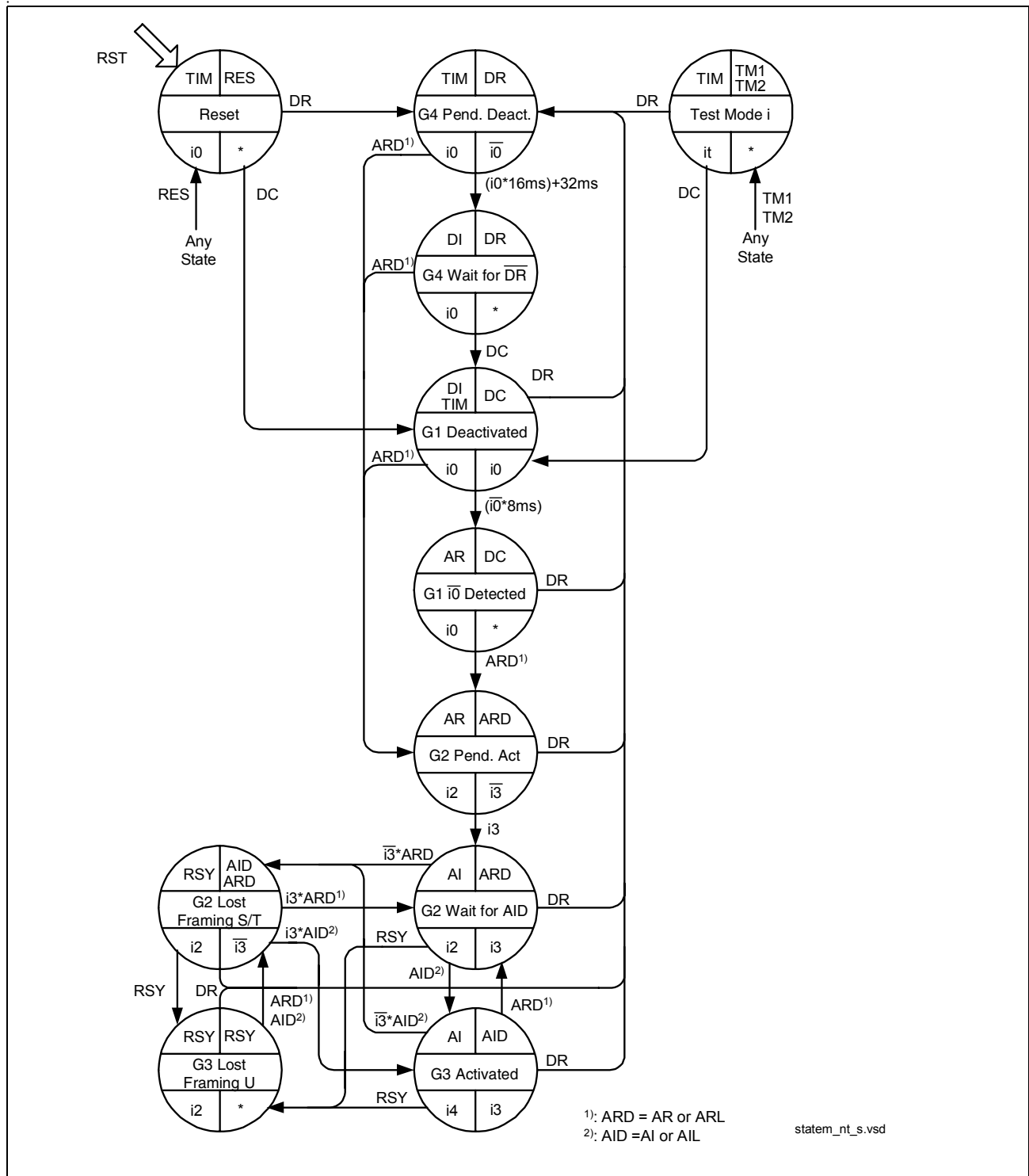
|                 |                                         |
|-----------------|-----------------------------------------|
| I0              | INFO 0 detected                         |
| $\overline{I0}$ | Level detected (signal different to I0) |
| I3              | INFO 3 detected                         |
| $\overline{I3}$ | Any INFO other than INFO 3              |

**Transmit Infos on S/T**

|    |                                                            |
|----|------------------------------------------------------------|
| I0 | INFO 0                                                     |
| I2 | INFO 2                                                     |
| I4 | INFO 4                                                     |
| It | Send Single Pulses (TM1).<br>Send Continuous Pulses (TM2). |

## Functional Description

### 2.5.5.2 State Machine NT Mode



**Figure 41 State Machine NT Mode**

Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself, i.e. C/I-code 'Tmi' must not be followed by C/I-code 'TMj' directly.

---

## Functional Description

### G1 Deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM<sup>®</sup>-2 interface.

### G1 $\overline{\text{IO}}$ Detected

An  $\overline{\text{INFO 0}}$  is detected on the S/T-interface, translated to an "Activation Request" indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream is synchronized.

### G2 Pending Activation

As a result of the ARD command, an INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

### G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a "switch-through" command AID from the device upstream.

### G3 Activated

INFO 4 is sent on the S/T-interface as a result of the "switch through" command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

### G2 Lost Framing S/T

This state is reached when the transceiver has lost synchronism in the state G3 activated.

### G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the transmission line, the S-transceiver transmits INFO 2.

### G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state "G4 wait for DR") is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms

or an internal timer of 32 ms expires.

**Functional Description**
**G4 wait for  $\overline{DR}$** 

Final state after a deactivation request. The S-transceiver remains in this state until DC is issued.

**Unconditional States**
**Test Mode TM1**

Send Single Pulses

**Test Mode TM2**

Send Continuous Pulses

**C/I Commands**

| Command                  | Abbr. | Code | Remark                                                                                                           |
|--------------------------|-------|------|------------------------------------------------------------------------------------------------------------------|
| Deactivation Request     | DR    | 0000 | Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.                                  |
| Reset                    | RES   | 0001 | Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.   |
| Send Single Pulses       | TM1   | 0010 | Send Single Pulses.                                                                                              |
| Send Continuous Pulses   | TM2   | 0011 | Send Continuous Pulses.                                                                                          |
| Receiver not Synchronous | RSY   | 0100 | Receiver is not synchronous                                                                                      |
| Activation Request       | AR    | 1000 | Activation Request. This command is used to start an activation.                                                 |
| Activation Request Loop  | ARL   | 1010 | Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface. |
| Activation Indication    | AI    | 1100 | Activation Indication. Synchronous receiver, i.e. activation completed.                                          |

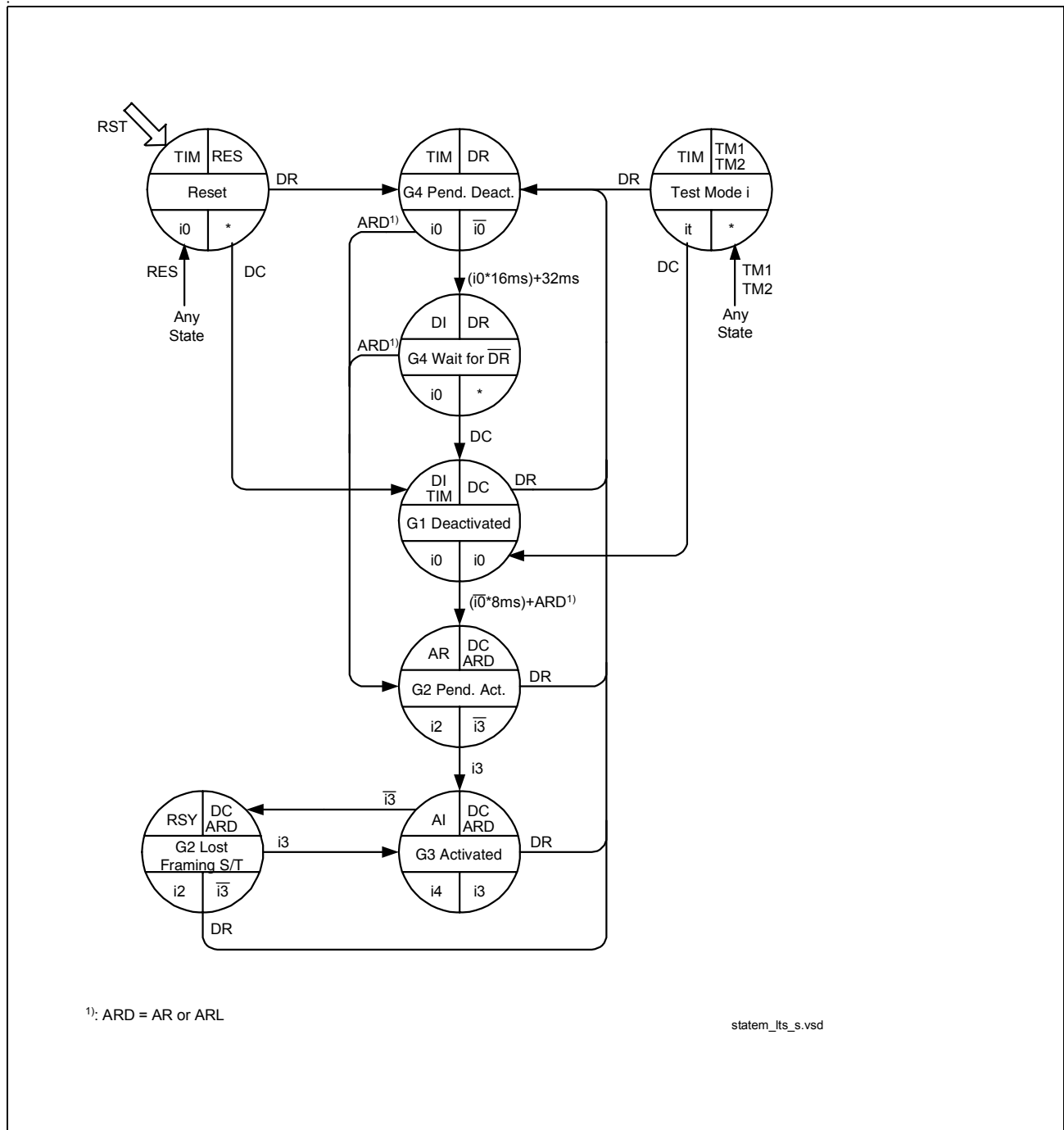
## Functional Description

| Command                    | Abbr. | Code | Remark                                                                                                                                                                         |
|----------------------------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Activation Indication Loop | AIL   | 1110 | Activation Indication Loop                                                                                                                                                     |
| Deactivation Confirmation  | DC    | 1111 | Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO } 0}$ enabled). |

| Indication               | Abbr. | Code | Remark                                                                                                            |
|--------------------------|-------|------|-------------------------------------------------------------------------------------------------------------------|
| Timing                   | TIM   | 0000 | Interim indication during deactivation procedure.                                                                 |
| Receiver not Synchronous | RSY   | 0100 | Receiver is not synchronous.                                                                                      |
| Activation Request       | AR    | 1000 | $\overline{\text{INFO } 0}$ received from terminal. Activation proceeds.                                          |
| Illegal Code Ciolation   | CVR   | 1011 | Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.                               |
| Activation Indication    | AI    | 1100 | Synchronous receiver, i.e. activation completed.                                                                  |
| Deactivation Indication  | DI    | 1111 | Timer (32 ms) expired or $\overline{\text{INFO } 0}$ received for a duration of 16 ms after deactivation request. |

## Functional Description

### 2.5.5.3 State Machine LT-S Mode



**Figure 42 State Machine LT-S Mode**

Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself, i.e. C/I-code 'TMi' must not be followed by C/I-code 'TMj' directly.

---

## Functional Description

### G1 deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM<sup>®</sup>-2 interface.

### G2 pending activation

As a result of an  $\overline{\text{INFO 0}}$  detected on the S/T line or an ARD command, the S-transceiver begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.

### G3 activated

Normal state where INFO 4 is transmitted to the S/T-interface. The transceiver remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver loses synchronism.

When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.

### G2 lost framing

This state is reached when the S-transceiver has lost synchronism in the state G3 activated.

### G4 pending deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state "G4 wait for DR.") is issued by the S-transceiver when:

either INFO0 is received for a duration of 16 ms,  
or an internal timer of 32 ms expires.

### G4 wait for $\overline{\text{DR}}$

Final state after a deactivation request. The transceiver remains in this state until DC is issued.

## Unconditional States

### Test mode - TM1

Single alternating pulses are sent on the S/T-interface.

**Functional Description**
**Test mode - TM2**

Continuous alternating pulses are sent on the S/T-interface.

| <b>Command</b>            | <b>Abbr.</b> | <b>Code</b> | <b>Remark</b>                                                                                                                                                    |
|---------------------------|--------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Deactivation Request      | DR           | 0000        | DR - Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.                                                                             |
| Reset                     | RES          | 0001        | Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.                                                   |
| Send Single Pulses        | TM1          | 0010        | Send Single Pulses.                                                                                                                                              |
| Send Continuous Pulses    | TM2          | 0011        | Send Continuous Pulses.                                                                                                                                          |
| Activation Request        | AR           | 1000        | Activation Request. This command is used to start an activation.                                                                                                 |
| Activation Request Loop   | ARL          | 1010        | Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface.                                                 |
| Deactivation Confirmation | DC           | 1111        | Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of <u>INFO 0</u> enabled). |

| <b>Indication</b>        | <b>Abbr.</b> | <b>Code</b> | <b>Remark</b>                                                                               |
|--------------------------|--------------|-------------|---------------------------------------------------------------------------------------------|
| Timing                   | TIM          | 0000        | Interim indication during activation procedure in G1.                                       |
| Receiver not Synchronous | RSY          | 0100        | Receiver is not synchronous                                                                 |
| Activation Request       | AR           | 1000        | <u>INFO 0</u> received from terminal. Activation proceeds.                                  |
| Illegal Code Ciolation   | CVR          | 1011        | Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.         |
| Activation Indication    | AI           | 1100        | Synchronous receiver, i.e. activation completed.                                            |
| Deactivation Indication  | DI           | 1111        | Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request |

### 2.5.6 S-Transceiver Enable / Disable

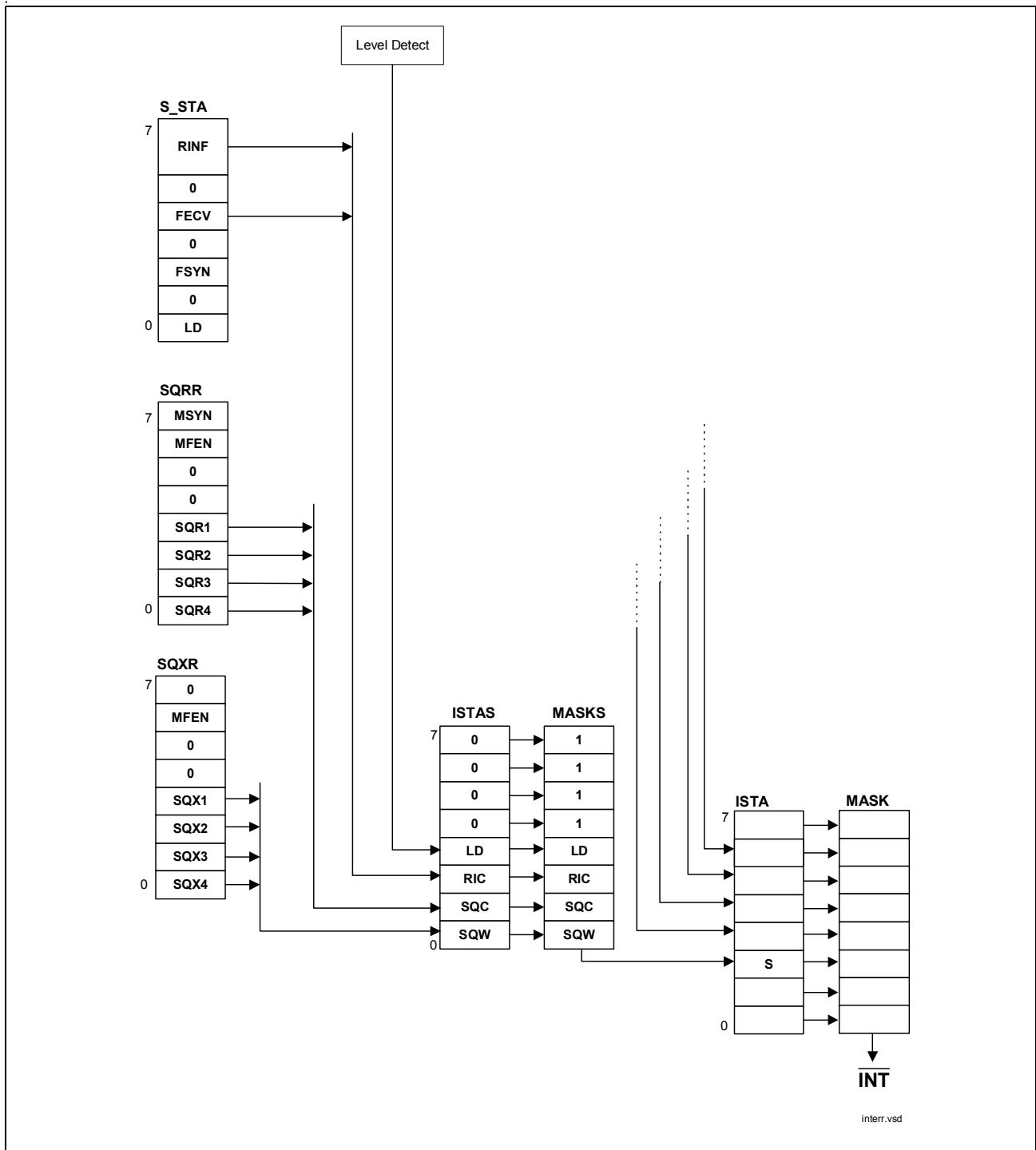
The layer-1 part of the S-transceiver can be enabled/disabled with the two bits S\_CONF0.DIS\_TR and S\_CONF2.DIS\_TX.

If DIS\_TX='1' the transmit buffers are disabled. The receiver will monitor for incoming data in this configuration. By default the transmitter is disabled (DIS\_TX = '1').

If the transceiver is disabled (DIS\_TR = '1', DIS\_TX = don't care) all layer-1 functions are disabled including the level detection circuit of the receiver. In this case the power consumption of the S-transceiver is reduced to a minimum.

## Functional Description

### 2.5.7 Interrupt Structure S-Transceiver



**Figure 43** Interrupt Structure S-Transceiver

### 3 Operational Description

#### 3.1 Layer 1 Activation/Deactivation

##### 3.1.1 Generation of 4B3T Signal Elements

For control and monitoring purposes of the activation/deactivation progress the following signal elements are defined by TS 102 080 and FTZ 1 TR 220.

**Table 25 4B3T Signal Elements**

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U0       | No signal or deactivation signal that is used in both directions.<br>Downstream, it requests the NT to deactivate. Upstream, the NT acknowledges by U0 that it is deactivated.                                                                                                                                                                                                                                                                                                                          |
| U1W, U2W | Awake or awake acknowledge signal used in the awake procedure of the U-interface.                                                                                                                                                                                                                                                                                                                                                                                                                       |
| U2       | The LT sends U2 to enable the own echo canceller to adapt the coefficients. By the Barker code the NT at the other end is enabled to synchronize. The detection of U2 is used by the NT as a criterion for synchronization.<br>The M-channel on U may be used to transfer loop commands.                                                                                                                                                                                                                |
| U2A      | While the NT-RP is synchronizing on the received signal, the LT-RP sends out U2A to enable its echo canceller to adapt the coefficients, but sending no Barker code it inhibits the NT to synchronize on the still asynchronous signal.<br>Due to proceeding synchronization, the U-frame may jump from time to time. U2A can not be detected in the NT at the far end.                                                                                                                                 |
| U1A      | U1A is similar to U1 but without framing information. While the NT synchronizes on the received signal, it sends out U1A to enable its echo canceller to adapt its coefficients, but sends no Barker code to prevent the LT from synchronizing on the still asynchronous signal. Due to proceeding synchronization, the U-frame may jump from time to time. U1A can not be detected by the far-end LT.                                                                                                  |
| U1       | When synchronized, the NT sends the Barker code and the LT may synchronize itself. U1 indicates additionally that a terminal equipment has not yet activated. Upon receiving U1 the LT indicates the synchronized state by C/I 'UAI' to layer-2.<br>Usually during activation, no U1 signal is detected in the LT because the TE is activated first and U1 changes to U3 before being detected.<br><br>The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data. |

## Operational Description

**Table 25 4B3T Signal Elements (cont'd)**

|     |                                                                                                                                                                                                                                                                                         |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U3  | <p>U3 indicates that the whole link to the TE is synchronous in both directions. On detecting U3 the LT requests the NT by U4H to establish a fully transparent connection.</p> <p>The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.</p> |
| U4H | <p>U4H requires the NT to go to the 'Transparent' state. On detecting U4H the NT stops sending signal U3 and informs the S-transceiver or a layer-2 device via the system interface.</p> <p>The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.</p> |
| U4  | U4 transports operational data on B and D channels. The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.                                                                                                                                             |
| U5  | U5 transports operational data on B and D channels. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.                                                                                                                                    |
| SP  | The T-SMINTI sends periodically single pulses once per millisecond on the U-interface. The test mode can be used for pulse mask measurements.                                                                                                                                           |
| LOF | Loss of frame, generated by flywheel                                                                                                                                                                                                                                                    |

**Table 26 Generation of the 4B3T Signal Elements**

| Upstream<br>(NT to LT) | Downstream<br>(LT to NT) |                                                                                                                                                                    | symbols<br>(ternary)                                | sync<br>word<br>(ternary) | M<br>sym<br>bol<br>(ternary) | binary<br>data<br>before<br>scrambling |
|------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------------|------------------------------|----------------------------------------|
| U1W                    | U2W                      | Resulting in a tone of:<br>Frequency: 7.5 kHz<br>Duration: 2.13 ms<br>when sending the<br>wakeup tone is finished,<br>signal AWT is set and<br>ternary "0" is sent | 16 times +<br>+ + + + +<br>+ + - - - -<br>- - - - - | n/a                       | n/a                          | n/a                                    |
| U1A                    | U2A                      | scrambled binary data                                                                                                                                              |                                                     | 0                         | 0                            | 0                                      |
| U1                     | U2                       | scrambled binary data                                                                                                                                              |                                                     | yes                       | yes                          | 0                                      |
| U3                     |                          | scrambled binary data                                                                                                                                              |                                                     | yes                       | yes                          | 1                                      |

## Operational Description

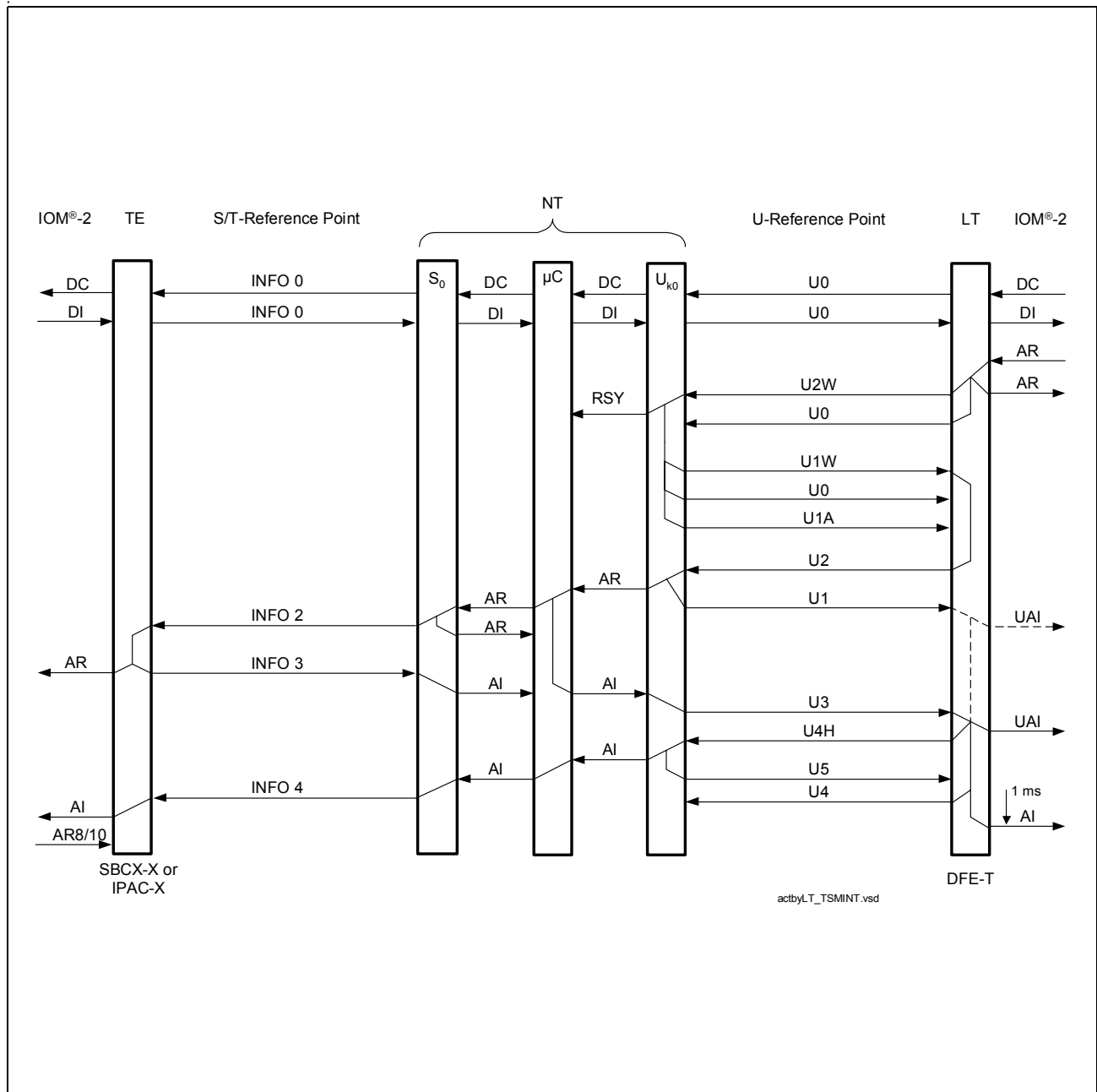
**Table 26 Generation of the 4B3T Signal Elements (cont'd)**

|    |     |                                                |                                               |     |     |     |
|----|-----|------------------------------------------------|-----------------------------------------------|-----|-----|-----|
|    | U4H | Duration: 1 ms<br>(warranted by state machine) |                                               | yes | yes | 1   |
| U5 | U4  | Binary data from the digital interface         |                                               | yes | yes | BBD |
| U0 | U0  | Ternary continuous "0"                         | 0                                             | 0   | 0   | n/a |
| SP | SP  | single pulses                                  | once "+",<br>119 times<br>"0"<br>(repeatedly) | n/a | n/a | n/a |

**Table 27 S/T-Interface Signals**

| Signals from NT to TE |                                                                                                                                                       | Signals from TE to NT |                                                                                            |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--------------------------------------------------------------------------------------------|
| INFO 0                | No signal.                                                                                                                                            | INFO 0                | No signal.                                                                                 |
|                       |                                                                                                                                                       | INFO 1                | A continuous signal with the following pattern:<br>Positive ZERO, negative ZERO, six ONES. |
| INFO 2                | Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules. |                       |                                                                                            |
|                       |                                                                                                                                                       | INFO 3                | Synchronized frames with operational data on B and D-channels.                             |
| INFO 4                | Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.                                                                   |                       |                                                                                            |

### 3.1.2 Complete Activation Initiated by Exchange

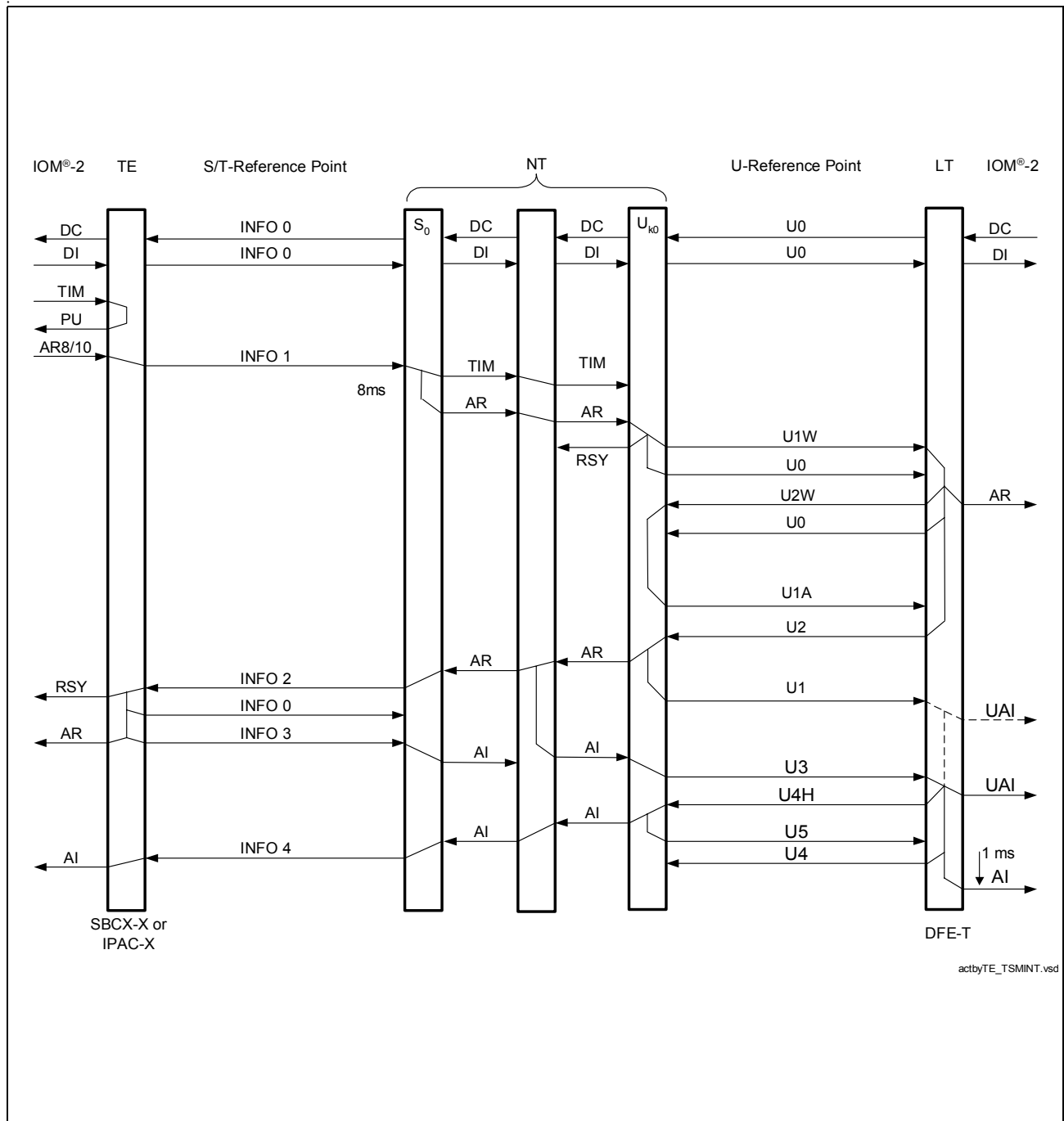


**Figure 44 Activation Initiated by Exchange**

Note: The LT starts issuing signal U2 before the NT starts issuing U1A. This chronological order is not displayed for clarification.

## Operational Description

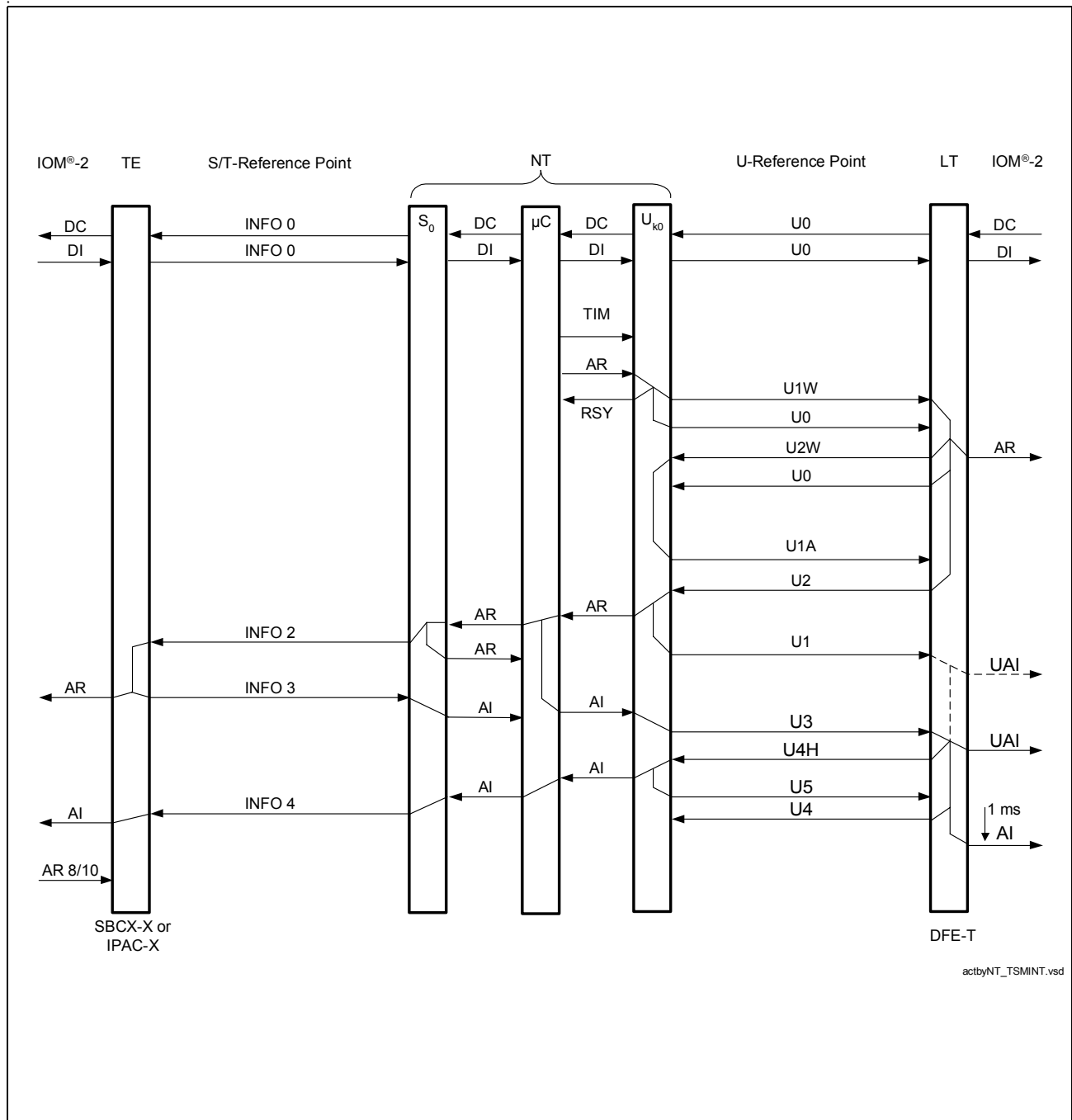
### 3.1.3 Complete Activation Initiated by TE



**Figure 45 Activation Initiated by TE**

Note: The LT starts issuing signal U2 before the NT starts issuing U1A. This chronological order is not displayed for clarification.

### 3.1.4 Complete Activation Initiated by NT

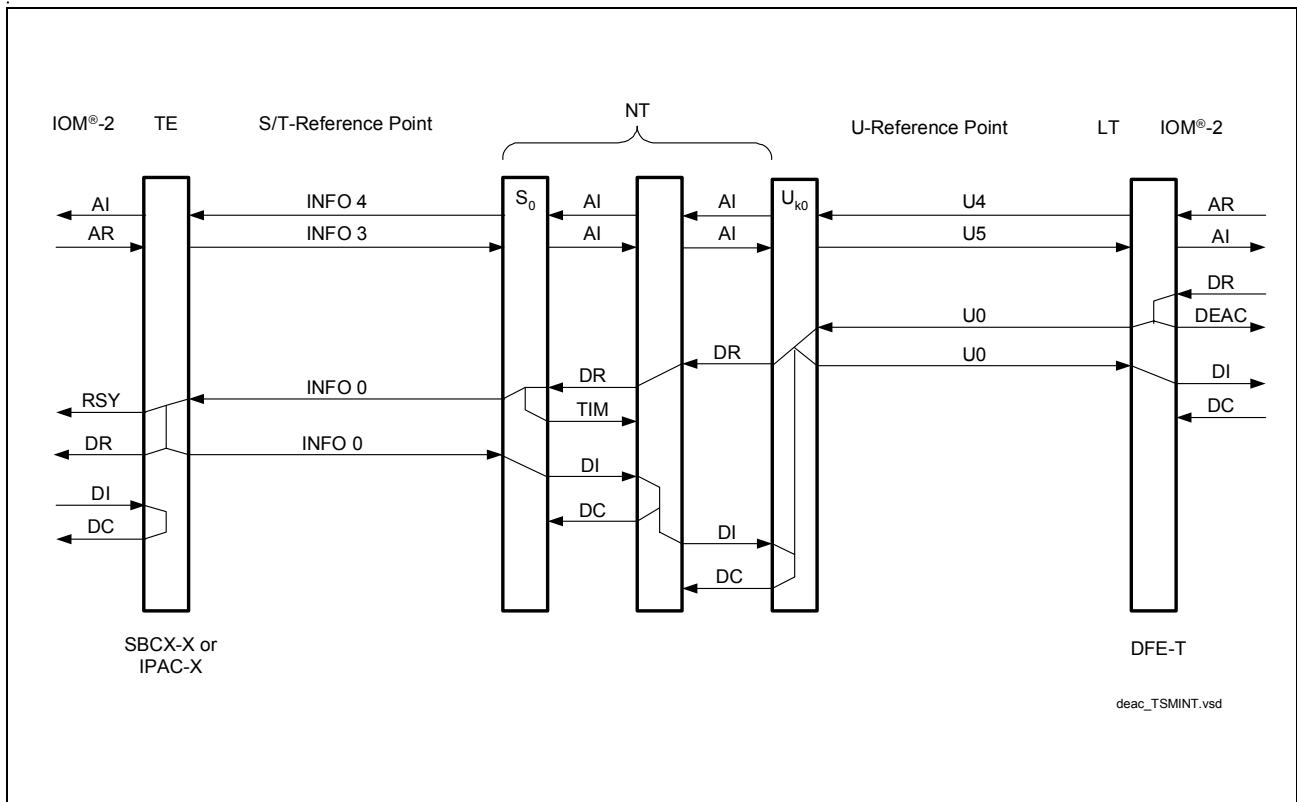


**Figure 46 Activation Initiated by NT**

Note: The LT starts issuing signal U2 before the NT starts issuing U1A. This chronological order is not displayed for clarification.

## Operational Description

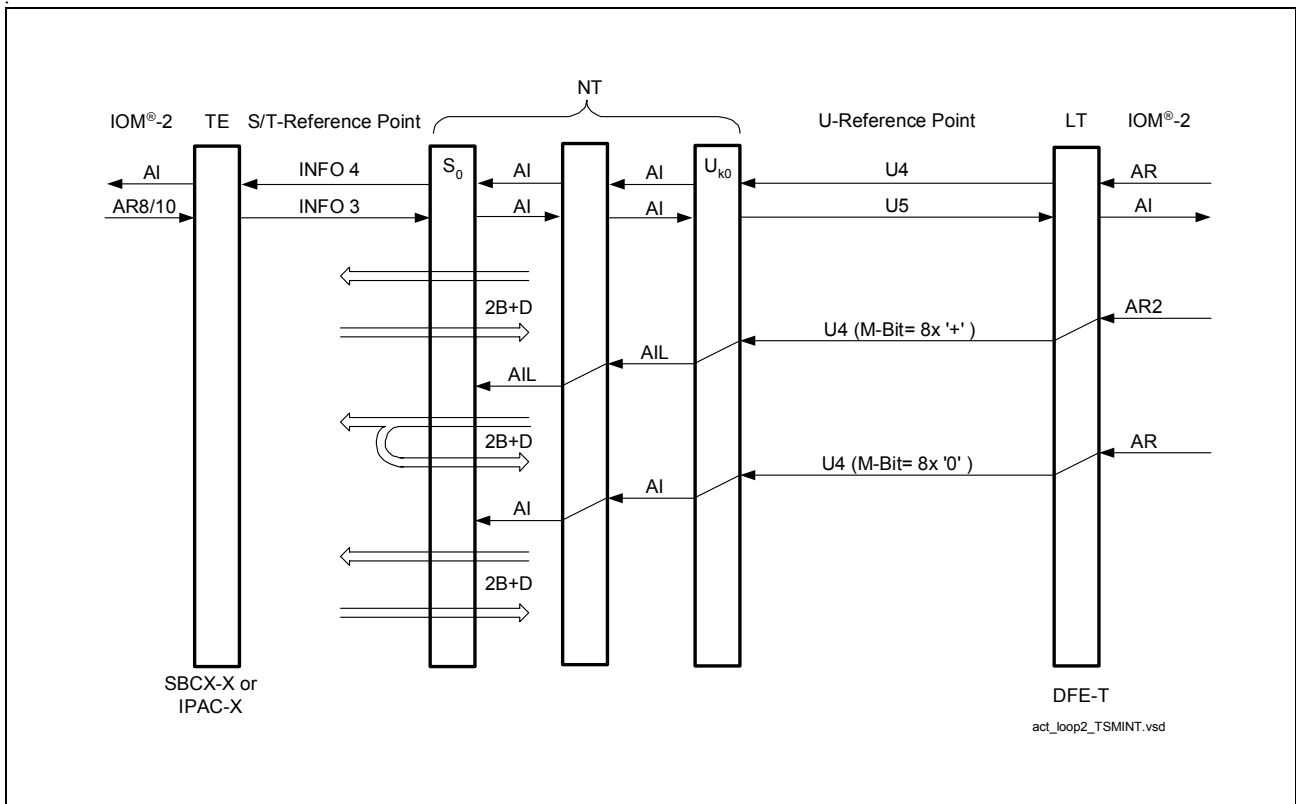
### 3.1.5 Complete Deactivation



**Figure 47 Complete Deactivation**

## Operational Description

### 3.1.6 Loop 2



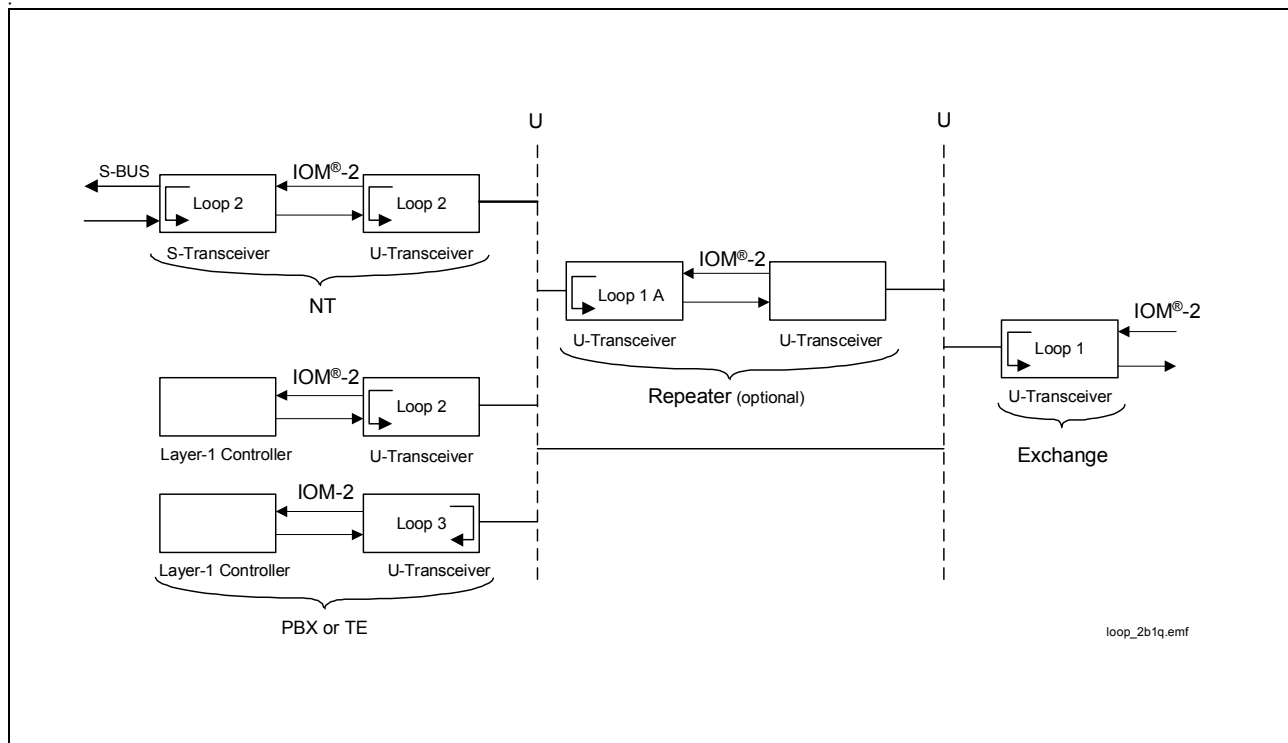
**Figure 48 Loop 2**

Note: Closing/resolving loop 2 may provoke the S-transceiver to resynchronize. In this case, the following C/I-codes are exchanged immediately on reception of AIL/AI, respectively: DU: 'RSY', DU: 'AI', DD: 'AIL'/'AI'.

## Operational Description

### 3.2 Layer 1 Loopbacks

Test loopbacks are specified by the national PTTs in order to facilitate the location of defect systems. Four different loopbacks are defined. The position of each loopback is illustrated in **Figure 49**.



**Figure 49 Test Loopbacks**

Loopbacks #1, #1A and #2 are controlled by the exchange. Loopback #3 is controlled locally on the remote side. All four loopback types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner. Only the data looped back internally is processed; signals on the receive pins are ignored. The propagation delay of actually looped B and D channels data must be identical in all loopbacks.

Besides the remote controlled loopback stimulation via the M channel, the T-SMINT®I features also direct loopback control via its register set.

#### 3.2.1 Analog Loop-Back S-Transceiver

The T-SMINT®I provides test and diagnostic functions for the S/T interface:

The **internal local loop** (internal Loop A) is activated by a C/I command ARL or by setting the bit LP\_A (Loop Analog) in the S\_CMD register if the layer-1 statemachine is disabled.

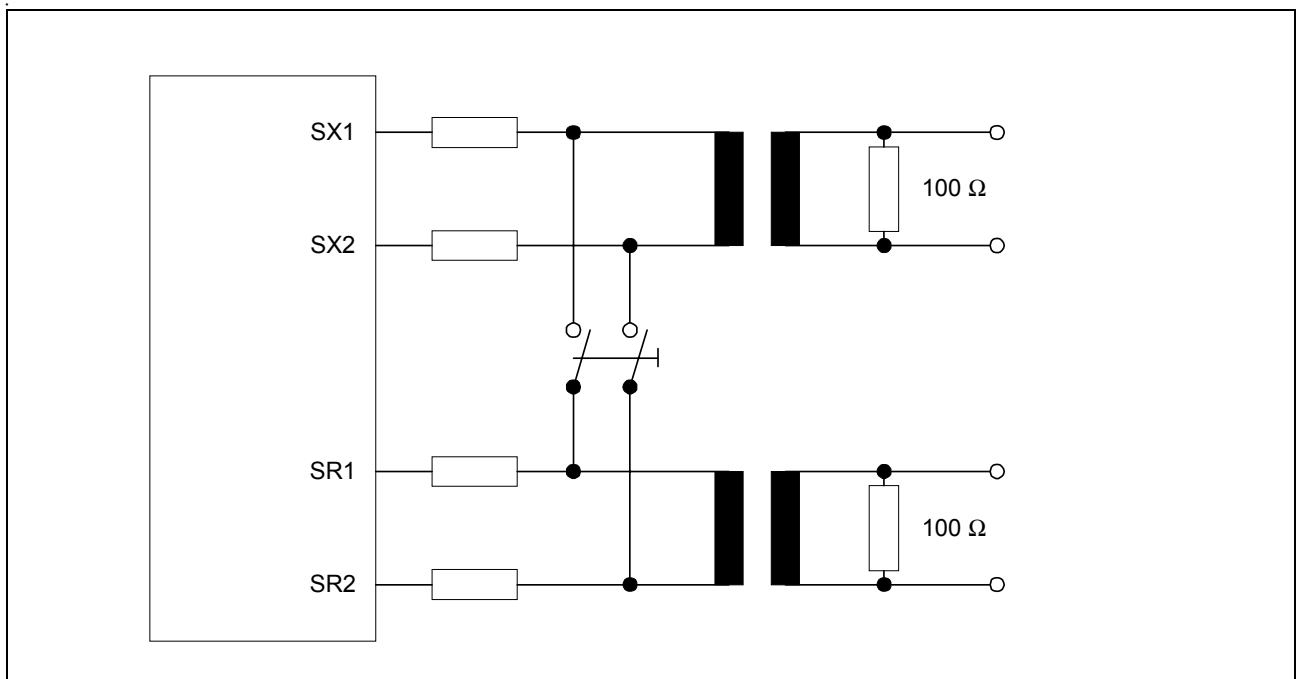
The transmit data of the transmitter is looped back internally to the receiver. The data of the IOM®-2 input B- and D-channels are looped back to the output B- and D-channels.

## Operational Description

The S/T interface level detector is enabled, i.e. if a level is detected this will be reported by the Resynchronization Indication (RSY) but the loop function is not affected. Depending on the DIS\_TX bit in the S\_CONF2 register the internal local loop can be transparent or non transparent to the S/T line.

The **external local loop (external Loop A)** is activated in the same way as the internal local loop described above. Additionally the EXLP bit in the S\_CONF0 register has to be programmed and the loop has to be closed externally as described in [Figure 50](#).

The S/T interface level detector is disabled.



**Figure 50 External Loop at the S/T-Interface**

### 3.2.2 Loopback No.2

For loopback #2 several alternatives exist. Both the type of loopback and the location may vary. The following loopback types belong to the loopback-#2 category:

- complete loopback (B1,B2,D), in the U-transceiver
- complete loopback (B1,B2,D), in a downstream device
- B1-channel loopback, always performed in the U-transceiver
- B2-channel loopback, always performed in the U-transceiver

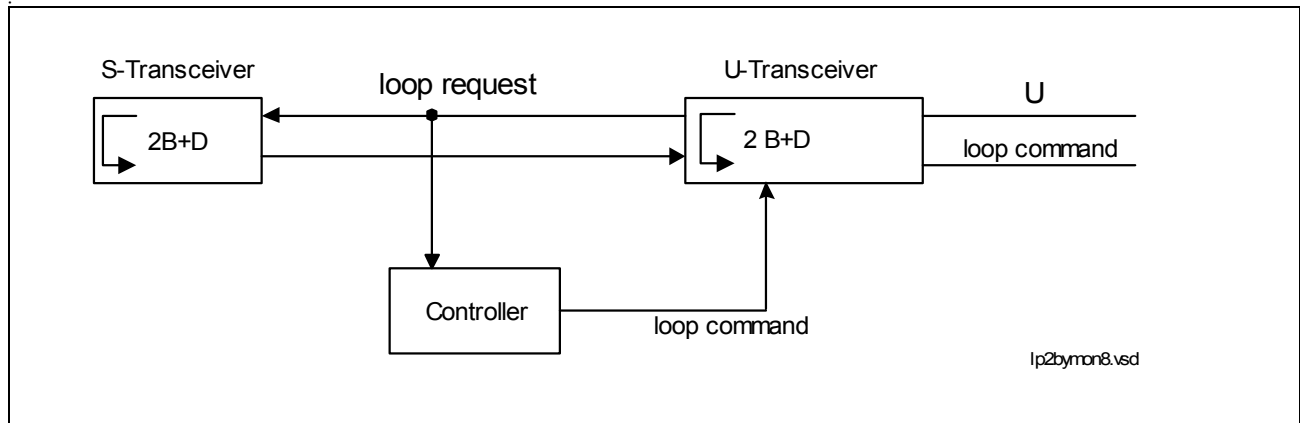
All loop variations performed by the U-transceiver are closed as near to the internal IOM<sup>®</sup>-2 interface as possible.

Normally loopback #2 is controlled by the exchange. The maintenance channel is used for this purpose.

## Operational Description

### 3.2.2.1 Complete Loopback

When receiving the request for a complete loopback, the U transceiver passes it on to the downstream device, e.g. the S-bus transceiver. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”



**Figure 51 Complete Loopback Options in NT-Mode**

The complete loopback is either opened under control of the exchange via the maintenance channel or locally controlled via the  $\mu$ C. No reset is required for loopback #2. The line stays active and is ready for data transmission.

### 3.2.2.2 Loopback No.2 - Single Channel Loopbacks

Single channel loopbacks are always performed directly in the U-Transceiver. No difference between the B1-channel and the B2-channel loopback control procedure exists.

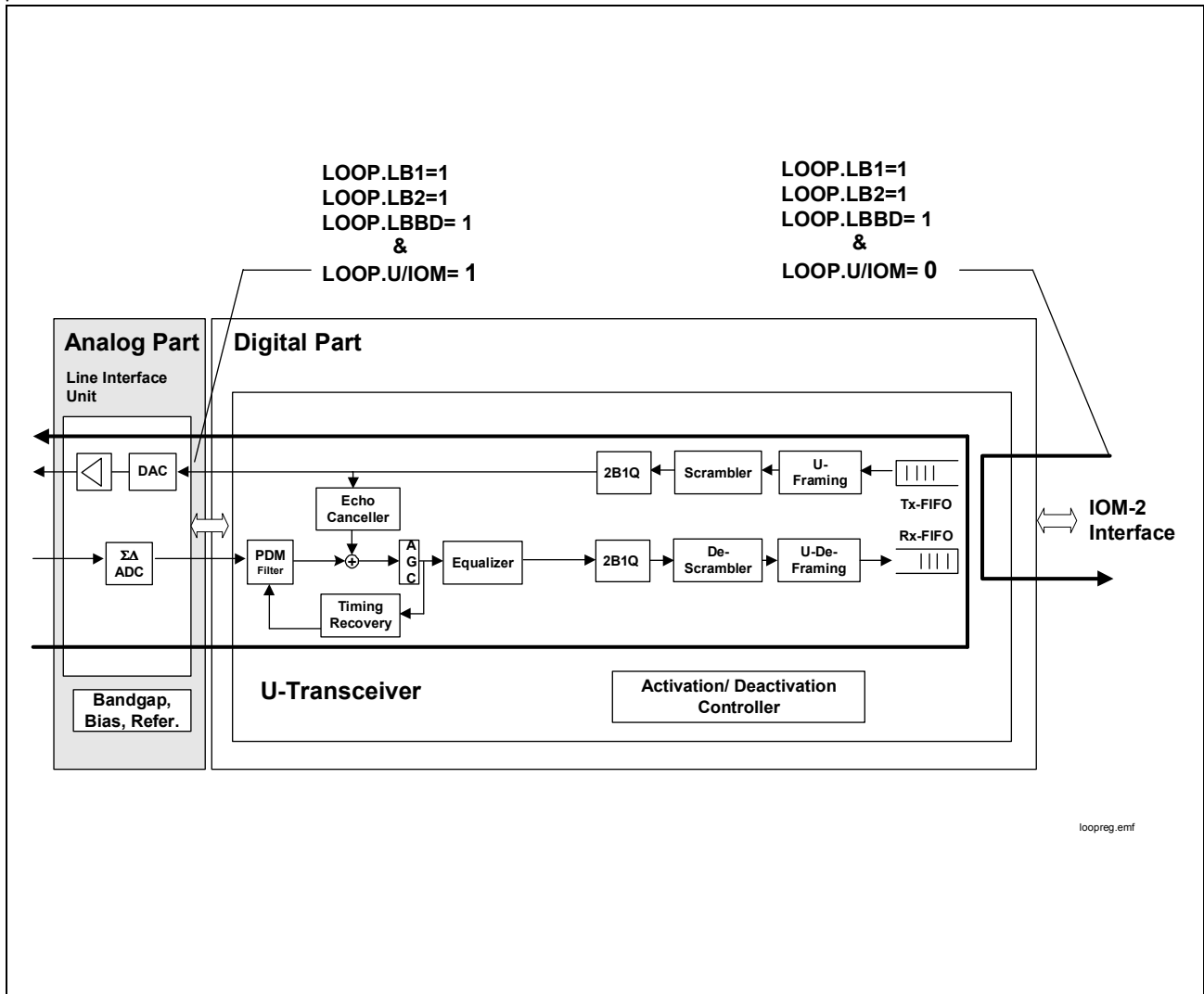
### 3.2.3 Local Loopbacks Featured By the LOOP Register

Besides the standardized remote loopbacks the U-transceiver features additional local loopbacks for enhanced test and debugging facilities. The local loopbacks that are featured by register LOOP are shown in [Figure 52](#). They are closed in the U-transceiver itself and can be activated regardless of the current operational status.

By the LOOP register it can be configured whether the loopback is closed only for the B1 and/or B2 or for 2B+D channels and whether the loopback is closed towards the internal IOM<sup>®</sup>-2 interface or towards the U-Interface.

By default the loopbacks are set to transparent mode. In transparent mode the data is both passed on and looped back. In non-transparent mode the data is not forwarded but substituted by 1s (idle code).

## Operational Description

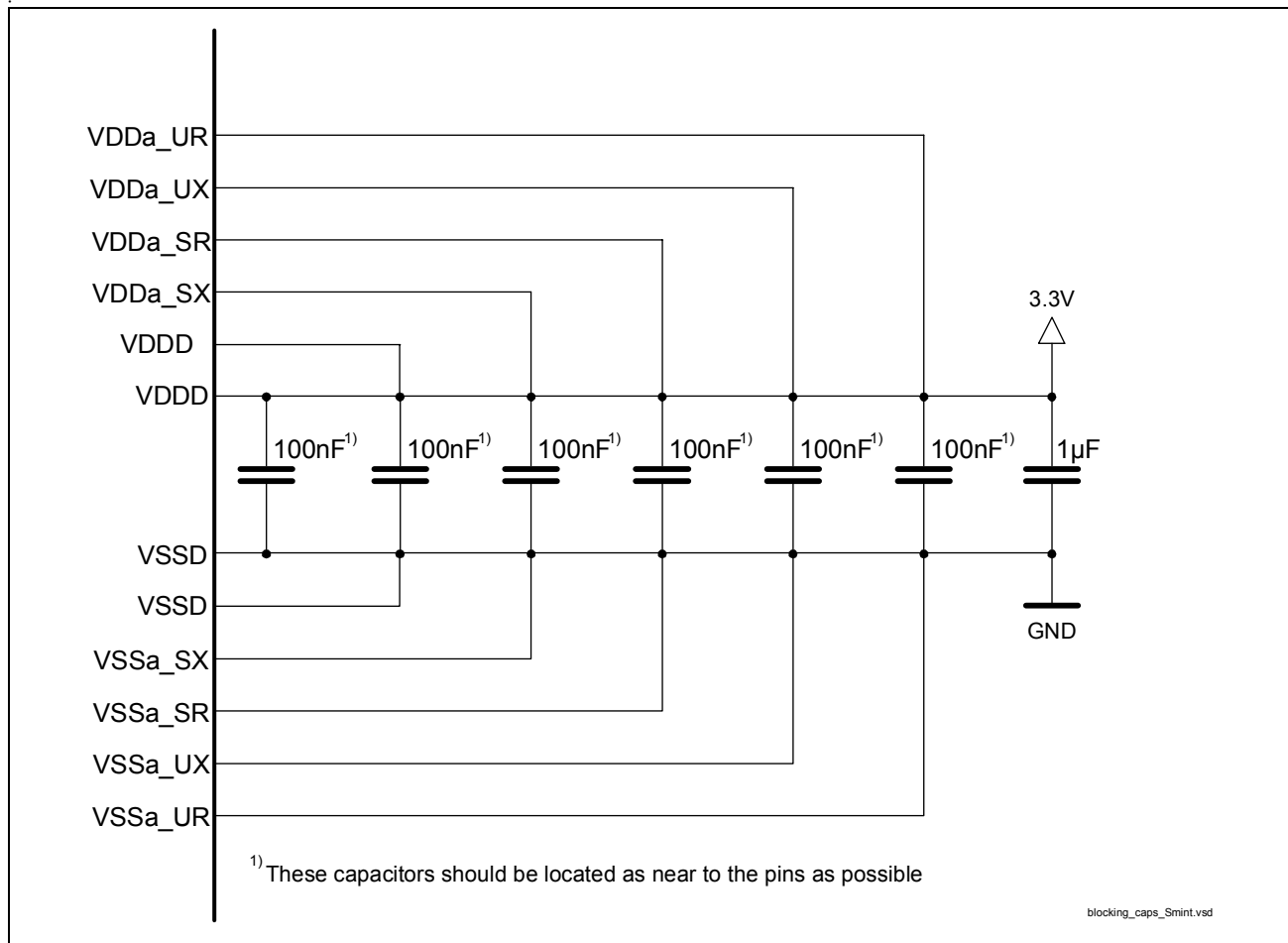


**Figure 52 Loopbacks Featured by Register LOOP**

### 3.3 External Circuitry

#### 3.3.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

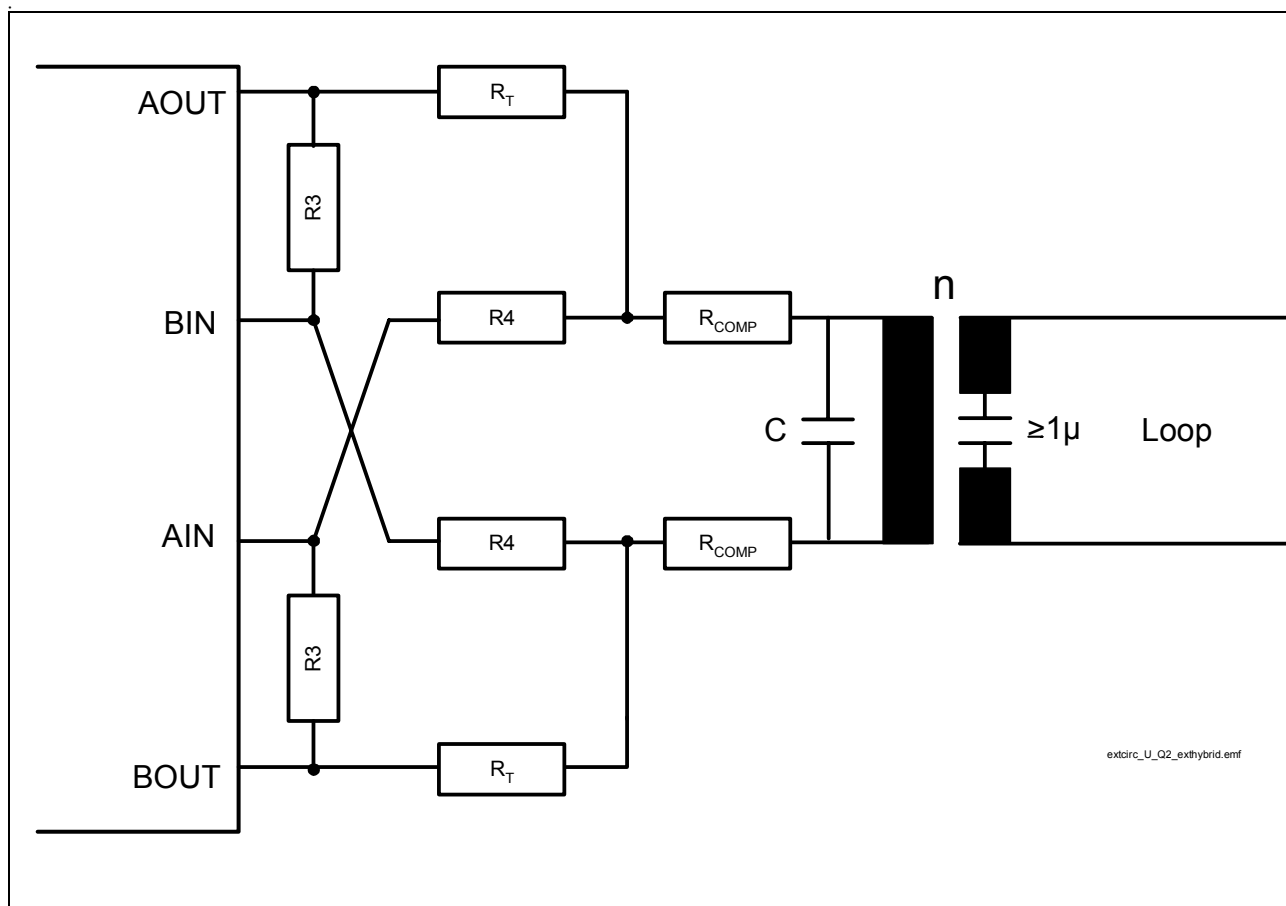


**Figure 53 Power Supply Blocking**

#### 3.3.2 U-Transceiver

The T-SMINTI is connected to the twisted pair via a transformer. [Figure 54](#) shows the recommended external circuitry with external hybrid. The recommended protection circuitry is not displayed.

## Operational Description



**Figure 54 External Circuity U-Transceiver with External Hybrid**

### U-Transformer Parameters

The following table lists parameters of typical U-transformers.

**Table 28 U-Transformer Parameters**

| U-Transformer Parameters                                                                       | Symbol | Value   | Unit     |
|------------------------------------------------------------------------------------------------|--------|---------|----------|
| U-Transformer ratio;<br>Device side : Line side                                                | n      | 1 : 1.6 |          |
| Main inductanc of windings on the line side                                                    | $L_H$  | 7.5     | mH       |
| Leakage inductance of windings on the line side                                                | $L_S$  | 120     | $\mu$ H  |
| Coupling capacitance between the windings on the device side and the windings on the line side | $C_K$  | 30      | pF       |
| DC resistance of the windings on device side                                                   | $R_B$  | 0.9     | $\Omega$ |
| DC resistance of the windings on line side                                                     | $R_L$  | 1.8     | $\Omega$ |

## Operational Description

### Resistors of the External Hybrid R3, R4 and R<sub>T</sub>

$$R_3 = 1.75 \text{ k}\Omega$$

$$R_4 = 1.0 \text{ k}\Omega$$

$$R_T = 25 \text{ }\Omega$$

### Resistors R<sub>COMP</sub> / R<sub>T</sub>

- Optional use of trafos with non negligible resistance R<sub>B</sub>, R<sub>L</sub> requires compensation resistors R<sub>COMP</sub> depending on R<sub>B</sub> and R<sub>L</sub>:

$$n^2 \times (2R_{\text{COMP}} + R_B) + R_L = 20\Omega \quad (1)$$

- Compliance with Return Loss Measurements:

$$n^2 \times (2R_{\text{COMP}} + 2R_T + R_{\text{out}} + R_B) + R_L = 150\Omega \quad (2)$$

R<sub>B</sub>, R<sub>L</sub> : see [Table 28](#)

R<sub>OUT</sub> : see [Table 35](#)

### 15nF Capacitor

To achieve optimum performance the 15nF capacitor should be MKT. A Ceramic capacitor is not recommended.

### Tolerances

- Rs: 1%
- C = 15nF: 10-20%
- L<sub>H</sub> = 7.5mH: 10%

### 3.3.3 S-Transceiver

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

## Operational Description

### S-Transformer Parameters

The following **Table 29** lists parameters of a typical S-transformer:

**Table 29 S-Transformer Parameters**

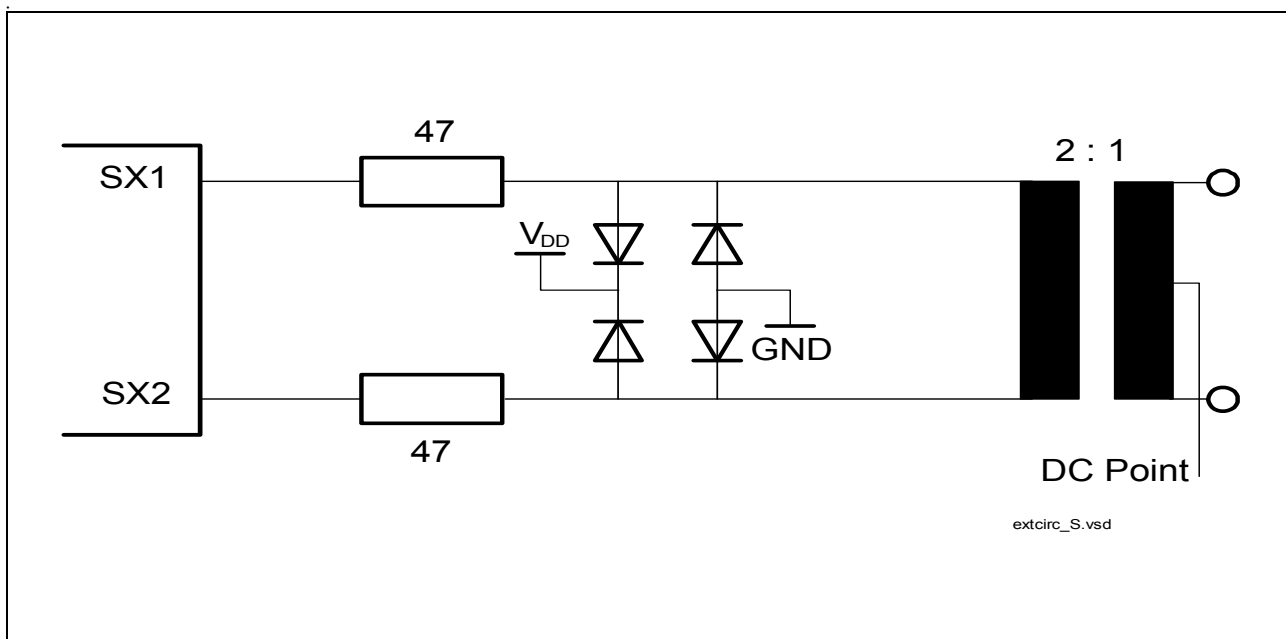
| Transformer Parameters                                                                         | Symbol | Value     | Unit     |
|------------------------------------------------------------------------------------------------|--------|-----------|----------|
| Transformer ratio;<br>Device side : Line side                                                  | n      | 2 : 1     |          |
| Main inductance of windings on the line side                                                   | $L_H$  | typ. 30   | mH       |
| Leakage inductance of windings on the line side                                                | $L_S$  | typ. <3   | $\mu$ H  |
| Coupling capacitance between the windings on the device side and the windings on the line side | $C_K$  | typ. <100 | pF       |
| DC resistance of the windings on device side                                                   | $R_B$  | typ. 2.4  | $\Omega$ |
| DC resistance of the windings on line side                                                     | $R_L$  | typ. 1.4  | $\Omega$ |

### Transmitter

The **transmitter** requires external resistors  $R_{stx} = 47\Omega$  in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode "TM1") on the one hand and in order to meet the output impedance of minimum 20  $\Omega$  on the other hand (to be tested with the testmode 'Continuous Pulses') on the other hand.

Note: The resistance of the S-transformer must be taken into account when dimensioning the external resistors  $R_{stx}$ . If the transmit path contains additional components (e.g. a choke), then the resistance of these additional components must be taken into account, too.

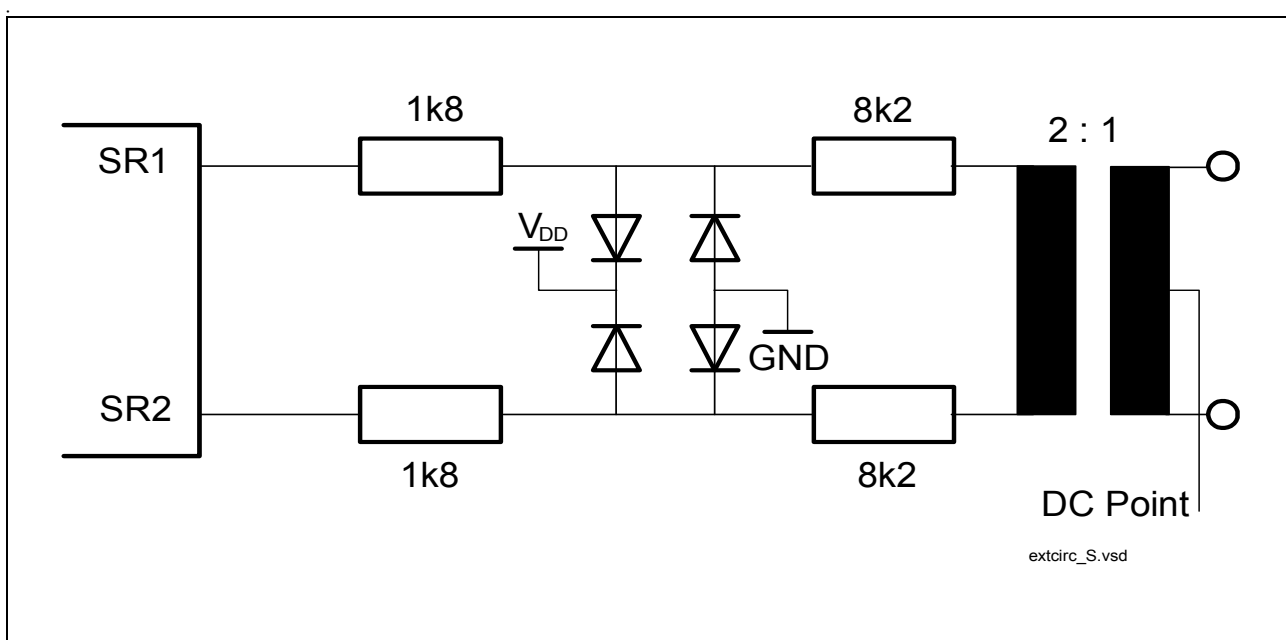
## Operational Description



**Figure 55 External Circuitry S-Interface Transmitter**

### Receiver

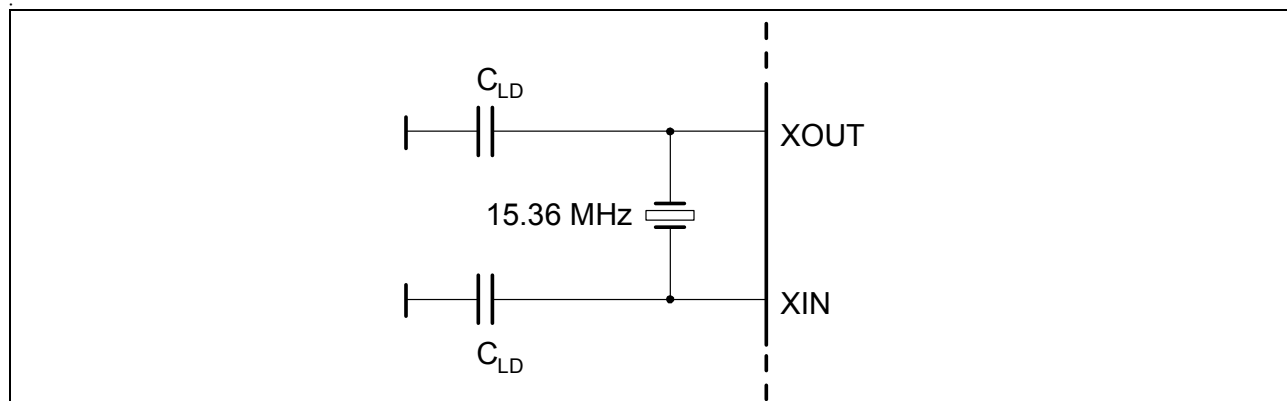
The **receiver** of the S-transceiver is symmetrical. 10 k $\Omega$  overall resistance are recommended in each receive path. It is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430 [6] and ETS 300012-1). The remaining resistance (1.8 k $\Omega$ ) protects the S-transceiver itself from input current peaks.



**Figure 56 External Circuitry S-Interface Receiver**

### 3.3.4 Oscillator Circuitry

**Figure 57** illustrates the recommended oscillator circuit.



**Figure 57** Crystal Oscillator

**Table 30** Crystal Parameters

| Parameter                       | Symbol         | Limit Values | Unit |
|---------------------------------|----------------|--------------|------|
| Frequency                       | f              | 15.36        | MHz  |
| Frequency calibration tolerance |                | +/-60        | ppm  |
| Load capacitance                | C <sub>L</sub> | 20           | pF   |
| Max. resonance resistance       | R1             | 20           | Ω    |
| Max. shunt capacitance          | C <sub>0</sub> | 7            | pF   |
| Oscillator mode                 |                | fundamental  |      |

### External Components and Parasitics

The load capacitance C<sub>L</sub> is computed from the external capacitances C<sub>LD</sub>, the parasitic capacitances C<sub>Par</sub> (pin and PCB capacitances to ground and V<sub>DD</sub>) and the stray capacitance C<sub>IO</sub> between XIN and XOUT:

$$C_L = \frac{(C_{LD} + C_{Par}) \times (C_{LD} + C_{Par})}{(C_{LD} + C_{Par}) + (C_{LD} + C_{Par})} + C_{IO}$$

For a specific crystal the total load capacitance is predefined, so the equation must be solved for the external capacitances C<sub>LD</sub>, which is usually the only variable to be determined by the circuit designer. Typical values for the capacitances C<sub>LD</sub> connected to the crystal are 22 - 33 pF.

### 3.3.5 General

- low power LEDs

## 4 Register Description

### 4.1 Address Space

|                 |                                                     |
|-----------------|-----------------------------------------------------|
| 7D <sub>H</sub> | U-Transceiver                                       |
| 60 <sub>H</sub> | Monitor Handler                                     |
| 5C <sub>H</sub> | IOM <sup>®</sup> -2 Handler<br>(CDA, TSDP, CR, STI) |
| 40 <sub>H</sub> | Interrupt, Global Registers                         |
| 3C <sub>H</sub> | S-Transceiver                                       |
| 30 <sub>H</sub> | CI-Register                                         |
| 2E <sub>H</sub> | MODEH-Register                                      |
| 22 <sub>H</sub> | reserved                                            |
| 00 <sub>H</sub> |                                                     |

**Figure 58 Address Space**

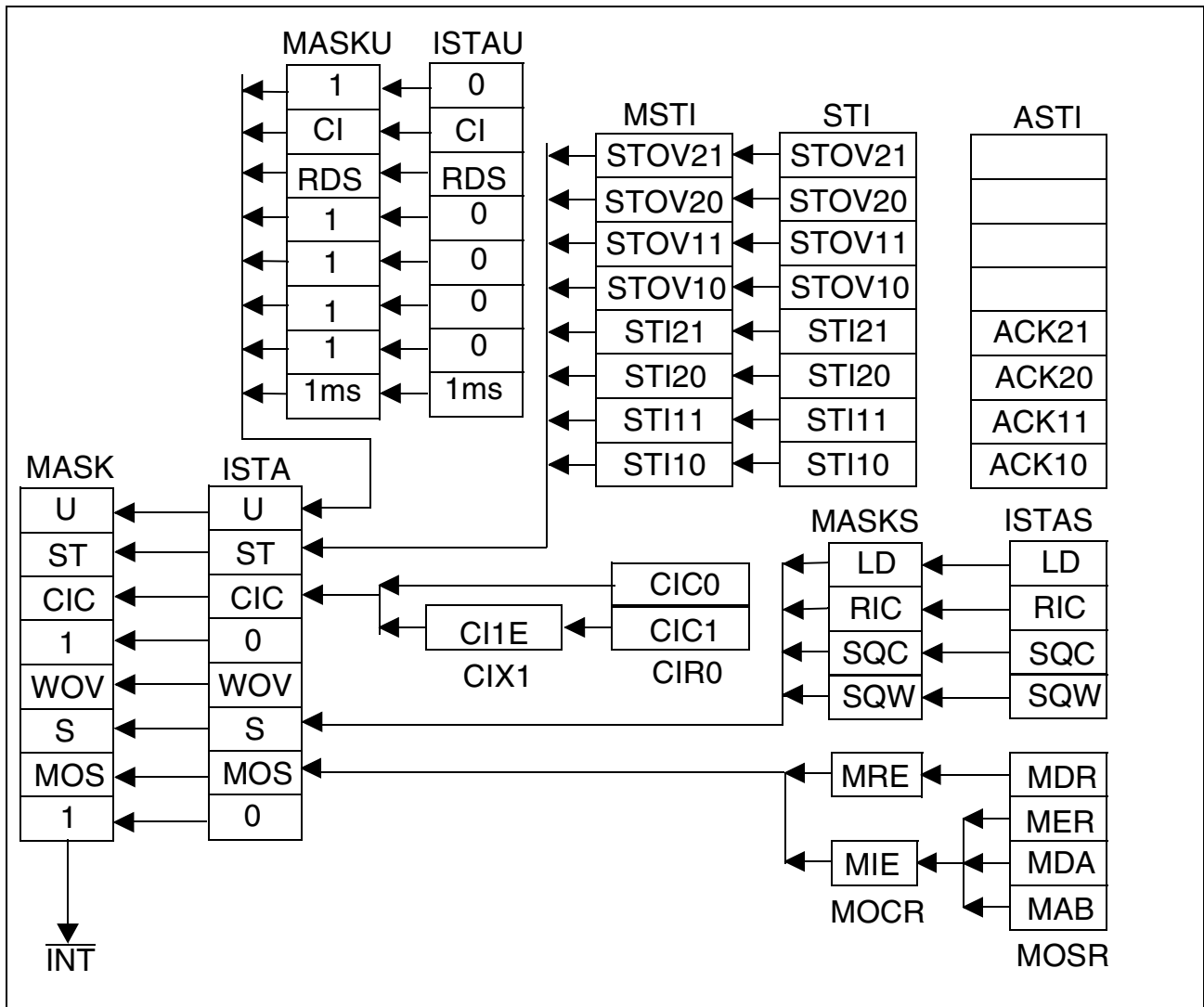
### 4.2 Interrupts

Special events in the T-SMINT<sup>®</sup>I are indicated by means of a single interrupt output, which requests the host to read status information from the T-SMINT<sup>®</sup>I or transfer data from/to the T-SMINT<sup>®</sup>I.

Since only one  $\overline{\text{INT}}$  request output is provided, the cause of an interrupt must be determined by the host reading the interrupt status registers of the T-SMINT<sup>®</sup>I.

The structure of the interrupt status registers is shown in [Figure 59](#).

## Register Description



**Figure 59 T-SMINT®I Interrupt Status Registers**

After the T-SMINT®I has requested an interrupt by setting its  $\overline{\text{INT}}$  pin to low, the host must read first the T-SMINT®I interrupt status register (ISTA) in the associated interrupt service routine. The  $\overline{\text{INT}}$  pin of the T-SMINT®I remains active until all interrupt sources are cleared. Therefore, it is possible that the INT pin is still active when the interrupt service routine is finished.

Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF<sub>H</sub> into the MASK register) and writing back the old mask to the MASK register.

## Register Description

### 4.3 Register Summary

r(0) = reserved, implemented as zero

#### CI Handler

| Name  | 7        | 6 | 5 | 4    | 3    | 2    | 1    | 0    | ADDR                                 | R/W | RES             |
|-------|----------|---|---|------|------|------|------|------|--------------------------------------|-----|-----------------|
| MODEH | reserved |   |   |      |      |      |      |      | 00 <sub>H</sub><br>-21 <sub>H</sub>  |     |                 |
|       | 1        | 1 | 0 | r(0) | 0    | DIM2 | DIM1 | DIM0 | 22 <sub>H</sub>                      | R/W | C0 <sub>H</sub> |
|       | reserved |   |   |      |      |      |      |      | 23 <sub>H</sub> -<br>2D <sub>H</sub> |     |                 |
| CIR0  | CODR0    |   |   |      | CIC0 | CIC1 | S/G  | BAS  | 2E <sub>H</sub>                      | R   | F3 <sub>H</sub> |
| CIX0  | CODX0    |   |   |      | TBA2 | TBA1 | TBA0 | BAC  | 2E <sub>H</sub>                      | W   | FE <sub>H</sub> |
| CIR1  | CODR1    |   |   |      |      |      | CICW | CI1E | 2F <sub>H</sub>                      | R   | FE <sub>H</sub> |
| CIX1  | CODX1    |   |   |      |      |      | CICW | CI1E | 2F <sub>H</sub>                      | W   | FE <sub>H</sub> |

**Register Description**
**S-Transceiver**

| Name        | 7          | 6    | 5          | 4     | 3           | 2       | 1    | 0    | ADDR                             | R/W | RES             |
|-------------|------------|------|------------|-------|-------------|---------|------|------|----------------------------------|-----|-----------------|
| S_<br>CONF0 | DIS_<br>TR | BUS  | EN_<br>ICV | 0     | L1SW        | 0       | EXLP | 0    | 30 <sub>H</sub>                  | R/W | 40 <sub>H</sub> |
|             | reserved   |      |            |       |             |         |      |      | 31 <sub>H</sub>                  |     |                 |
| S_<br>CONF2 | DIS_<br>TX | 0    | 0          | 0     | 0           | 0       | 0    | 0    | 32 <sub>H</sub>                  | R/W | 80 <sub>H</sub> |
| S_STA       | RINF       |      | 0          | ICV   | 0           | FSYN    | 0    | LD   | 33 <sub>H</sub>                  | R   | 00 <sub>H</sub> |
| S_CMD       | XINF       |      |            | DPRIO | 1           | PD      | LP_A | 0    | 34 <sub>H</sub>                  | R/W | 08 <sub>H</sub> |
| SQRR        | MSYN       | MFEN | 0          | 0     | SQR1        | SQR2    | SQR3 | SQR4 | 35 <sub>H</sub>                  | R   | 00 <sub>H</sub> |
| SQXR        | 0          | MFEN | 0          | 0     | SQX1        | SQX2    | SQX3 | SQX4 | 35 <sub>H</sub>                  | W   | 00 <sub>H</sub> |
|             | reserved   |      |            |       |             |         |      |      | 36 <sub>H</sub> -37 <sub>H</sub> |     |                 |
| ISTAS       | 0          | x    | x          | x     | LD          | RIC     | SQC  | SQW  | 38 <sub>H</sub>                  | R   | 00 <sub>H</sub> |
| MASKS       | 1          | 1    | 1          | 1     | LD          | RIC     | SQC  | SQW  | 39 <sub>H</sub>                  | R/W | FF <sub>H</sub> |
| S_<br>MODE  | 0          | 0    | 0          | 0     | DCH_<br>INH | MODE2-0 |      |      | 3A <sub>H</sub>                  | R/W | 02 <sub>H</sub> |
|             | reserved   |      |            |       |             |         |      |      | 3B <sub>H</sub>                  |     |                 |

## Register Description

### Interrupt, General Configuration

| Name  | 7    | 6    | 5              | 4    | 3    | 2   | 1         | 0         | ADDR            | R/W | RES             |
|-------|------|------|----------------|------|------|-----|-----------|-----------|-----------------|-----|-----------------|
| ISTA  | U    | ST   | CIC            | 0    | WOV  | S   | MOS       | 0         | 3C <sub>H</sub> | R   | 00 <sub>H</sub> |
| MASK  | U    | ST   | CIC            | 1    | WOV  | S   | MOS       | 1         | 3C <sub>H</sub> | W   | FF <sub>H</sub> |
| MODE1 | MCLK |      | CDS            | WTC1 | WTC2 | CFS | RSS2      | RSS1      | 3D <sub>H</sub> | R/W | 04 <sub>H</sub> |
| MODE2 | LED2 | LED1 | LEDC           |      | 0    | 0   | AMOD      | PPSDX     | 3E <sub>H</sub> | R/W | 00 <sub>H</sub> |
| ID    | 0    | 0    | DESIGN         |      |      |     |           |           | 3F <sub>H</sub> | R   | 20 <sub>H</sub> |
| SRES  | 0    | 0    | RES_<br>CI/TIC | 0    | 0    | 0   | RES_<br>S | RES_<br>U | 3F <sub>H</sub> | W   | 00 <sub>H</sub> |

**Register Description**
**IOM Handler (Timeslot, Data Port Selection,  
CDA Data and CDA Control Register)**

| Name              | 7                               | 6 | 5          | 4     | 3     | 2     | 1     | 0    | ADDR                                 | R/W | RES             |
|-------------------|---------------------------------|---|------------|-------|-------|-------|-------|------|--------------------------------------|-----|-----------------|
| CDA10             | Controller Data Access Register |   |            |       |       |       |       |      | 40 <sub>H</sub>                      | R/W | FF <sub>H</sub> |
| CDA11             | Controller Data Access Register |   |            |       |       |       |       |      | 41 <sub>H</sub>                      | R/W | FF <sub>H</sub> |
| CDA20             | Controller Data Access Register |   |            |       |       |       |       |      | 42 <sub>H</sub>                      | R/W | FF <sub>H</sub> |
| CDA21             | Controller Data Access Register |   |            |       |       |       |       |      | 43 <sub>H</sub>                      | R/W | FF <sub>H</sub> |
| CDA_<br>TSDP10    | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 44 <sub>H</sub>                      | R/W | 00 <sub>H</sub> |
| CDA_<br>TSDP11    | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 45 <sub>H</sub>                      | R/W | 01 <sub>H</sub> |
| CDA_<br>TSDP20    | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 46 <sub>H</sub>                      | R/W | 80 <sub>H</sub> |
| CDA_<br>TSDP21    | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 47 <sub>H</sub>                      | R/W | 81 <sub>H</sub> |
|                   | reserved                        |   |            |       |       |       |       |      | 48 <sub>H</sub> ~<br>4B <sub>H</sub> |     |                 |
| S_<br>TSDP_<br>B1 | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 4C <sub>H</sub>                      | R/W | 84 <sub>H</sub> |
| S_<br>TSDP_<br>B2 | DPS                             | 0 | 0          | 0     | TSS   |       |       |      | 4D <sub>H</sub>                      | R/W | 85 <sub>H</sub> |
| CDA1_<br>CR       | 0                               | 0 | EN_<br>TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4E <sub>H</sub>                      | R/W | 00 <sub>H</sub> |
| CDA2_<br>CR       | 0                               | 0 | EN_<br>TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4F <sub>H</sub>                      | R/W | 00 <sub>H</sub> |

## Register Description

### IOM Handler (Control Registers, Synchronous Transfer Interrupt Control)

| Name    | 7        | 6         | 5         | 4       | 3      | 2      | 1      | 0       | ADDR                             | R/W | RES             |
|---------|----------|-----------|-----------|---------|--------|--------|--------|---------|----------------------------------|-----|-----------------|
| S_CR    | reserved |           |           |         |        |        |        |         | 50 <sub>H</sub>                  |     |                 |
|         | 1        | CI_CS     | EN_D      | EN_B2R  | EN_B1R | EN_B2X | EN_B1X | D_CS    | 51 <sub>H</sub>                  | R/W | FF <sub>H</sub> |
| CI_CR   | DPS_CI1  | EN_CI1    | 0         | 0       | 0      | 1      | 0      |         | 52 <sub>H</sub>                  | R/W | 04 <sub>H</sub> |
| MON_CR  | DPS      | EN_MON    | 0         | 0       | 0      | 0      | MCS    |         | 53 <sub>H</sub>                  | R/W | 40 <sub>H</sub> |
| SDS1_CR | ENS_TSS  | ENS_TSS+1 | ENS_TSS+3 | 0       | TSS    |        |        |         | 54 <sub>H</sub>                  | R/W | 00 <sub>H</sub> |
| SDS2_CR | ENS_TSS  | ENS_TSS+1 | ENS_TSS+3 | 0       | TSS    |        |        |         | 55 <sub>H</sub>                  | R/W | 00 <sub>H</sub> |
| IOM_CR  | SPU      | 0         | 0         | TIC_DIS | EN_BCL | 0      | DIS_OD | DIS_IOM | 56 <sub>H</sub>                  | R/W | 08 <sub>H</sub> |
| MCDA    | MCDA21   |           | MCDA20    |         | MCDA11 |        | MCDA10 |         | 57 <sub>H</sub>                  | R   | FF <sub>H</sub> |
| STI     | STOV21   | STOV20    | STOV11    | STOV10  | STI21  | STI20  | STI11  | STI10   | 58 <sub>H</sub>                  | R   | 00 <sub>H</sub> |
| ASTI    | 0        | 0         | 0         | 0       | ACK21  | ACK20  | ACK11  | ACK10   | 58 <sub>H</sub>                  | W   | 00 <sub>H</sub> |
| MSTI    | STOV21   | STOV20    | STOV11    | STOV10  | STI21  | STI20  | STI11  | STI10   | 59 <sub>H</sub>                  | R/W | FF <sub>H</sub> |
|         | reserved |           |           |         |        |        |        |         | 5A <sub>H</sub> -5B <sub>H</sub> |     |                 |

## Register Description

### MONITOR Handler

| Name  | 7                     | 6   | 5   | 4   | 3 | 2   | 1 | 0    | ADDR            | R/W | RES             |
|-------|-----------------------|-----|-----|-----|---|-----|---|------|-----------------|-----|-----------------|
| MOR   | MONITOR Receive Data  |     |     |     |   |     |   |      | 5C <sub>H</sub> | R   | FF <sub>H</sub> |
| MOX   | MONITOR Transmit Data |     |     |     |   |     |   |      | 5C <sub>H</sub> | W   | FF <sub>H</sub> |
| MOSR  | MDR                   | MER | MDA | MAB | 0 | 0   | 0 | 0    | 5D <sub>H</sub> | R   | 00 <sub>H</sub> |
| MOCR  | MRE                   | MRC | MIE | MXC | 0 | 0   | 0 | 0    | 5E <sub>H</sub> | R/W | 00 <sub>H</sub> |
| MSTA  | 0                     | 0   | 0   | 0   | 0 | MAC | 0 | TOUT | 5F <sub>H</sub> | R   | 00 <sub>H</sub> |
| MCONF | 0                     | 0   | 0   | 0   | 0 | 0   | 0 | TOUT | 5F <sub>H</sub> | W   | 00 <sub>H</sub> |

## Register Description

### U-Transceiver

| Name           | 7                         | 6   | 5     | 4     | 3               | 2    | 1   | 0    | ADDR                                 | R/W  | RES             |
|----------------|---------------------------|-----|-------|-------|-----------------|------|-----|------|--------------------------------------|------|-----------------|
| OPMODE         | 0                         | UCI | 0     | 0     | 0               | 0    | 0   | 0    | 60 <sub>H</sub>                      | R*/W | 00 <sub>H</sub> |
|                | reserved                  |     |       |       |                 |      |     |      | 61 <sub>H</sub> -<br>6C <sub>H</sub> |      |                 |
| UCIR           | 0                         | 0   | 0     | 0     | C/I code output |      |     |      | 6D <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| UCIW           | 0                         | 0   | 0     | 0     | C/I code input  |      |     |      | 6E <sub>H</sub>                      | W    | 01 <sub>H</sub> |
| LOOP           | reserved                  |     |       |       |                 |      |     |      | 6F <sub>H</sub>                      |      |                 |
|                | 0                         | 0   | TRANS | U/IOM | 1               | LBBD | LB2 | LB1  | 70 <sub>H</sub>                      | R*/W | 08 <sub>H</sub> |
|                | reserved                  |     |       |       |                 |      |     |      | 71 <sub>H</sub>                      |      |                 |
| RDS            | Block Error Counter Value |     |       |       |                 |      |     |      | 72 <sub>H</sub>                      | R    | 00 <sub>H</sub> |
|                | reserved                  |     |       |       |                 |      |     |      | 73 <sub>H</sub> -<br>79 <sub>H</sub> |      |                 |
| ISTAU          | 0                         | CI  | RDS   | 0     | 0               | 0    | 0   | 1 ms | 7A <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| MASKU          | 1                         | CI  | RDS   | 1     | 1               | 1    | 1   | 1 ms | 7B <sub>H</sub>                      | R*/W | FF <sub>H</sub> |
|                | reserved                  |     |       |       |                 |      |     |      | 7C <sub>H</sub>                      |      |                 |
| FW_<br>VERSION | FW Version Number         |     |       |       |                 |      |     |      | 7D <sub>H</sub>                      | R    | 3E <sub>H</sub> |

Note: Registers, which are denoted as 'reserved', may not be accessed by the  $\mu\text{C}$ , neither for read nor for write operations.

#### 4.3.1 Reset of U-Transceiver Functions During Deactivation or with C/I-Code RESET

The following U-transceiver register is reset upon transition to state 'Deactivating' or with software reset:

## Register Description

**Table 31 Reset of U-Transceiver Functions During Deactivation or with C/I-Code RESET**

| Register | Affected Bits/ Comment                    |
|----------|-------------------------------------------|
| LOOP     | only the bits LBBD, LB2 and LB1 are reset |

### 4.3.2 Mode Register Evaluation Timing

**Table 32** lists registers, which are evaluated and executed immediately.

**Table 32 Mode Register with Immediate Evaluation and Execution**

| Register | Affected Bits     | Comment |
|----------|-------------------|---------|
| OPMODE   | UCI               |         |
| LOOP     | complete register |         |
| MASKU    | complete register |         |

## Register Description

### 4.4 Detailed C/I Registers

#### 4.4.1 MODEH - Mode Register IOM-2

**MODEH** read/write Address: 22<sub>H</sub>  
Value after reset: C0<sub>H</sub>

|   |   |   |      |   |      |      |      |
|---|---|---|------|---|------|------|------|
| 7 |   |   |      |   |      |      | 0    |
| 1 | 1 | 0 | r(0) | 0 | DIM2 | DIM1 | DIM0 |

**DIM2-0** Digital Interface Modes  
These bits define the characteristics of the IOM Data Ports (DU, DD). The DIM0 bit enables/disables the stop/go bit (S/G) evaluation. The DIM1 bit enables/disables the TIC bus access. The effect of the individual DIM bits is as follows:

- 0-0 = Stop/go bit evaluation is disabled
- 0-1 = Stop/go bit evaluation is enabled
- 00- = TIC bus access is enabled
- 01- = TIC bus access is disabled
- 1xx = Reserved

#### 4.4.2 CIR0 - Command/Indication Receive 0

**CIR0** read Address: 2E<sub>H</sub>  
Value after reset: F3<sub>H</sub>

|   |       |      |      |     |     |
|---|-------|------|------|-----|-----|
| 7 |       |      |      |     | 0   |
|   | CODR0 | CIC0 | CIC1 | S/G | BAS |

## Register Description

### **CODR0** C/I0 Code Receive

Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

### **CIC0** C/I0 Code Change

0 = No change in the received Command/Indication code has been recognized

1 = A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

### **CIC1** C/I1 Code Change

0 = No change in the received Command/Indication code has been recognized

1 = A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

### **S/G** Stop/Go Bit Monitoring

Indicates the availability of the upstream D-channel;

0 = Go

1 = Stop

### **BAS** Bus Access Status

Indicates the state of the TIC-bus:

0 = the T-SMINT<sup>®</sup> I itself occupies the D- and C/I-channel

1 = another device occupies the D- and C/I-channel

Note: The CODR0 bits are updated every time a new C/I-code is detected in two consecutive IOM-frames. If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I code are made available in CIR0 at the first and second read of that register.

## Register Description

### 4.4.3 CIX0 - Command/Indication Transmit 0

**CIX0** write Address: 2E<sub>H</sub>

Value after reset: FE<sub>H</sub>

|       |  |      |      |      |     |
|-------|--|------|------|------|-----|
| 7     |  |      |      |      | 0   |
| CODX0 |  | TBA2 | TBA1 | TBA0 | BAC |

**CODX0** C/I0-Code Transmit

Code to be transmitted in the C/I-channel 0. The code is only transmitted if the TIC bus is occupied, otherwise "1s" are transmitted.

**TBA2-0** TIC Bus Address

Defines the individual address for the T-SMINT<sup>®</sup>I on the IOM bus. This address is used to access the C/I- and D-channel on the IOM interface.

Note: If only one device is liable to transmit in the C/I- and D-channels of the IOM it should always be given the address value '7'.

**BAC** Bus Access Control

Only valid if the TIC-bus feature is enabled (MODE:DIM2-0).

0 = inactive

1 = The T-SMINT<sup>®</sup>I will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

Note: Access is always granted by default to the T-SMINT<sup>®</sup>I with TIC-Bus Address (TBA2-0, CIX0 register) '7', which has the lowest priority in a bus configuration.

### 4.4.4 CIR1 - Command/Indication Receive 1

**CIR1** read Address: 2F<sub>H</sub>

Value after reset: FE<sub>H</sub>

## Register Description

|       |              |
|-------|--------------|
| 7     | 0            |
| CODR1 | CICW    CI1E |

**CODR1**    C/I1-Code Receive

**CICW**    C/I-Channel Width  
Contains the read back value from CIX1 register (see below)

- 0 =    4 bit C/I1 channel width
- 1 =    6 bit C/I1 channel width

**CI1E**    C/I1-channel Interrupt Enable  
Contains the read back value from CIX1 register (see below)

- 0 =    Interrupt generation ISTA.CIC of CIR0.CIC1 is masked
- 1 =    Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled

### 4.4.5    CIX1 - Command/Indication Transmit 1

**CIX1**    write    Address:    2F<sub>H</sub>  
Value after reset: FE<sub>H</sub>

|       |              |
|-------|--------------|
| 7     | 0            |
| CODX1 | CICW    CI1E |

**CODX1**    C/I1-Code Transmit  
Bits 5-0 of C/I-channel 1

**CICW**    C/I-Channel Width

- 0 =    4 bit C/I1 channel width
- 1 =    6 bit C/I1 channel width

## Register Description

The C/I1 handler always reads and writes 6-bit values but if 4-bit is selected, the higher two bits are ignored for interrupt generation. However, in write direction the full CODX1 code is transmitted, i.e. the host must write the higher two bits to “1”.

### CI1E C/I1-channel Interrupt Enable

0 = Interrupt generation ISTA.CIC of CIR0.CIC1 is masked

1 = Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled

## 4.5 Detailed S-Transceiver Registers

### 4.5.1 S\_CONF0 - S-Transceiver Configuration Register 0

**S\_CONF0** read/write Address: 30<sub>H</sub>

Value after reset: 40<sub>H</sub>

|        |     |        |   |      |   |      |   |
|--------|-----|--------|---|------|---|------|---|
| 7      |     |        |   | 0    |   |      |   |
| DIS_TR | BUS | EN_ICV | 0 | L1SW | 0 | EXLP | 0 |

### DIS\_TR Disable Transceiver

0 = All S-transceiver functions are enabled.

1 = All S-transceiver functions are disabled and powered down (analog and digital parts).

### BUS Point-to-Point / Bus Selection

0 = Adaptive Timing (Point-to-Point, extended passive bus).

1 = Fixed Timing (Short passive bus), directly derived from transmit clock.

### EN\_ICV Enable Far End Code Violation

0 = normal operation.

1 = ICV enabled. The receipt of at least one illegal code violation within one multi-frame according to ANSI T1.605 is indicated by the C/I indication ‘1011’ (CVR) in two consecutive IOM frames.

## Register Description

**L1SW** Enable Layer 1 State Machine in Software

0 = Layer 1 state machine of the T-SMINT<sup>®</sup>I is used.

1 = Layer 1 state machine is disabled. The functionality must be realized in software.  
The commands are written to register S\_CMD and the status read in the S\_STA.

**EXLP** External Loop

In case the analog loopback is activated with C/I = ARL or with the LP\_A bit in the S\_CMD register the loop is a

0 = internal loop next to the line pins

1 = external loop which has to be closed between SR1/SR2 and SX1/SX2

Note: For the external loop the transmitter must be enabled (S\_CONF2:DIS\_TX = 0).

### 4.5.2 S\_CONF2 - S-Transmitter Configuration Register 2

**S\_CONF2** read/write Address: 32<sub>H</sub>

Value after reset: 80<sub>H</sub>

|        |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|
| 7      |   |   |   |   |   |   | 0 |
| DIS_TX | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DIS\_TX** Disable Line Driver

0 = Transmitter is enabled

1 = Transmitter is disabled

### 4.5.3 S\_STA - S-Transceiver Status Register

**S\_STA** read Address: 33<sub>H</sub>

Value after reset: 00<sub>H</sub>

## Register Description

|      |   |     |   |      |   |    |
|------|---|-----|---|------|---|----|
| 7    |   |     |   |      |   | 0  |
| RINF | 0 | ICV | 0 | FSYN | 0 | LD |

Important: This register is used only if the Layer 1 state machine of the device is disabled (S\_CONF0:L1SW = 1) and implemented in software! With the layer 1 state machine enabled, the signals from this register are automatically evaluated.

### RINF Receiver INFO

- 00 = Received INFO 0 (no signal)
- 01 = Received any signal except INFO 0 or INFO 3
- 10 = reserved
- 11 = Received INFO 3

### ICV Illegal Code Violation

- 0 = No illegal code violation is detected.
- 1 = Illegal code violation (ANSI T1.605) in data stream is detected.

### FSYN Frame Synchronization State

- 0 = The S/T receiver is not synchronized.
- 1 = The S/T receiver has synchronized to the framing bit F.

### LD Level Detection

- 0 = No receive signal has been detected on the line.
- 1 = Any receive signal has been detected on the line.

## 4.5.4 S\_CMD - S-Transceiver Command Register

**S\_CMD** read/write Address: 34<sub>H</sub>

Value after reset: 08<sub>H</sub>

|      |       |   |    |      |   |
|------|-------|---|----|------|---|
| 7    |       |   |    |      | 0 |
| XINF | DPRIO | 1 | PD | LP_A | 0 |

## Register Description

Important: This register - except bit DPRIO - is writable only if the Layer 1 state machine of the device is disabled (S\_CONF0.L1SW = 1) and implemented in software! With the device layer 1 state machine enabled, the signals from this register are automatically generated. DPRIO can also be written in intelligent NT mode.

### **XINF** Transmit INFO

- 000 = Transmit INFO 0
- 001 = reserved
- 010 = Transmit INFO 2
- 011 = Transmit INFO 4
- 100 = Send continuous pulses at 192 kbit/s alternating or 96 kHz rectangular, respectively (TM2)
- 101 = Send single pulses at 4 kbit/s with alternating polarity corresponding to 2 kHz fundamental mode (TM1)
- 11x = reserved

### **DPRIO** D-Channel Priority

- 0 = Priority class 1 for D channel access on IOM
- 1 = Priority class 2 for D channel access on IOM

### **PD** Power Down

- 0 = The transceiver is set to operational mode
- 1 = The transceiver is set to power down mode

### **LP\_A** Loop Analog

The setting of this bit corresponds to the C/I command ARL.

- 0 = Analog loop is open
- 1 = Analog loop is closed internally or externally according to the EXLP bit in the S\_CONF0 register

## 4.5.5 SQRR - S/Q-Channel Receive Register

**SQRR** read Address: 35<sub>H</sub>

Value after reset: 00<sub>H</sub>

## Register Description

|      |      |   |   |      |      |      |      |
|------|------|---|---|------|------|------|------|
| 7    |      |   |   |      |      |      | 0    |
| MSYN | MFEN | 0 | 0 | SQR1 | SQR2 | SQR3 | SQR4 |

### **MSYN** Multi-frame Synchronization State

0 = The S/T receiver has not synchronized to the received  $F_A$  and M bits

1 = The S/T receiver has synchronized to the received  $F_A$  and M bits

### **MFEN** Multiframe Enable

Read-back of the MFEN bit of the SQXR register

0 = S/T multiframe is disabled

1 = S/T multiframe is enabled

### **SQR1-4** Received S/Q Bits

Received Q bits in frames 1, 6, 11 and 16

## 4.5.6 SQXR- S/Q-Channel Transmit Register

**SQXR** write Address: 35<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |      |   |   |      |      |      |      |
|---|------|---|---|------|------|------|------|
| 7 |      |   |   |      |      |      | 0    |
| 0 | MFEN | 0 | 0 | SQX1 | SQX2 | SQX3 | SQX4 |

### **MFEN** Multiframe Enable

Used to enable or disable the multiframe structure.

0 = S/T multiframe is disabled

1 = S/T multiframe is enabled

### **SQX1-4** Transmitted S/Q Bits

Transmitted S bits in frames 1, 6, 11 and 16

## Register Description

### 4.5.7 ISTAS - Interrupt Status Register S-Transceiver

**ISTAS** read Address: 38<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |   |   |   |    |     |     |     |
|---|---|---|---|----|-----|-----|-----|
| 7 |   |   |   |    |     |     | 0   |
| x | x | x | x | LD | RIC | SQC | SQW |

These bits are set if an interrupt status occurs and an interrupt signal is activated if the corresponding mask bit is set to “0”. If the mask bit is set to “1” no interrupt is generated, however the interrupt status bit is set in ISTAS. RIC, SQC and SQW are cleared by reading the corresponding source register S\_STA, SQRR or writing SQXR, respectively.

**x** Reserved

**LD** Level Detection

0 = inactive

1 = Any receive signal has been detected on the line. This bit is set to “1” (i.e. an interrupt is generated if not masked) as long as any receive signal is detected on the line.

**RIC** Receiver INFO Change

0 = inactive

1 = RIC is activated if one of the S\_STA bits RINF or ICV has changed.

**SQC** S/Q-Channel Change

0 = inactive

1 = A change in the received 4-bit Q-channel has been detected. The new code can be read from the SQRx bits of registers SQRR within the next multiframe<sup>1)</sup>. This bit is reset by a read access to the SQRR register.

**SQW** S/Q-Channel Writable

## Register Description

0 = inactive

1 = The S channel data for the next multiframe is writable.  
The register for the S bits to be transmitted has to be written within the next multiframe. This bit is reset by writing register SQXR.  
This timing signal is indicated with the start of every multiframe.  
Data which is written right after SQW-indication will be transmitted with the start of the following multiframe. Data which is written before SQW-indication is transmitted in the multiframe which is indicated by SQW.  
SQW and SQC could be generated at the same time.

<sup>1)</sup> Register SQRR stays valid as long as no code change has been received.

### 4.5.8 MASKS - Mask S-Transceiver Interrupt

**MASKS** read/write Address: 39<sub>H</sub>

Value after reset: FF<sub>H</sub>

|   |   |   |   |    |     |     |     |
|---|---|---|---|----|-----|-----|-----|
| 7 |   |   |   |    |     |     | 0   |
| 1 | 1 | 1 | 1 | LD | RIC | SQC | SQW |

**Bit 3..0** Mask bits

0 = The transceiver interrupts LD, RIC, SQC and SQW are enabled

1 = The transceiver interrupts LD, RIC, SQC and SQW are masked

### 4.5.9 S\_MODE - S-Transceiver Mode

**S\_MODE** read/write Address: 3A<sub>H</sub>

Value after reset: 02<sub>H</sub>

|   |   |   |   |         |      |   |
|---|---|---|---|---------|------|---|
| 7 |   |   |   |         |      | 0 |
| 0 | 0 | 0 | 0 | DCH_INH | MODE |   |

## Register Description

**DCH\_**  
**INH** D-Channel Inhibit

- 0 = inactive  
1 = The S-transceiver blocks the access to the D-channel on S by inverting the E-bits.

**MODE** Mode Selection

- 000 = reserved  
001 = reserved  
010 = NT (without D-channel handler)  
011 = LT-S (without D-channel handler)  
110 Intelligent NT mode (with NT state machine and with D-channel handler)  
111 Intelligent NT mode (with LT-S state machine and with D-channel handler)  
100 reserved  
101 reserved

## 4.6 Interrupt and General Configuration Registers

### 4.6.1 ISTA - Interrupt Status Register

**ISTA** read Address: 3C<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |    |     |   |     |   |     |   |
|---|----|-----|---|-----|---|-----|---|
| 7 |    |     |   |     |   |     | 0 |
| U | ST | CIC | 0 | WOV | S | MOS | 0 |

**U** U-Transceiver Interrupt

- 0 = inactive  
1 = An interrupt was generated by the U-transceiver. Read the ISTAU register.

## Register Description

|            |                                                                                                                                                                                                                                                                                                |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>ST</b>  | Synchronous Transfer                                                                                                                                                                                                                                                                           |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| 1 =        | This interrupt enables the microcontroller to lock on to the IOM <sup>®</sup> -2 timing, for synchronous transfers.                                                                                                                                                                            |
| <b>CIC</b> | C/I Channel Change                                                                                                                                                                                                                                                                             |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| 1 =        | A change in C/I0 channel or C/I1 channel has been recognized. The actual value can be read from CIR0 or CIR1.                                                                                                                                                                                  |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| <b>WOV</b> | Watchdog Timer Overflow                                                                                                                                                                                                                                                                        |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| 1 =        | Signals the expiration of the watchdog timer, which means that the microcontroller has failed to set the watchdog timer control bits WTC1 and WTC2 (MODE1 register) in the correct manner. A reset out pulse on pin $\overline{\text{RSTO}}$ has been generated by the T-SMINT <sup>®</sup> I. |
| <b>S</b>   | S-Transceiver Interrupt                                                                                                                                                                                                                                                                        |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| 1 =        | An interrupt was generated by the S-transceiver. Read the ISTAS register.                                                                                                                                                                                                                      |
| <b>MOS</b> | MONITOR Status                                                                                                                                                                                                                                                                                 |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |
| 1 =        | A change in the MONITOR Status Register (MOSR) has occurred.                                                                                                                                                                                                                                   |
| 0 =        | inactive                                                                                                                                                                                                                                                                                       |

Note: A read of the ISTA register clears only the WOVS interrupt. The other interrupts are cleared by reading the corresponding status register.

### 4.6.2 MASK - Mask Register

**MASK** write Address:  $3C_H$   
Value after reset:  $FF_H$

## Register Description

|   |    |     |   |     |   |     |   |
|---|----|-----|---|-----|---|-----|---|
| 7 |    |     |   |     |   |     | 0 |
| U | ST | CIC | 1 | WOV | S | MOS | 1 |

### Bit 7..0 Mask bits

0 = Interrupt is not masked

1 = Interrupt is masked

Each interrupt source in the ISTA register can be selectively masked by setting the corresponding bit in MASK to '1'. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to '0'.

Note: In the event of a C/I channel change, CIC is set in ISTA even if the corresponding mask bit in MASK is active, but no interrupt is generated.

### 4.6.3 MODE1 - Mode1 Register

#### MODE1

read/write

Address: 3D<sub>H</sub>

Value after reset: 04<sub>H</sub>

|      |     |      |      |     |      |      |
|------|-----|------|------|-----|------|------|
| 7    |     |      |      |     |      | 0    |
| MCLK | CDS | WTC1 | WTC2 | CFS | RSS2 | RSS1 |

#### MCLK Master Clock Frequency

The Master Clock Frequency bits control the microcontroller clock output depending on MODE1.CDS = '0' or '1' (Table [Table 2.1.3](#)).

|      | MODE1.CDS = '0' | MODE1.CDS = '1' |
|------|-----------------|-----------------|
| 00 = | 3.84 MHz        | 7.68 MHz        |
| 01 = | 0.96 MHz        | 1.92 MHz        |
| 10 = | 7.68 MHz        | 15.36 MHz       |
| 11 = | disabled        | disabled        |

## Register Description

### CDS Clock Divider Selection

- 0 = The 15.36 MHz oscillator clock divided by two is input to the MCLK prescaler
- 1 = The 15.36 MHz oscillator clock is input to the MCLK prescaler.

### WTC1, 2 Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected (RSS = '11') the watchdog timer is started. During every time period of 128 ms the microcontroller has to program the WTC1 and WTC2 bit in the following sequence ([Chapter 2.2](#)):

- 10 first step
- 01 second step

to reset and restart the watchdog timer.

If not, the timer expires and a WOV-interrupt (ISTA Register) together with a reset out pulse on pin  $\overline{\text{RSTO}}$  is generated.

The watchdog timer runs only when the internal IOM<sup>®</sup>-2 clocks are active, i.e. the watchdog timer is dead when bit CFS = 1 and the U and S-transceivers are in state power down.

### CFS Configuration Select

- 0 = The IOM<sup>®</sup>-2 interface clock and frame signals are always active, "Deactivated State" of the U-transceiver and the S-transceiver included.
- 1 = The IOM<sup>®</sup>-2 interface clocks and frame signals are inactive in the "Deactivated State" of the U-transceiver and the S-transceiver.

### RSS2, RSS1 Reset Source Selection 2,1

The T-SMINT<sup>®</sup>I reset sources can be selected according to the table below.

|      | C/I Code Change | Watchdog Timer                                     | POR/UVD and $\overline{\text{RSTO}}$ |
|------|-----------------|----------------------------------------------------|--------------------------------------|
| 00 = | --              | --                                                 | x                                    |
| 01 = |                 | $\overline{\text{RSTO}}$ disabled (high impedance) |                                      |
| 10 = | x               | --                                                 | x                                    |
| 11 = | --              | x                                                  | x                                    |

## Register Description

### 4.6.4 MODE2 - Mode2 Register

**MODE2** read/write Address: 3E<sub>H</sub>

Value after reset: 00<sub>H</sub>

|      |      |      |   |   |   |      |       |
|------|------|------|---|---|---|------|-------|
| 7    |      |      |   |   |   |      | 0     |
| LED2 | LED1 | LEDC | 0 | 0 | 0 | AMOD | PPSDX |

#### LED2,1 LED Control on pin $\overline{\text{ACT}}$

- 00 = High
- 01 = flashing at 2 Hz (1 : 1)\*
- 10 = flashing at 1 Hz (3 : 1)\*
- 11 = Low

#### LEDC LED Control Enable

- 0 = LED is controlled by the state machines as defined in [Table 3](#).
- 1 = LED is controlled via bits LED2,1.

#### AMOD Address Mode

Selects between direct and indirect register access of the parallel microcontroller interface.

- 0 = Indirect address mode is selected. The address line A0 is used to select between address (A0 = '0') and data (A0 = '1') register
- 1 = Direct address mode is selected. The address is applied to the address bus (A0-A6)

#### PPSDX Push/Pull Output for SDX

- 0 = The SDX pin has open drain characteristic
- 1 = The SDX pin has push/pull characteristic

### 4.6.5 ID - Identification Register

**ID** read Address: 3F<sub>H</sub>

Value after reset: 20<sub>H</sub>

## Register Description

|   |   |        |
|---|---|--------|
| 7 |   | 0      |
| 0 | 0 | DESIGN |

### DESIGN Design Number

The design number (DESIGN) allows to identify different hardware designs<sup>1)</sup> of the T-SMINT<sup>®</sup>I by software.

100000: Version 1.1

<sup>1)</sup> Distinction of different firmware versions is also possible by reading register (7D)<sub>H</sub> in the address space of the U-transceiver (see [Chapter 4.9.8](#)).

## 4.6.6 SRES - Software Reset Register

**SRES** write Address: 3F<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |   |                |   |   |   |       |       |
|---|---|----------------|---|---|---|-------|-------|
| 7 |   |                |   |   |   |       | 0     |
| 0 | 0 | RES_<br>CI/TIC | 0 | 0 | 0 | RES_S | RES_U |

**RES\_xx** Reset\_xx

0 = Deactivates the reset of the functional block xx

1 = Activates the reset of the functional block xx.

The reset state is activated as long as the bit is set to '1'

## 4.7 Detailed IOM<sup>®</sup>-2 Handler Registers

### 4.7.1 CDAXy - Controller Data Access Register xy

These registers are used for microcontroller access to the IOM<sup>®</sup>-2 timeslots as well as for timeslot manipulations. (e.g. loops, shifts, ... see also [“Controller Data Access \(CDA\)” on Page 30](#)).

**Register Description**
**CDAxy**

read/write

Address: 40-43<sub>H</sub>

7

0

|                                 |
|---------------------------------|
| Controller Data Access Register |
|---------------------------------|

Data register CDAxy which can be accessed by the controller.

| Register | Value after Reset | Register Address |
|----------|-------------------|------------------|
| CDA10    | FF <sub>H</sub>   | 40 <sub>H</sub>  |
| CDA11    | FF <sub>H</sub>   | 41 <sub>H</sub>  |
| CDA20    | FF <sub>H</sub>   | 42 <sub>H</sub>  |
| CDA21    | FF <sub>H</sub>   | 43 <sub>H</sub>  |

**4.7.2 XXX\_TSDPxy - Time Slot and Data Port Selection for CHxy**
**XXX\_TSDPxy**

read/write

Address: 44-4D<sub>H</sub>

7

0

|     |   |   |   |     |
|-----|---|---|---|-----|
| DPS | 0 | 0 | 0 | TSS |
|-----|---|---|---|-----|

| Register   | Value after Reset                    | Register Address   |
|------------|--------------------------------------|--------------------|
| CDA_TSDP10 | 00 <sub>H</sub> (= output on B1-DD)  | 44 <sub>H</sub>    |
| CDA_TSDP11 | 01 <sub>H</sub> (= output on B2-DD)  | 45 <sub>H</sub>    |
| CDA_TSDP20 | 80 <sub>H</sub> (= output on B1-DU)  | 46 <sub>H</sub>    |
| CDA_TSDP21 | 81 <sub>H</sub> (= output on B2-DU)  | 47 <sub>H</sub>    |
|            | reserved                             | 48-4B <sub>H</sub> |
| S_TSDP_B1  | 84 <sub>H</sub> (= output on TS4-DU) | 4C <sub>H</sub>    |
| S_TSDP_B2  | 85 <sub>H</sub> (= output on TS5-DU) | 4D <sub>H</sub>    |

This register determines the time slots and the data ports on the IOM<sup>®</sup>-2 Interface for the data channels xy of the functional units XXX (Controller Data Access (CDA) and S-transceiver (S)).

Note: The U-transceiver is always in IOM-2 channel 0.

## Register Description

### DPS Data Port Selection

- 0 = The data channel xy of the functional unit XXX is output on DD.  
The data channel xy of the functional unit XXX is input from DU.
- 1 = The data channel xy of the functional unit XXX is output on DU.  
The data channel xy of the functional unit XXX is input from DD.

Note: For the CDA (controller data access) data the input is determined by the CDAX\_CR.SWAP bit. If SWAP = '0' the input for the CDAXy data is vice versa to the output setting for CDAXy. If the SWAP = '1' the input from CDAX0 is vice versa to the output setting of CDAX1 and the input from CDAX1 is vice versa to the output setting of CDAX0.

### TSS Timeslot Selection

Selects one of the 12 timeslots from 0...11 on the IOM<sup>®</sup>-2 interface for the data channels.

### 4.7.3 CDAX\_CR - Control Register Controller Data Access CH1x

**CDAX\_CR** read/write Address: 4E-4F<sub>H</sub>

|   |   |        |       |       |       |       |      |
|---|---|--------|-------|-------|-------|-------|------|
| 7 |   |        |       |       |       |       | 0    |
| 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP |

| Register | Value after Reset | Register Address |
|----------|-------------------|------------------|
| CDA1_CR  | 00 <sub>H</sub>   | 4E <sub>H</sub>  |
| CDA2_CR  | 00 <sub>H</sub>   | 4F <sub>H</sub>  |

### EN\_TBM Enable TIC Bus Monitoring

- 0 = The TIC bus monitoring is disabled
- 1 = The TIC bus monitoring with the CDAX0 register is enabled. The TSDPx0 register must be set to 08<sub>H</sub> for monitoring from DU, or 88<sub>H</sub> for monitoring from DD.

### EN\_I1, EN\_I0 Enable Input CDAX1, CDAX0

## Register Description

0 = The input of the CDAX1, CDAX0 register is disabled

1 = The input of the CDAX1, CDAX0 register is enabled

**EN\_O1,** Enable Output CDAX1, CDAX0  
**EN\_O0**

0 = The output of the CDAX1, CDAX0 register is disabled

1 = The output of the CDAX1, CDAX0 register is enabled

**SWAP** **Swap Inputs**

0 = The time slot and data port for the input of the CDAXy register is defined by its own TSDPxy register. The data port for the CDAXy input is vice versa to the output setting for CDAXy.

1 = The input (time slot and data port) of the CDAX0 is defined by the TSDP register of CDAX1 and the input of CDAX1 is defined by the TSDP register of CDAX0. The data port for the CDAX0 input is vice versa to the output setting for CDAX1. The data port for the CDAX1 input is vice versa to the output setting for CDAX0. The input definition for time slot and data port CDAX0 are thus swapped to CDAX1 and for CDAX1 to CDAX0. The outputs are not affected by the SWAP bit.

### 4.7.4 S\_CR - Control Register S-Transceiver Data

**S\_CR** read/write Address: 51<sub>H</sub>

Value after reset: FF<sub>H</sub>

|   |       |      |        |        |        |        |      |
|---|-------|------|--------|--------|--------|--------|------|
| 7 |       |      |        |        |        |        | 0    |
| 1 | CI_CS | EN_D | EN_B2R | EN_B1R | EN_B2X | EN_B1X | D_CS |

**CI\_CS** C/I Channel Selection

This bit is used to select the IOM channel to which the S-transceiver C/I-channel is related to.

0 = C/I-channel in IOM-channel 0

1 = C/I-channel in IOM-channel 1

## Register Description

### **EN\_D** Enable Transceiver D-Channel Data

- 0 = The corresponding data path to the transceiver is disabled
- 1 = The corresponding data path to the transceiver is enabled.

### **EN\_B2R** Enable Transceiver B2 Receive Data (transmitter receives from IOM)

- 0 = The corresponding data path to the transceiver is disabled
- 1 = The corresponding data path to the transceiver is enabled.

### **EN\_B1R** Enable Transceiver B1 Receive Data (transmitter receives from IOM)

- 0 = The corresponding data path to the transceiver is disabled
- 1 = The corresponding data path to the transceiver is enabled.

### **EN\_B2X** Enable Transceiver B2 Transmit Data (transmitter transmits to IOM)

- 0 = The corresponding data path to the transceiver is disabled
- 1 = The corresponding data path to the transceiver is enabled.

### **EN\_B1X** Enable Transceiver B1 Transmit Data (transmitter transmits to IOM)

- 0 = The corresponding data path to the transceiver is disabled
- 1 = The corresponding data path to the transceiver is enabled.

These bits are used to individually enable/disable the D-channel and the receive/transmit paths for the B-channels for the S-transceiver.

### **D\_CS** D Channel Selection

This bit is used to select the IOM channel to which the S-transceiver D-channel is related to.

- 0 = D-channel in IOM-channel 0
- 1 = D-channel in IOM-channel 1

## 4.7.5 CI\_CR - Control Register for CI1 Data

**CI\_CR** read/write Address: 52<sub>H</sub>

Value after reset: 04<sub>H</sub>

## Register Description

|         |        |   |   |   |   |   |
|---------|--------|---|---|---|---|---|
| 7       |        |   |   |   |   | 0 |
| DPS_CI1 | EN_CI1 | 0 | 0 | 0 | 1 | 0 |

### **DPS\_CI1** Data Port Selection CI1 Handler

0 = The CI1 data is output on DD and input from DU

1 = The CI1 data is output on DU and input from DD

### **EN\_CI1** Enable CI1 Handler

0 = CI1 data access is disabled

1 = CI1 data access is enabled

Note: The timeslot for the C/I1 handler cannot be programmed but is fixed to IOM channel 1.

## 4.7.6 MON\_CR - Control Register Monitor Data

**MON\_CR** read/write Address: 53<sub>H</sub>

Value after reset: 40<sub>H</sub>

|     |        |   |   |   |   |     |
|-----|--------|---|---|---|---|-----|
| 7   |        |   |   |   |   | 0   |
| DPS | EN_MON | 0 | 0 | 0 | 0 | MCS |

### **DPS** Data Port Selection

0 = The Monitor data is output on DD and input from DU

1 = The Monitor data is output on DU and input from DD

### **EN\_MON** Enable Output

0 = The Monitor data input and output is disabled

1 = The Monitor data input and output is enabled

### **MCS** MONITOR Channel Selection

00 = The MONITOR data is output on MON0

## Register Description

01 = The MONITOR data is output on MON1

10 = The MONITOR data is output on MON2

11 = Not defined

### 4.7.7 SDS1\_CR - Control Register Serial Data Strobe 1

**SDS1\_CR** read/write Address: 54<sub>H</sub>

Value after reset: 00<sub>H</sub>

|             |               |               |   |     |
|-------------|---------------|---------------|---|-----|
| 7           |               |               | 0 |     |
| ENS_<br>TSS | ENS_<br>TSS+1 | ENS_<br>TSS+3 | 0 | TSS |

This register is used to select position and length of the strobe signal 1. The length can be any combination of two 8-bit timeslot (ENS\_TSS, ENS\_TSS+1) and one 2-bit timeslot (ENS\_TSS+3).

**ENS\_TSS** Enable Serial Data Strobe of timeslot TSS

0 = The serial data strobe signal SDS1 is inactive during TSS

1 = The serial data strobe signal SDS1 is active during TSS

**ENS\_TSS+1** Enable Serial Data Strobe of timeslot TSS+1

0 = The serial data strobe signal SDS1 is inactive during TSS+1

1 = The serial data strobe signal SDS1 is active during TSS+1

**ENS\_TSS+3** Enable Serial Data Strobe of timeslot TSS+3 (D-Channel)

0 = The serial data strobe signal SDS1 is inactive during the D-channel (bit7, 6) of TSS+3

1 = The serial data strobe signal SDS1 is active during the D-channel (bit7, 6) of TSS+3

## Register Description

**TSS** Timeslot Selection

Selects one of 12 timeslots on the IOM<sup>®</sup>-2 interface (with respect to FSC) during which SDS1 is active high. The data strobe signal allows standard data devices to access a programmable channel.

### 4.7.8 SDS2\_CR - Control Register Serial Data Strobe 2

**SDS2\_CR** read/write Address: 55<sub>H</sub>

Value after reset: 00<sub>H</sub>

|             |               |               |   |     |
|-------------|---------------|---------------|---|-----|
| 7           |               |               | 0 |     |
| ENS_<br>TSS | ENS_<br>TSS+1 | ENS_<br>TSS+3 | 0 | TSS |

This register is used to select position and length of the strobe signal 2. The length can be any combination of two 8-bit timeslot (ENS\_TSS, ENS\_TSS+1) and one 2-bit timeslot (ENS\_TSS+3).

**ENS\_  
TSS** Enable Serial Data Strobe of timeslot TSS

- 0 = The serial data strobe signal SDS2 is inactive during TSS
- 1 = The serial data strobe signal SDS2 is active during TSS

**ENS\_  
TSS+1** Enable Serial Data Strobe of timeslot TSS+1

- 0 = The serial data strobe signal SDS2 is inactive during TSS+1
- 1 = The serial data strobe signal SDS2 is active during TSS+1

**ENS\_  
TSS+3** Enable Serial Data Strobe of timeslot TSS+3 (D-Channel)

- 0 = The serial data strobe signal SDS2 is inactive during the D-channel (bit7, 6) of TSS+3
- 1 = The serial data strobe signal SDS2 is active during the D-channel (bit7, 6) of TSS+3

## Register Description

### TSS Timeslot Selection

Selects one of 12 timeslots on the IOM<sup>®</sup>-2 interface (with respect to FSC) during which SDS2 is active high. The data strobe signal allows standard data devices to access a programmable channel.

### 4.7.9 IOM\_CR - Control Register IOM Data

**IOM\_CR** read/write Address: 56<sub>H</sub>

Value after reset: 08<sub>H</sub>

|     |   |   |         |        |   |        |         |
|-----|---|---|---------|--------|---|--------|---------|
| 7   |   |   |         | 0      |   |        |         |
| SPU | 0 | 0 | TIC_DIS | EN_BCL | 0 | DIS_OD | DIS_IOM |

### SPU Software Power UP

0 = The DU line is normally used for transmitting data.

1 = Setting this bit to '1' will pull the DU line to low. This will enforce the T-SMINT<sup>®</sup>I and other connected layer 1 devices to deliver IOM-clocking.

### TIC\_DIS TIC Bus Disable

0 = The last octet of the last IOM time slot (TS 11) is used as TIC bus.

1 = The TIC bus is disabled. The last octet of the last IOM time slot (TS 11) can be used like any other time slot. This means that the timeslots TIC, A/B, S/G and BAC are not available any more.

### EN\_BCL Enable Bit Clock BCL

0 = The BCL clock is disabled (output is high impedant)

1 = The BCL clock is enabled

### DIS\_OD Disable Open Drain

0 = IOM outputs are open drain driver

1 = IOM outputs are push pull driver

## Register Description

### DIS\_IOM Disable IOM

DIS\_IOM should be set to '1' if external devices connected to the IOM interface should be "disconnected" e.g. for power saving purposes. However, the T-SMINT<sup>®</sup>I internal operation is independent of the DIS\_IOM bit.

0 = The IOM interface is enabled

1 = The IOM interface is disabled (FSC, DCL, clock outputs have high impedance; DU, DD data line inputs are switched off and outputs are high impedant)

### 4.7.10 MCDA - Monitoring CDA Bits

**MCDA** read Address: 57<sub>H</sub>

Value after reset: FF<sub>H</sub>

|        |      |        |      |        |      |        |      |   |  |
|--------|------|--------|------|--------|------|--------|------|---|--|
| 7      |      |        |      |        |      |        |      | 0 |  |
| MCDA21 |      | MCDA20 |      | MCDA11 |      | MCDA10 |      |   |  |
| Bit7   | Bit6 | Bit7   | Bit6 | Bit7   | Bit6 | Bit7   | Bit6 |   |  |

### MCDAxy Monitoring CDAxy Bits

Bit 7 and Bit 6 of the CDAxy registers are mapped into the MCDA register. This can be used for monitoring the D-channel bits on DU and DD and the "Echo bits" on the TIC bus with the same register.

### 4.7.11 STI - Synchronous Transfer Interrupt

**STI** read Address: 58<sub>H</sub>

Value after reset: 00<sub>H</sub>

|        |        |        |        |       |       |       |       |   |  |
|--------|--------|--------|--------|-------|-------|-------|-------|---|--|
| 7      |        |        |        |       |       |       |       | 0 |  |
| STOV21 | STOV20 | STOV11 | STOV10 | STI21 | STI20 | STI11 | STI10 |   |  |

## Register Description

For all interrupts in the STI register the following logical states are applied

- 0 = Interrupt has not occurred
- 1 = Interrupt has occurred

### **STOVxy** Synchronous Transfer Overflow Interrupt

Enabled STOV interrupts for a certain STIxy interrupt are generated when the STIxy has not been acknowledged in time via the ACKxy bit in the ASTI register. This must be one (for DPS = '0') or zero (for DPS = '1') BCL clock cycles before the time slot which is selected for the STOV.

### **STIxy** Synchronous Transfer Interrupt

Depending on the DPS bit in the corresponding TSDPxy register the Synchronous Transfer Interrupt STIxy is generated two (for DPS = '0') or one (for DPS = '1') BCL clock cycles after the selected time slot (TSDPxy.TSS).

Note: STOVxy and ACKxy are useful for synchronizing microcontroller accesses and receive/transmit operations. One BCL clock is equivalent to two DCL clocks.

## 4.7.12 ASTI - Acknowledge Synchronous Transfer Interrupt

**ASTI** write Address: 58<sub>H</sub>  
Value after reset: 00<sub>H</sub>

|   |   |   |   |       |       |       |       |
|---|---|---|---|-------|-------|-------|-------|
| 7 |   |   |   | 0     |       |       |       |
| 0 | 0 | 0 | 0 | ACK21 | ACK20 | ACK11 | ACK10 |

### **ACKxy** Acknowledge Synchronous Transfer Interrupt

After a STIxy interrupt the microcontroller has to acknowledge the interrupt by setting the corresponding ACKxy bit.

- 0 = No activity is initiated
- 1 = Sets the acknowledge bit ACKxy for a STIxy interrupt

## Register Description

### 4.7.13 MSTI - Mask Synchronous Transfer Interrupt

**MSTI** read/write Address: 59<sub>H</sub>

Value after reset: FF<sub>H</sub>

|        |        |        |        |       |       |       |       |
|--------|--------|--------|--------|-------|-------|-------|-------|
| 7      |        |        |        |       |       |       | 0     |
| STOV21 | STOV20 | STOV11 | STOV10 | STI21 | STI20 | STI11 | STI10 |

For the MSTI register the following logical states are applied:

0 = Interrupt is not masked

1 = Interrupt is masked

**STOVxy** Mask Synchronous Transfer Overflow xy  
Mask bits for the corresponding STOVxy interrupt bits.

**STIxy** Synchronous Transfer Interrupt xy  
Mask bits for the corresponding STIxy interrupt bits.

## 4.8 Detailed MONITOR Handler Registers

### 4.8.1 MOR - MONITOR Receive Channel

**MOR** read Address: 5C<sub>H</sub>

Value after reset: FF<sub>H</sub>

|   |  |  |  |  |  |  |   |
|---|--|--|--|--|--|--|---|
| 7 |  |  |  |  |  |  | 0 |
|   |  |  |  |  |  |  |   |

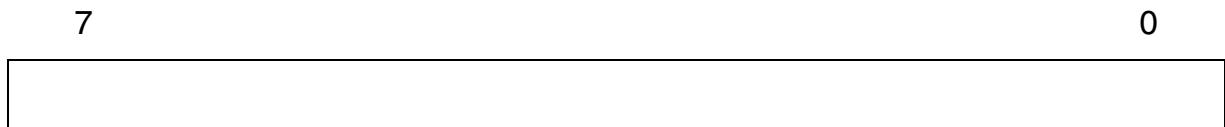
Contains the MONITOR data received in the IOM<sup>®</sup>-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON\_CR.MCS.

## Register Description

### 4.8.2 MOX - MONITOR Transmit Channel

**MOX** write Address: 5C<sub>H</sub>

Value after reset: FF<sub>H</sub>

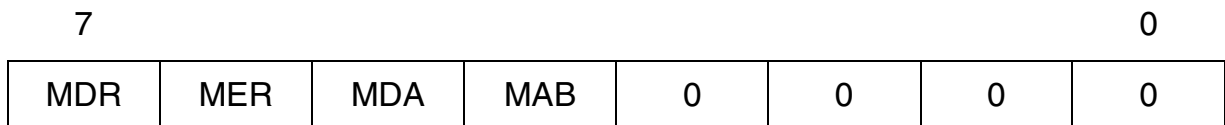


Contains the MONITOR data to be transmitted in IOM<sup>®</sup>-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON\_CR.MCS

### 4.8.3 MOSR - MONITOR Interrupt Status Register

**MOSR** read Address: 5D<sub>H</sub>

Value after reset: 00<sub>H</sub>



**MDR** MONITOR channel Data Received

0 = inactive

1 = MONITOR channel Data Received

**MER** MONITOR channel End of Reception

0 = inactive

1 = MONITOR channel End of Reception

**MDA** MONITOR channel Data Acknowledged

The remote end has acknowledged the MONITOR byte being transmitted.

0 = inactive

1 = MONITOR channel Data Acknowledged

**MAB** MONITOR channel Data Abort

## Register Description

- 0 = inactive  
1 = MONITOR channel Data Abort

### 4.8.4 MOCR - MONITOR Control Register

**MOCR** read/write Address: 5E<sub>H</sub>

Value after reset: 00<sub>H</sub>

|     |     |     |     |   |   |   |   |
|-----|-----|-----|-----|---|---|---|---|
| 7   |     |     |     |   |   |   | 0 |
| MRE | MRC | MIE | MXC | 0 | 0 | 0 | 0 |

**MRE** MONITOR Receive Interrupt Enable

- 0 = MONITOR interrupt status MDR generation is masked.  
1 = MONITOR interrupt status MDR generation is enabled.

**MRC** MR Bit Control

Determines the value of the MR bit:

- 0 = MR is always '1'. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRE = 1).  
1 = MR is internally controlled by the T-SMINT<sup>®</sup>I according to MONITOR channel protocol. In addition, the MDR interrupt is enabled for all received bytes according to the MONITOR channel protocol (if MRE = 1).

**MIE** MONITOR Interrupt Enable

- 0 = MONITOR interrupt status MER, MDA, MAB generation is masked  
1 = MONITOR interrupt status MER, MDA, MAB generation is enabled

**MXC** MX Bit Control

Determines the value of the MX bit:

- 0 = The MX bit is always '1'.  
1 = The MX bit is internally controlled by the T-SMINT<sup>®</sup>I according to MONITOR channel protocol.

## Register Description

### 4.8.5 MSTA - MONITOR Status Register

**MSTA** read Address: 5F<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |   |   |   |   |     |      |
|---|---|---|---|---|-----|------|
| 7 |   |   |   |   |     | 0    |
| 0 | 0 | 0 | 0 | 0 | MAC | TOUT |

**MAC** MONITOR Transmit Channel Active

0 = No data transmission in the MONITOR channel

1 = The data transmission in the MONITOR channel is in progress.

**TOUT** Time-Out

Read-back value of the TOUT bit

0 = The monitor time-out function is disabled

1 = The monitor time-out function is enabled

### 4.8.6 MCONF - MONITOR Configuration Register

**MCONF** write Address: 5F<sub>H</sub>

Value after reset: 00<sub>H</sub>

|   |   |   |   |   |   |      |
|---|---|---|---|---|---|------|
| 7 |   |   |   |   |   | 0    |
| 0 | 0 | 0 | 0 | 0 | 0 | TOUT |

**TOUT** Time-Out

0 = The monitor time-out function is disabled

1 = The monitor time-out function is enabled

## Register Description

### 4.9 Detailed U-Transceiver Registers

#### 4.9.1 OPMODE - Operation Mode Register

The **Operation Mode** register determines the operating mode of the U-transceiver.

**OPMODE** read\*/write Address: 60<sub>H</sub>

Reset value: 00<sub>H</sub>

| 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
|---|-----|---|---|---|---|---|---|
| 0 | UCI | 0 | 0 | 0 | 0 | 0 | 0 |

**UCI** Enable/Disable  $\mu$ P-control of C/I codes

0 =  $\mu$ P control disabled - C/I codes are exchanged via IOM<sup>®</sup>-2  
Read access to register UCIR by the  $\mu$ P is still possible

1 =  $\mu$ P control enabled - C/I codes are exchanged via UCIR and UCIW registers  
In this case, the according C/I-channel on IOM<sup>®</sup>-2 is idle '1111'

#### 4.9.2 UCIR - C/I Code Read Register

Via the **U-transceiver C/I code Read** register a microcontroller can access the C/I code that is output from the state machine.

**UCIR** read Address: 6D<sub>H</sub>

Reset value: 00<sub>H</sub>

| 7 | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|---|---|---|---|-----------------|---|---|---|
| 0 | 0 | 0 | 0 | C/I code output |   |   |   |

#### 4.9.3 UCIW - C/I Code Write Register

The **U-transceiver C/I code Write** register allows a microcontroller to control the state of the U-transceiver. To enable this function bit UCI in register OPMODE must be set to '1' before.

## Register Description

**UCIW**

**write**

Address: 6E<sub>H</sub>

Reset value: 01<sub>H</sub>

| 7 | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
|---|---|---|---|----------------|---|---|---|
| 0 | 0 | 0 | 0 | C/I code input |   |   |   |

### 4.9.4 LOOP - Loopback Register

The **Loop** register controls local digital loopbacks of the U-transceiver.

**LOOP**

read<sup>\*)</sup>/write

Address: 70<sub>H</sub>

Reset value: 08<sub>H</sub>

| 7 | 6 | 5         | 4     | 3 | 2    | 1   | 0   |
|---|---|-----------|-------|---|------|-----|-----|
| 0 | 0 | TRAN<br>S | U/IOM | 1 | LBBD | LB2 | LB1 |

#### **TRANS** Transparent/ Non-Transparent Loopback

In transparent mode data is both passed on and looped back, whereas in non-transparent mode data is not forwarded but substituted by 1s (idle code) and just looped back

0 = transparent mode

1 = non-transparent mode

'1's are sent on the IOM<sup>®</sup>-2 interface in the corresponding time-slot

#### **U/IOM<sup>®</sup>**

Close LBBD, LB2, LB1 towards U or towards IOM<sup>®</sup>

Switch that selects whether loopback LB1, LB2 or LBBD is closed towards U or towards IOM<sup>®</sup>-2

the setting affects all test loops, LBBD, LB2 and LB1

an individual selection for LBBD, LB2, LB1 is not possible

0 = LB1, LB2, LBBD loops are closed towards IOM<sup>®</sup>

1 = LB1, LB2, LBBD loops are closed towards U

## Register Description

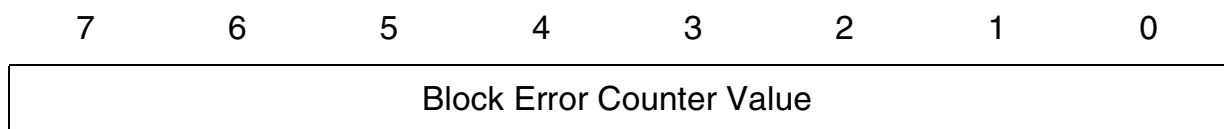
- LBBD** Close complete loop (B1, B2, D) near the system interface
- the direction towards which the loop is closed is determined by bit U/IOM<sup>®</sup>
  - the state machine has to be in state 'Transparent' first (e.g. by C/I = DT) before data is output on the U-interface
- 0 = complete loopback open  
1 = complete loopback closed
- LB2** Close loop B2 near the system interface
- the direction towards which the loop is closed is determined by bit U/IOM<sup>®</sup>
  - the state machine has to be in state 'Transparent' first (e.g. by C/I = DT) before data is output on the U-interface
- 0 = loopback B2 open  
1 = loopback B2 closed
- LB1** Close loop B1 near the system interface
- the direction towards which the loop is closed is determined by bit U/IOM<sup>®</sup>
  - the state machine has to be in state 'Transparent' first (e.g. by C/I = DT) before data is output on the U-interface
- 0 = loopback B1 open  
1 = loopback B1 closed

### 4.9.5 RDS - Block Error Counter Register

see [Chapter 2.4.4.2](#).

**RDS** **read** Address: 72<sub>H</sub>

Reset value: 00<sub>H</sub>



### 4.9.6 ISTAU - Interrupt Status Register U-Interface

The Interrupt **Status** register **U**-interface generates an interrupt for the unmasked interrupt flags. Refer to [Chapter 2.4.8](#) for details on masking and clearing of interrupt flags.

## Register Description

**ISTAU**

**read**

Address: 7A<sub>H</sub>

Reset value: 00<sub>H</sub>

| 7 | 6  | 5   | 4 | 3 | 2 | 1 | 0    |
|---|----|-----|---|---|---|---|------|
| 0 | CI | RDS | 0 | 0 | 0 | 0 | 1 ms |

**CI** C/I code indication  
the CI interrupt is generated independently on OPMODE.UCI

0 = inactive

1 = CI code change has occurred

**RDS** Code violation occurred

0 = inactive

1 = code violation has occurred

**1 ms** Start of a new frame on the U-interface  
useful for synchronization of register accesses by an external  $\mu$ C

0 = inactive

1 = signals the start of a new frame on the U-interface

### 4.9.7 MASKU - Mask Register U-Interface

The Interrupt **Mask** register **U-Interface** selectively masks each interrupt source in the ISTAU register by setting the corresponding bit to '1'.

**MASKU**

read<sup>\*)</sup>/write

Address: 7B<sub>H</sub>

Reset Value: FF<sub>H</sub>

| 7 | 6  | 5   | 4 | 3 | 2 | 1 | 0    |
|---|----|-----|---|---|---|---|------|
| 1 | CI | RDS | 1 | 1 | 1 | 1 | 1 ms |

## Register Description

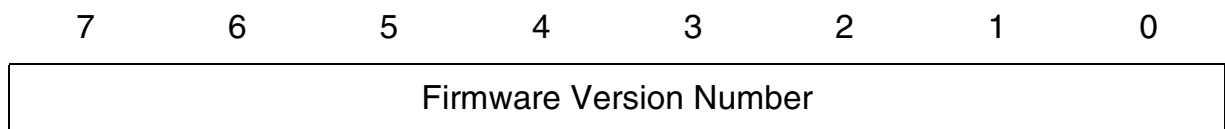
**Bit 0..7** Mask bits  
 0 = interrupt active  
 1 = interrupt masked

### 4.9.8 FW\_VERSION

FW\_VERSION Register contains the Firmware Version number

**FW\_VERSION** **read** Address: 7D<sub>H</sub>

Reset value: 3E<sub>H</sub>



## Electrical Characteristics

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

| Parameter                                         | Symbol    | Limit Values                           | Unit |
|---------------------------------------------------|-----------|----------------------------------------|------|
| Ambient temperature under bias                    | $T_A$     | -40 to 85                              | °C   |
| Storage temperature                               | $T_{STG}$ | – 65 to 150                            | °C   |
| Maximum Voltage on $V_{DD}$                       | $V_{DD}$  | 4.2                                    | V    |
| Maximum Voltage on any pin with respect to ground | $V_S$     | -0.3 to $V_{DD} + 3.3$<br>(max. < 5.5) | V    |

ESD integrity (according EIA/JESD22-A114B (HBM)): 2 kV

*Note: Stress above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.*

### Line Overload Protection

The T-SMINT<sup>®</sup>I is compliant to ESD tests according to ANSI / EOS / ESD-S 5.1-1993 (CDM), EIA/JESD22-A114B (HBM) and to Latch-up tests according to JEDEC EIA / JESD78. From these tests the following max. input currents are derived ([Table 33](#)):

**Table 33 Maximum Input Currents**

| Test     | Pulse Width | Current   | Remarks                     |
|----------|-------------|-----------|-----------------------------|
| ESD      | 100 ns      | 1.3 A     | 3 repetitions               |
| Latch-up | 5 ms        | +/-200 mA | 2 repetitions, respectively |
| DC       | --          | 10 mA     |                             |

## Electrical Characteristics

### 5.2 DC Characteristics

$V_{DD}/V_{DDA} = 3.3 \text{ V} \pm 5\%$  ;  $V_{SS}/V_{SSA} = 0 \text{ V}$  ;  $T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$

| Digital Pins                          | Parameter                             | Symbol    | Limit Values |      | Unit          | Test Condition                          |
|---------------------------------------|---------------------------------------|-----------|--------------|------|---------------|-----------------------------------------|
|                                       |                                       |           | min.         | max. |               |                                         |
| All                                   | Input low voltage                     | $V_{IL}$  | -0.3         | 0.8  | V             |                                         |
|                                       | Input high voltage                    | $V_{IH}$  | 2.0          | 5.25 | V             |                                         |
| All except DD/DU<br>ACT, LP2I<br>MCLK | Output low voltage                    | $V_{OL1}$ |              | 0.45 | V             | $I_{OL1} = 3.0 \text{ mA}$              |
|                                       | Output high voltage                   | $V_{OH1}$ | 2.4          |      | V             | $I_{OH1} = 3.0 \text{ mA}$              |
| DD/DU<br>ACT, LP2I<br>MCLK            | Output low voltage                    | $V_{OL2}$ |              | 0.45 | V             | $I_{OL2} = 4.0 \text{ mA}$              |
|                                       | Output high voltage (DD/DU push-pull) | $V_{OH2}$ | 2.4          |      | V             | $I_{OH2} = 4.0 \text{ mA}$              |
| All                                   | Input leakage current                 | $I_{LI}$  |              | 10   | $\mu\text{A}$ | $0 \text{ V} \leq V_{IN} \leq V_{DD}$   |
|                                       | Output leakage current                | $I_{LO}$  |              | 10   | $\mu\text{A}$ | $0 \text{ V} \leq V_{IN} \leq V_{DD}$   |
| <b>Analog Pins</b>                    |                                       |           |              |      |               |                                         |
| AIN, BIN                              | Input leakage current                 | $I_{LI}$  |              | 30   | $\mu\text{A}$ | $0 \text{ V} \leq V_{IN} \leq V_D$<br>D |

**Table 34 S-Transceiver Characteristics**

| Pin   | Parameter                                                        | Symbol | Limit Values |      |      | Unit                  | Test Condition                                     |
|-------|------------------------------------------------------------------|--------|--------------|------|------|-----------------------|----------------------------------------------------|
|       |                                                                  |        | min.         | typ. | max. |                       |                                                    |
| SX1,2 | Absolute value of output pulse amplitude ( $V_{SX2} - V_{SX1}$ ) | $V_X$  | 2.03         | 2.2  | 2.31 | V                     | $R_L = 50 \Omega$                                  |
| SX1,2 | S-Transmitter output impedance                                   | $Z_X$  | 10           | 34   |      | $k\Omega$             | see <sup>1)</sup>                                  |
|       |                                                                  |        | 0            |      |      |                       | see <sup>2)3)</sup>                                |
| SR1,2 | S-Receiver input impedance                                       | $Z_R$  | 10<br>100    |      |      | $k\Omega$<br>$\Omega$ | $V_{DD} = 3.3 \text{ V}$<br>$V_{DD} = 0 \text{ V}$ |

<sup>1)</sup> Requirement ITU-T I.430, chapter 8.5.1.1a): 'At all times except when transmitting a binary zero, the output impedance, in the frequency range of 2kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 11. The requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s value)'

## Electrical Characteristics

- 2) Requirement ITU-T I.430, chapter 8.5.1.1b): 'When transmitting a binary zero, the output impedance shall be  $> 20 \Omega$ .' Must be met by external circuitry.
- 3) Requirement ITU-T I.430, chapter 8.5.1.1b), Note: 'The output impedance limit shall apply for a nominal load impedance (resistive) of  $50 \Omega$ . The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value  $\pm 10\%$ . The peak amplitude shall be defined as the the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.'

**Table 35 U-Transceiver Characteristics**

|                                                                                                      | Limit Values     |          |          | Unit            |
|------------------------------------------------------------------------------------------------------|------------------|----------|----------|-----------------|
|                                                                                                      | min.             | typ.     | max.     |                 |
| Receive Path                                                                                         |                  |          |          |                 |
| Signal / (noise + total harmonic distortion) <sup>1)</sup>                                           | 65 <sup>2)</sup> |          |          | dB              |
| DC-level at AD-output                                                                                | 45               | 50       | 55       | % <sup>3)</sup> |
| Threshold of level detect<br>(measured between AIN and BIN with<br>respect to zero signal)           | 10               |          | 23       | mV<br>peak      |
| Input impedance AIN/BIN                                                                              | 80               |          |          | kΩ              |
| Transmit Path                                                                                        |                  |          |          |                 |
| Signal / (noise + total harmonic distortion) <sup>4)</sup>                                           | 70               |          |          | dB              |
| Common mode DC-level                                                                                 | 1.61             | 1.65     | 1.69     | V               |
| Offset between AOUT and BOUT                                                                         |                  |          | 35       | mV              |
| Absolute peak voltage for a single +3 or -3<br>pulse measured between AOUT and<br>BOUT <sup>5)</sup> | 2.42             | 2.5      | 2.58     | V               |
| Output impedance AOUT/BOUT:<br>Power-up<br>Power-down                                                |                  | 0.8<br>3 | 1.5<br>6 | Ω<br>Ω          |

<sup>1)</sup> Test conditions: 1.4 Vpp differential sine wave as input on AIN/BIN with long range (low, critical range).

<sup>2)</sup> Versions PEF 8x913 with enhanced performance of the U-interface are tested with tightened limit values

<sup>3)</sup> The percentage of the "1"-values in the PDM-signal.

<sup>4)</sup> Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 70 dB below the signal for an evenly distributed but otherwise random sequence of +3, +1, -1, -3.

<sup>5)</sup> The signal amplitude measured over a period of 1 min. varies less than 1%.

## Electrical Characteristics

### 5.3 Capacitances

$T_A = 25\text{ °C}$ ,  $3.3\text{ V} \pm 5\%$   $V_{SSA} = 0\text{ V}$ ,  $V_{SSD} = 0\text{ V}$ ,  $f_c = 1\text{ MHz}$ , unmeasured pins grounded.

**Table 36 Pin Capacitances**

| Parameter                          | Symbol    | Limit Values |      | Unit | Remarks      |
|------------------------------------|-----------|--------------|------|------|--------------|
|                                    |           | min.         | max. |      |              |
| Digital pads:<br>Input Capacitance | $C_{IN}$  |              | 7    | pF   |              |
| I/O Capacitance                    | $C_{I/O}$ |              | 7    | pF   |              |
| Analog pads:<br>Load Capacitance   | $C_L$     |              | 3    | pF   | pin AIN, BIN |

### 5.4 Power Consumption

#### Power Consumption

$V_{DD}=3.3\text{ V}$ ,  $V_{SS}=0\text{ V}$ , Inputs at  $V_{SS}/V_{DD}$ , no LED connected, 50% bin. zeros, no output loads except SX1,2 ( $50\text{ }\Omega$ <sup>1)</sup>)

| Parameter                                               | Limit Values |      |      | Unit | Test Condition                |
|---------------------------------------------------------|--------------|------|------|------|-------------------------------|
|                                                         | min.         | typ. | max. |      |                               |
| Operational<br>U and S enabled, IOM <sup>®</sup> -2 off |              | 185  |      | mW   | U: ETSI loop 1 (0 m)          |
|                                                         |              | 165  |      | mW   | U: ETSI Loop 2.(typical line) |
| Power Down                                              |              | 15   |      | mW   |                               |

<sup>1)</sup>  $50\text{ }\Omega$  (2 x TR) on the S-bus.

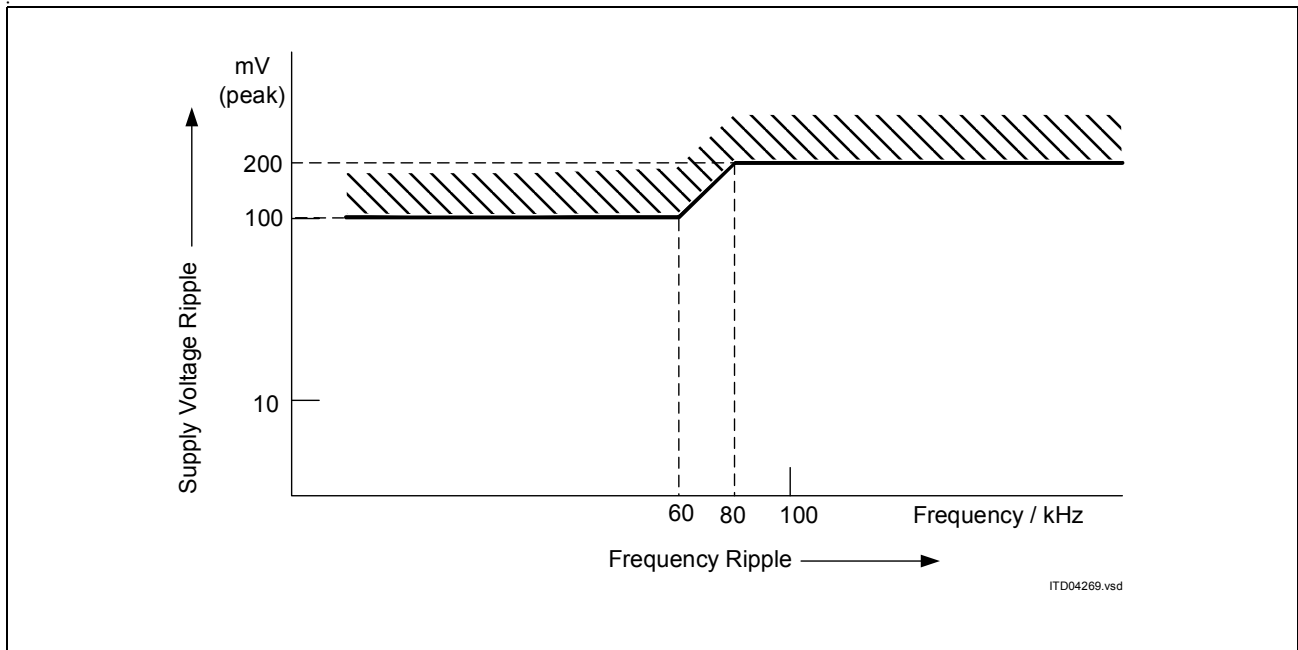
### 5.5 Supply Voltages

$$V_{DD_D} = + V_{dd} \pm 5\%$$

$$V_{DD_A} = + V_{dd} \pm 5\%$$

The maximum sinusoidal ripple on  $V_{DD}$  is specified in the following figure:

## Electrical Characteristics



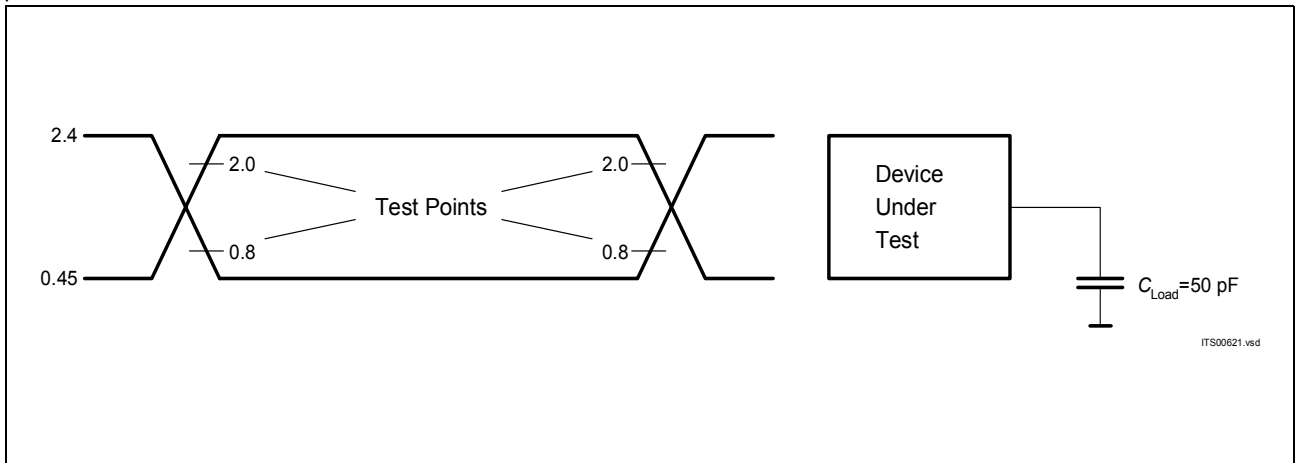
**Figure 60 Maximum Sinusoidal Ripple on Supply Voltage**

## Electrical Characteristics

### 5.6 AC Characteristics

$T_A = -40$  to  $85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 5\%$

Inputs are driven to  $2.4\text{ V}$  for a logical "1" and to  $0.4\text{ V}$  for a logical "0". Timing measurements are made at  $2.0\text{ V}$  for a logical "1" and  $0.8\text{ V}$  for a logical "0". The AC testing input/output waveforms are shown in **Figure 61**.

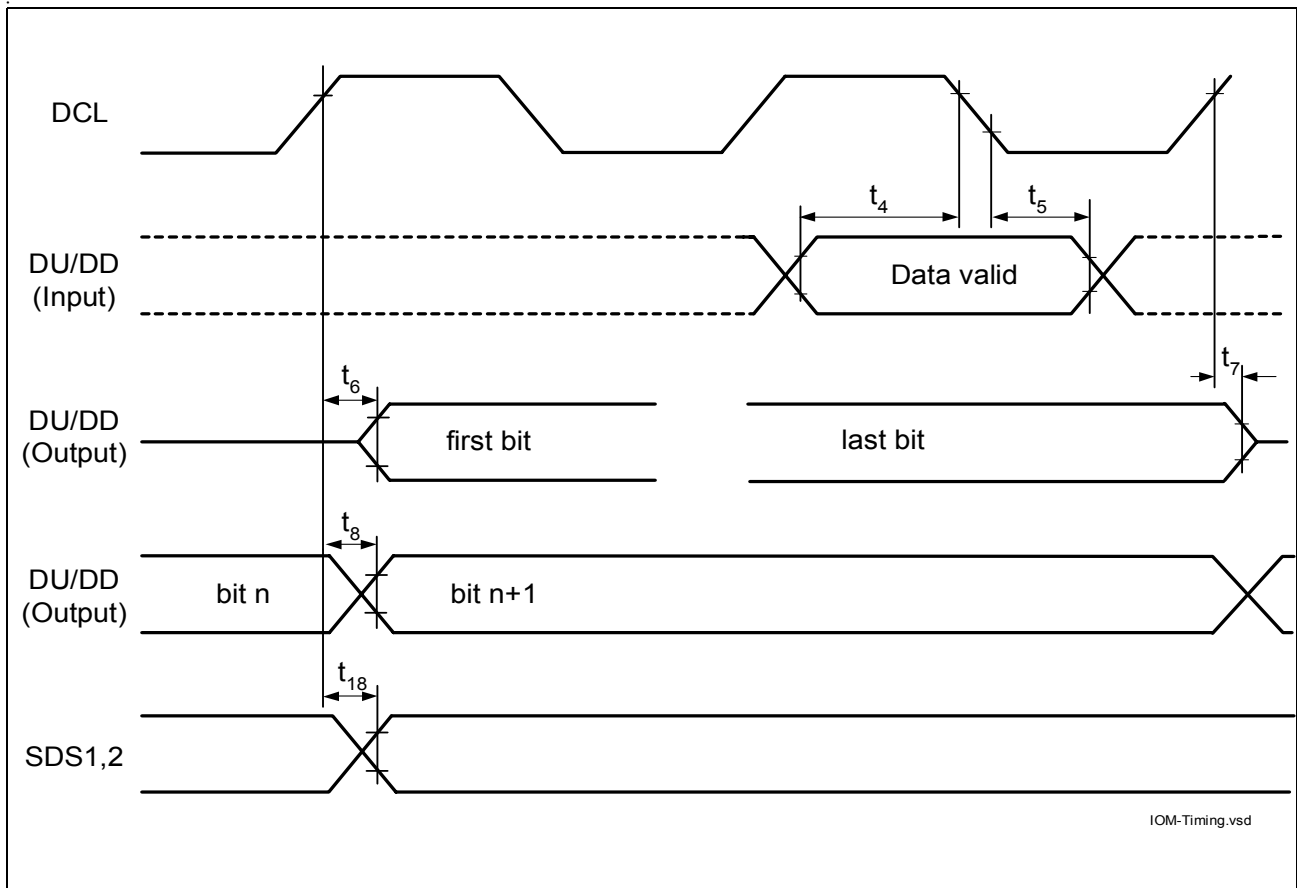


**Figure 61 Input/Output Waveform for AC Tests**

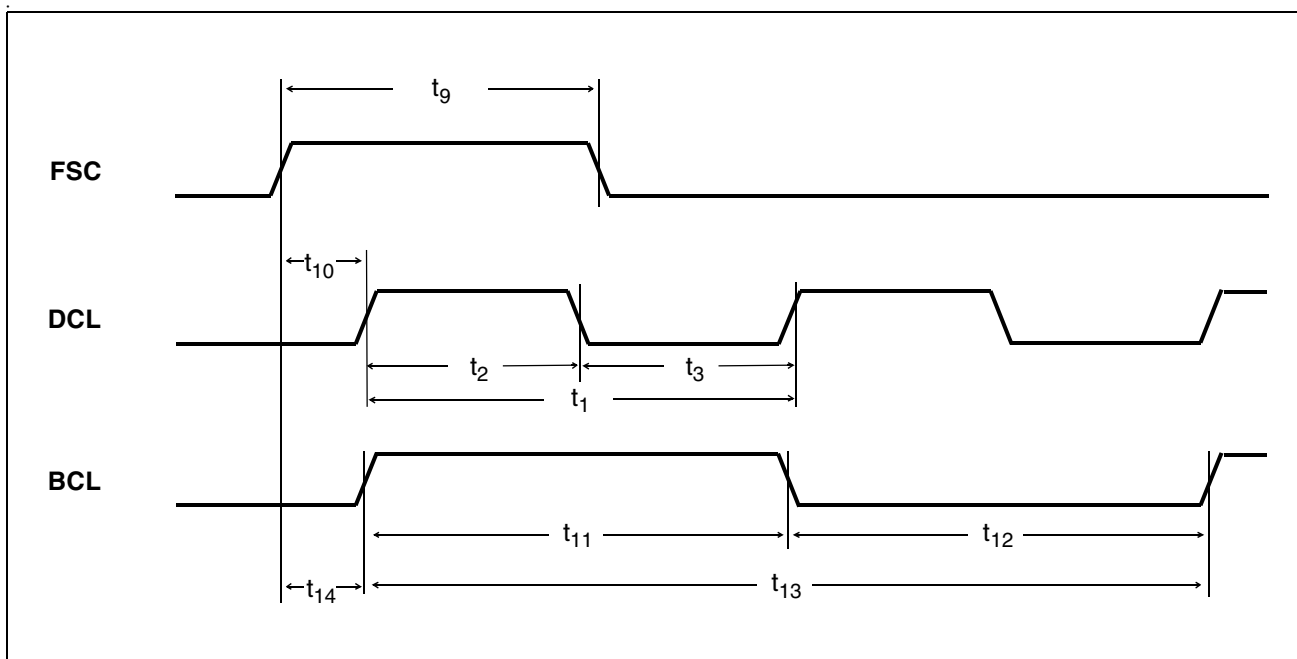
| Parameter<br>All Output Pins | Symbol | Limit values |     | Unit |
|------------------------------|--------|--------------|-----|------|
|                              |        | Min          | Max |      |
| Fall time                    |        |              | 30  | ns   |
| Rise time                    |        |              | 30  | ns   |

## Electrical Characteristics

### 5.6.1 IOM<sup>®</sup>-2 Interface



**Figure 62 IOM<sup>®</sup>-2 Interface - Bit Synchronization Timing**



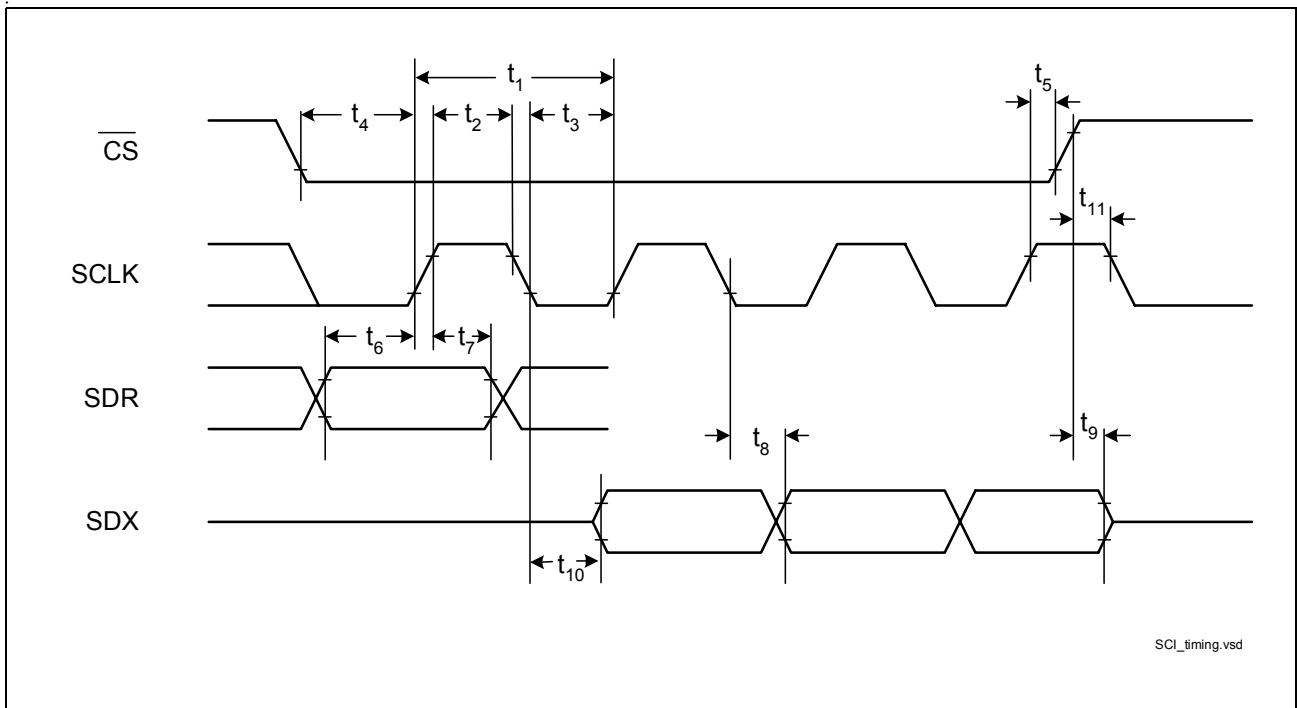
**Figure 63 IOM<sup>®</sup>-2 Interface - Frame Synchronization Timing**

**Electrical Characteristics**

| Parameter<br>IOM <sup>®</sup> -2 Interface                                           | Symbol   | Limit values |                       |      | Unit |
|--------------------------------------------------------------------------------------|----------|--------------|-----------------------|------|------|
|                                                                                      |          | Min          | Typ                   | Max  |      |
| DCL period                                                                           | $t_1$    | 565          | 651                   | 735  | ns   |
| DCL high                                                                             | $t_2$    | 200          | 310                   | 420  | ns   |
| DCL low                                                                              | $t_3$    | 200          | 310                   | 420  | ns   |
| Input data setup                                                                     | $t_4$    | 20           |                       |      | ns   |
| Input data hold                                                                      | $t_5$    | 20           |                       |      | ns   |
| Output data from high impedance to active<br>(FSC high or other than first timeslot) | $t_6$    |              |                       | 100  | ns   |
| Output data from active to high impedance                                            | $t_7$    |              |                       | 100  | ns   |
| Output data delay from clock                                                         | $t_8$    |              |                       | 80   | ns   |
| FSC high                                                                             | $t_9$    |              | 50% of FSC cycle time |      | ns   |
| FSC advance to DCL                                                                   | $t_{10}$ | 65           | 130                   | 195  | ns   |
| BCL high                                                                             | $t_{11}$ | 565          | 651                   | 735  | ns   |
| BCL low                                                                              | $t_{12}$ | 565          | 651                   | 735  | ns   |
| BCL period                                                                           | $t_{13}$ | 1130         | 1302                  | 1470 | ns   |
| FSC advance to BCL                                                                   | $t_{14}$ | 65           | 130                   | 195  | ns   |
| DCL, FSC rise/fall                                                                   | $t_{15}$ |              |                       | 30   | ns   |
| Data out fall ( $C_L = 50$ pF, $R = 2$ k $\Omega$ to $V_{DD}$ , open drain)          | $t_{16}$ |              |                       | 200  | ns   |
| Data out rise/fall ( $C_L = 50$ pF, tristate)                                        | $t_{17}$ |              |                       | 150  | ns   |
| Strobe Signal Delay                                                                  | $t_{18}$ |              |                       | 120  | ns   |

*Note: At the start and end of a reset period, a frame jump may occur. This results in a DCL, BCL and FSC high time of min. 130 ns after this specific event.*

## 5.6.2 Serial $\mu$ P Interface

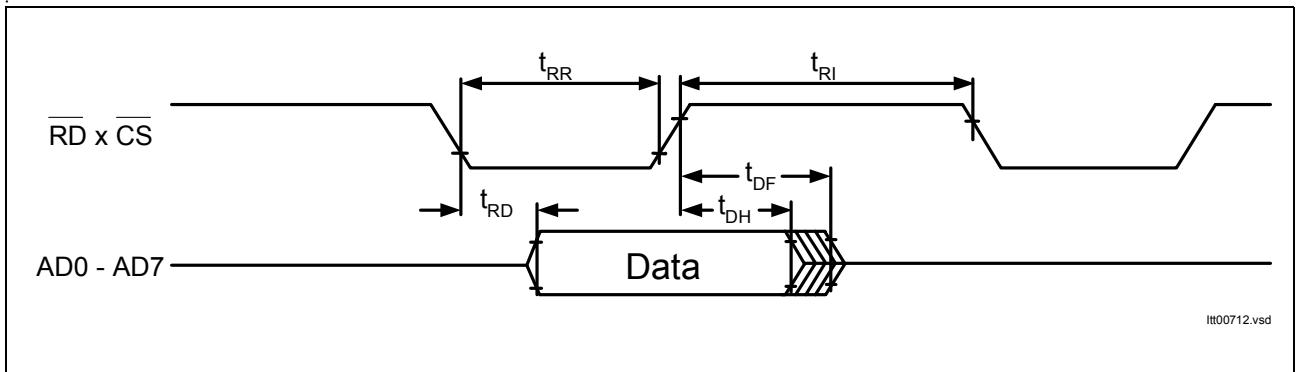


**Figure 64 Serial Control Interface**

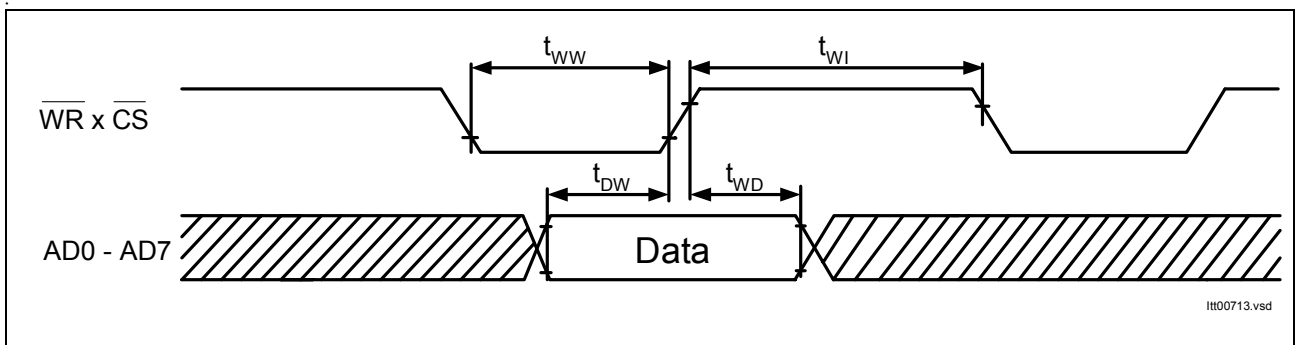
| Parameter<br>SCI Interface                  | Symbol   | Limit values |     | Unit |
|---------------------------------------------|----------|--------------|-----|------|
|                                             |          | Min          | Max |      |
| SCLK cycle time                             | $t_1$    | 200          |     | ns   |
| SCLK high time                              | $t_2$    | 80           |     | ns   |
| SCLK low time                               | $t_3$    | 80           |     | ns   |
| $\overline{\text{CS}}$ setup time           | $t_4$    | 20           |     | ns   |
| $\overline{\text{CS}}$ hold time            | $t_5$    | 10           |     | ns   |
| SDR setup time                              | $t_6$    | 15           |     | ns   |
| SDR hold time                               | $t_7$    | 15           |     | ns   |
| SDX data out delay                          | $t_8$    |              | 60  | ns   |
| $\overline{\text{CS}}$ high to SDX tristate | $t_9$    |              | 40  | ns   |
| SCLK to SDX active                          | $t_{10}$ |              | 60  | ns   |
| $\overline{\text{CS}}$ high to SCLK         | $t_{11}$ | 10           |     | ns   |

### 5.6.3 Parallel $\mu$ P Interface

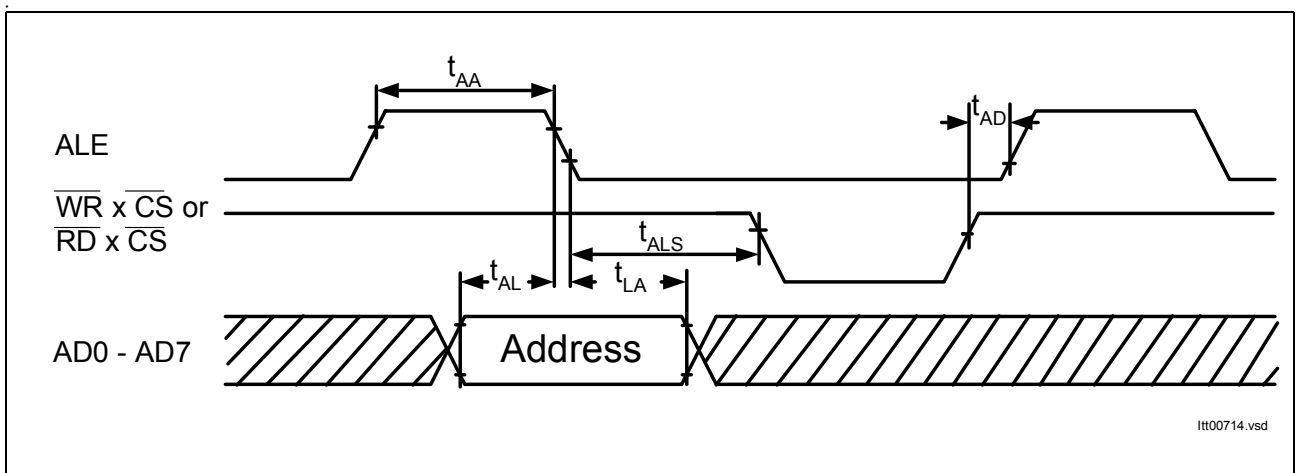
#### Siemens/Intel Bus Mode



**Figure 65 Microprocessor Read Cycle**

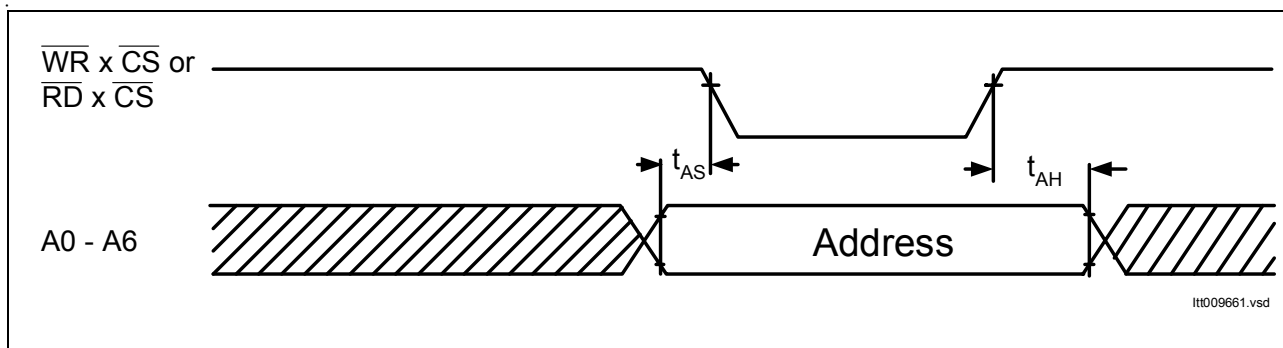


**Figure 66 Microprocessor Write Cycle**



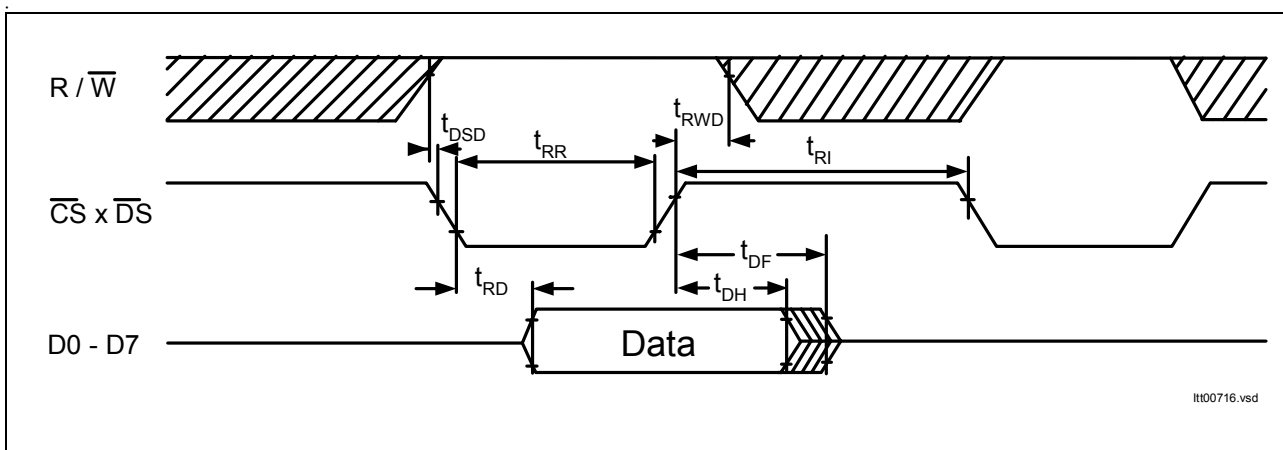
**Figure 67 Multiplexed Address Timing**

## Electrical Characteristics

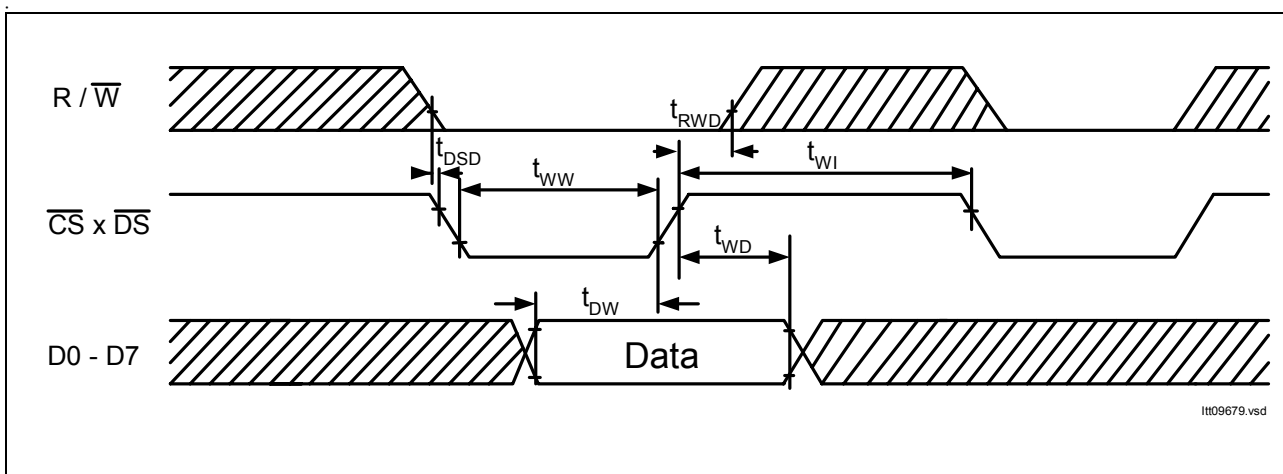


**Figure 68** Non-Multiplexed Address Timing

### Motorola Bus Mode

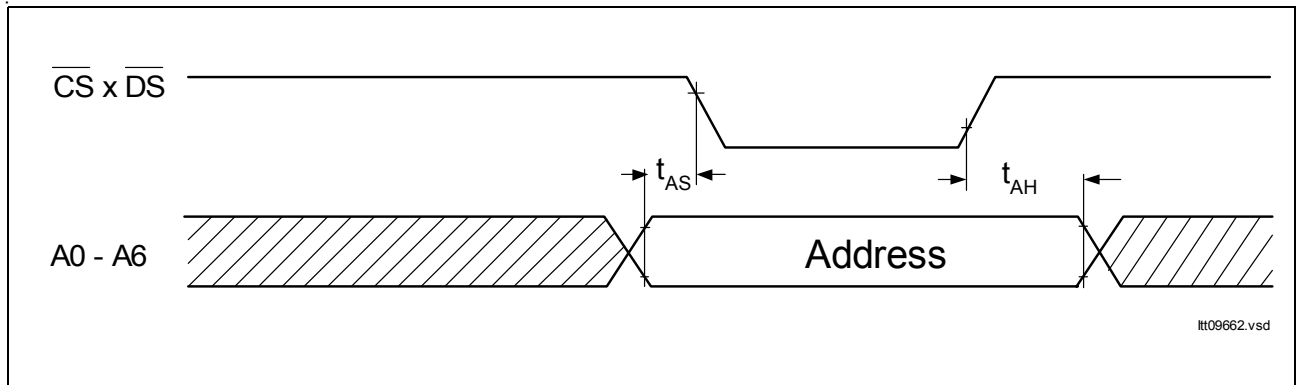


**Figure 69** Microprocessor Read Timing



**Figure 70** Microprocessor Write Cycle

## Electrical Characteristics



**Figure 71 Non-Multiplexed Address Timing**

### Microprocessor Interface Timing

| Parameter                                                                | Symbol    | Limit Values |      | Unit |
|--------------------------------------------------------------------------|-----------|--------------|------|------|
|                                                                          |           | min.         | max. |      |
| ALE pulse width                                                          | $t_{AA}$  | 20           |      | ns   |
| Address setup time to ALE                                                | $t_{AL}$  | 10           |      | ns   |
| Address hold time from ALE                                               | $t_{LA}$  | 10           |      | ns   |
| Address latch setup time to $\overline{WR}$ , $\overline{RD}$            | $t_{ALS}$ | 10           |      | ns   |
| Address setup time                                                       | $t_{AS}$  | 10           |      | ns   |
| Address hold time                                                        | $t_{AH}$  | 10           |      | ns   |
| ALE guard time                                                           | $t_{AD}$  | 10           |      | ns   |
| $\overline{DS}$ delay after $R/\overline{W}$ setup                       | $t_{DSD}$ | 10           |      | ns   |
| $\overline{RD}$ pulse width                                              | $t_{RR}$  | 80           |      | ns   |
| Data output delay from $\overline{RD}$                                   | $t_{RD}$  |              | 80   | ns   |
| Data hold from $\overline{RD}$                                           | $t_{DH}$  | 0            |      | ns   |
| Data float from $\overline{RD}$                                          | $t_{DF}$  |              | 25   | ns   |
| $\overline{RD}$ control interval <sup>1)</sup>                           | $t_{RI}$  | 70           |      | ns   |
| $\overline{W}$ pulse width                                               | $t_{WW}$  | 60           |      | ns   |
| Data setup time to $\overline{W} \times \overline{CS}$                   | $t_{DW}$  | 10           |      | ns   |
| Data hold time $\overline{W} \times \overline{CS}$                       | $t_{WD}$  | 10           |      | ns   |
| $\overline{W}$ control interval                                          | $t_{WI}$  | 70           |      | ns   |
| $R/\overline{W}$ hold from $\overline{CS} \times \overline{DS}$ inactive | $t_{RWD}$ | 10           |      | ns   |

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## Electrical Characteristics

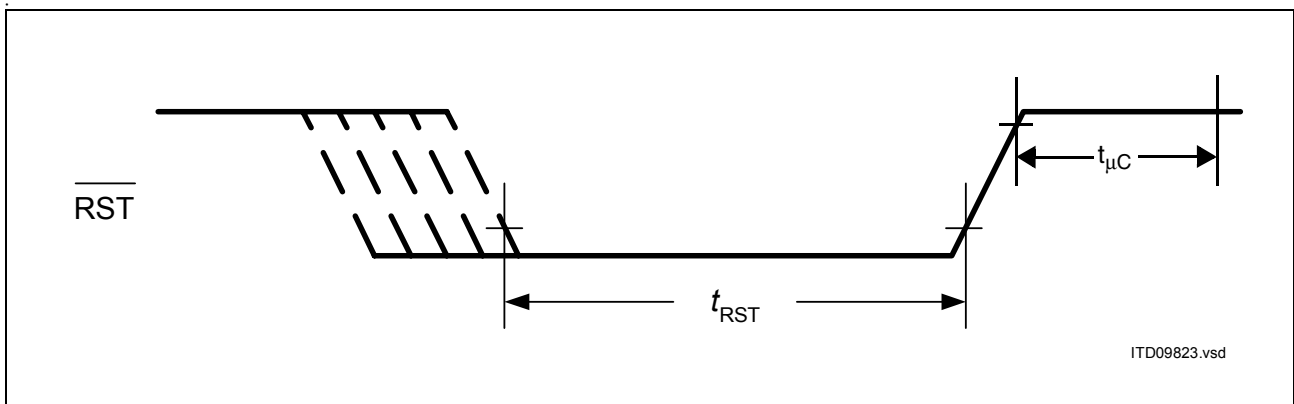
- <sup>1)</sup> control interval:  $t_{RI}$  is minimal 70ns for all registers except ISTAU, FEBE and NEBE. However, the time between two consecutive read accesses to one of the registers ISTAU, FEBE or NEBE, respectively, must be longer than 330ns. This does not limit  $t_{RI}$  of read sequences, which involve intermediate read access to other registers, as for instance: ISTAU -( $t_{RI}$ )- ISTA -( $t_{RI}$ )- ISTAH -( $t_{RI}$ )- ISTAU.

## Electrical Characteristics

### 5.6.4 Reset

**Table 37**      **Reset Input Signal Characteristics**

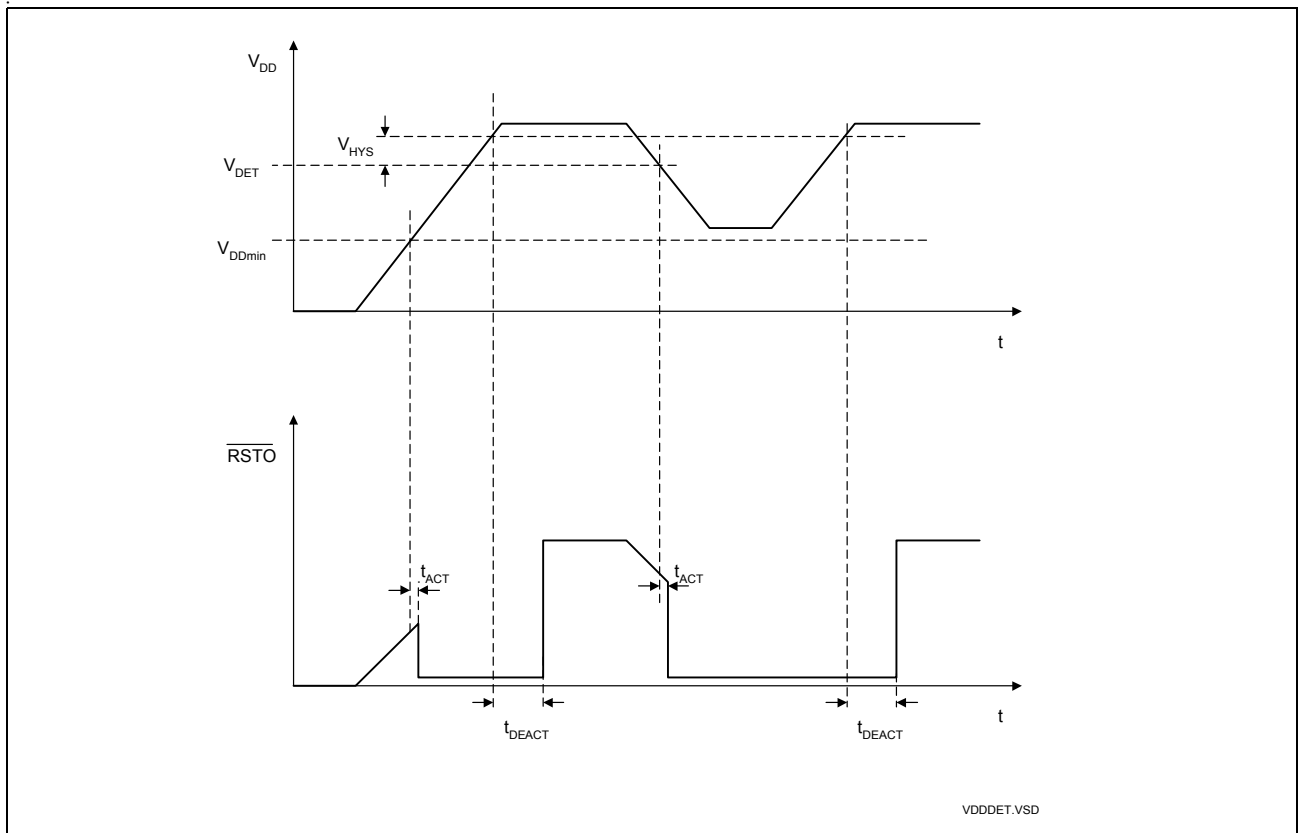
| Parameter                                                                     | Symbol                      | Limit Values                  |      |      | Unit | Test Conditions                                                                        |
|-------------------------------------------------------------------------------|-----------------------------|-------------------------------|------|------|------|----------------------------------------------------------------------------------------|
|                                                                               |                             | min.                          | typ. | max. |      |                                                                                        |
| Length of active low state                                                    | $t_{\overline{\text{RST}}}$ | 4                             |      |      | ms   | Power On<br>the 4 ms are assumed to be long enough for the oscillator to run correctly |
|                                                                               |                             | 2 x DCL clock cycles + 400 ns |      |      |      | After Power On                                                                         |
| Delay time for $\mu\text{C}$ access after $\overline{\text{RST}}$ rising edge | $t_{\mu\text{C}}$           | 500                           |      |      | ns   |                                                                                        |



**Figure 72**      **Reset Input Signal**

## Electrical Characteristics

### 5.6.5 Undervoltage Detection Characteristics



**Figure 73** Undervoltage Control Timing

**Table 38** Parameters of the UVD/POR Circuit

$V_{DD} = 3.3 \text{ V} \pm 5 \%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$

| Parameter                                                            | Symbol       | Limit Values |      |      | Unit             | Test Condition                    |
|----------------------------------------------------------------------|--------------|--------------|------|------|------------------|-----------------------------------|
|                                                                      |              | min.         | typ. | max. |                  |                                   |
| Detection Threshold <sup>1)</sup>                                    | $V_{DET}$    | 2.7          | 2.8  | 2.92 | V                | $V_{DD} = 3.3 \text{ V} \pm 5 \%$ |
| Hysteresis                                                           | $V_{Hys}$    | 30           |      | 90   | mV               |                                   |
| Max. rising/falling $V_{DD}$ edge for activation/deactivation of UVD | $dV_{DD}/dt$ |              |      | 0.1  | V/ $\mu\text{s}$ |                                   |
| Max. rising $V_{DD}$ for power-on <sup>2)</sup>                      |              |              |      | 0.1  | V/ms             |                                   |
| Min. operating voltage                                               | $V_{DDmin}$  | 1.5          |      |      | V                |                                   |

## Electrical Characteristics

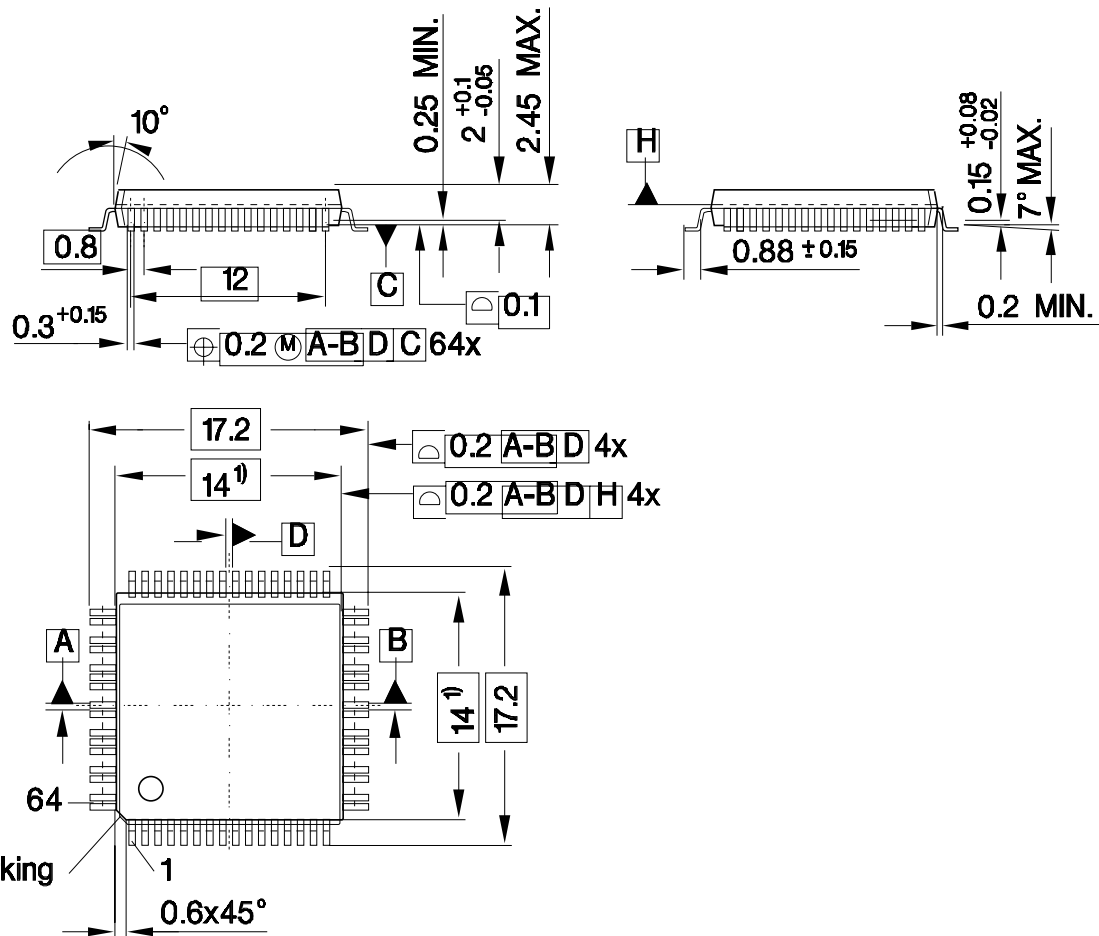
$V_{DD} = 3.3 \text{ V} \pm 5 \%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$

| Parameter                                          | Symbol             | Limit Values |      |      | Unit          | Test Condition |
|----------------------------------------------------|--------------------|--------------|------|------|---------------|----------------|
|                                                    |                    | min.         | typ. | max. |               |                |
| Delay for activation of $\overline{\text{RSTO}}$   | $t_{\text{ACT}}$   |              |      | 10   | $\mu\text{s}$ |                |
| Delay for deactivation of $\overline{\text{RSTO}}$ | $t_{\text{DEACT}}$ |              | 64   |      | ms            |                |

- 1) The Detection Threshold  $V_{\text{DET}}$  is far below the specified supply voltage range of analog and digital parts of the T-SMINT<sup>®</sup>. Therefore, the board designer must take into account that a range of voltages is existing, where neither performance and functionality of the T-SMINT<sup>®</sup> are guaranteed, nor a reset is generated.
- 2) If the integrated Power-On Reset of the T-SMINTI is selected ( $\overline{\text{VDDDET}} = '0'$ ) and the supply voltage  $V_{DD}$  is ramped up from 0V to 3.3V  $\pm 5\%$ , then the T-SMINTI is kept in reset during  $V_{DD\text{min}} < V_{DD} < V_{\text{DET}} + V_{\text{Hys}}$ .  $V_{DD}$  must be ramped up so slowly that the T-SMINTI leaves the reset state after the oscillator circuit has already finished start-up. The start-up time of the oscillator circuit is typically in the range between 3ms and 12ms.

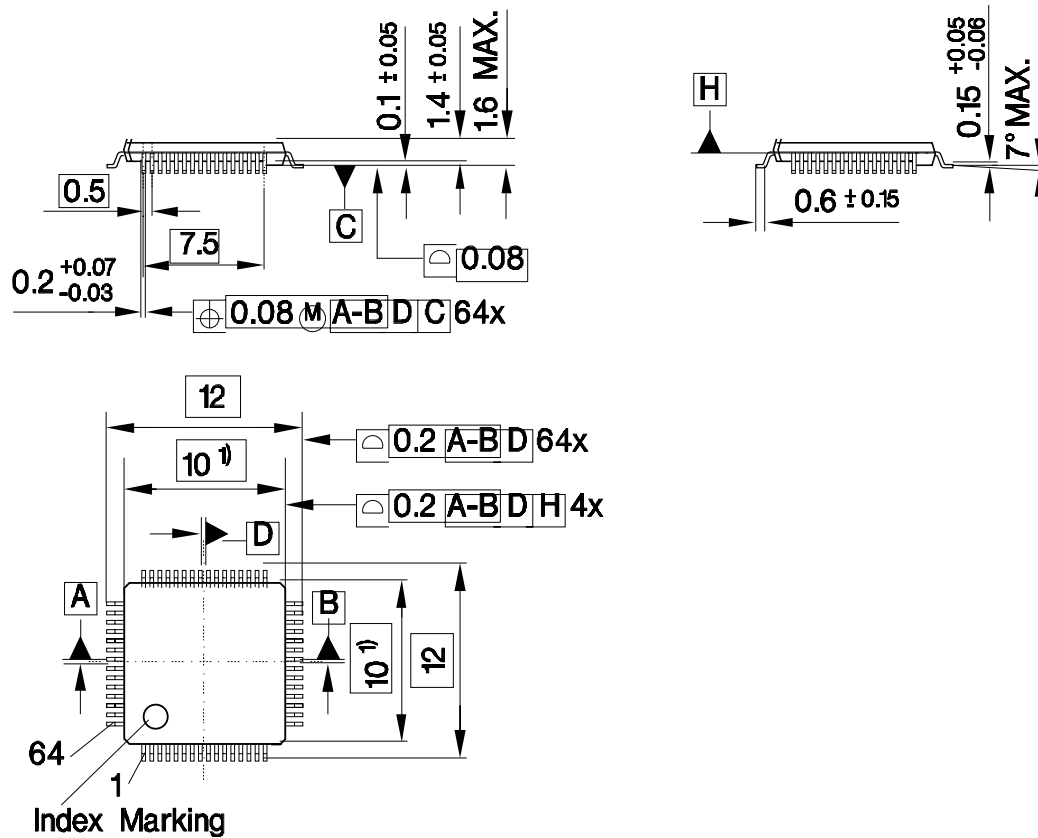
## 6 Package Outlines

### Plastic Package, P-MQFP-64 (Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

## Plastic Package, P-TQFP-64 (Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

## Appendix: Differences between Q- and T-SMINT,I

### 7 Appendix: Differences between Q- and T-SMINT®I

The Q- and T-SMINT®I have been designed to be as compatible as possible. However, some differences between them are unavoidable due to the different line codes 2B1Q and 4B3T used for data transmission on the  $U_{k0}$  line.

Especially the pin compatibility between Q- and T-SMINT®I allows for one single PCB design for both series with only some mounting differences. The  $\mu$ C software can distinguish between the Q- and T-series by reading the hardware Design Number via the IOM®-2 (MONITOR channel identification command) or the  $\mu$ C interface (register ID.DESIGN), respectively (see [Table 39](#)).

**Table 39 Design Number**

|                | Design Number          |                        |
|----------------|------------------------|------------------------|
|                | Q-SMINT®I: 2B1Q        | T-SMINT®I: 4B3T        |
| <b>Version</b> | Version 1.3: '000 001' | Version 1.1: '100 000' |

The following chapter summarizes the main differences between the Q- and T-SMINT®I.

## Appendix: Differences between Q- and T-SMINT,I

### 7.1 Pinning

#### 7.1.1 Pin Definitions and Functions

**Table 40 Pin Definitions and Functions**

|  | Pin<br>T/MQFP-64 | Q-SMINT <sup>®</sup> I: 2B1Q     | T-SMINT <sup>®</sup> I: 4B3T |
|--|------------------|----------------------------------|------------------------------|
|  | 16               | Metallic Termination Input (MTI) | Tie to '1'                   |
|  | 55               | Power Status (primary) (PS1)     | Tie to '1'                   |
|  | 41               | Power Status (secondary) (PS2)   | Tie to '1'                   |

#### 7.1.2 LED Pin $\overline{\text{ACT}}$

The 4 LED states (off, fast flashing, slow flashing, on), which can be displayed with pin  $\overline{\text{ACT}}$ , are slightly different for Q- and T-SMINT<sup>®</sup>I (see [Table 41](#)). This adoption guarantees full compliance of T-SMINT<sup>®</sup>I to the new iNT specification TS 0284/96.

**Table 41  $\overline{\text{ACT}}$  States**

| LED States    | Pin $\overline{\text{ACT}}$  |                              |
|---------------|------------------------------|------------------------------|
|               | Q-SMINT <sup>®</sup> I: 2B1Q | T-SMINT <sup>®</sup> I: 4B3T |
| off           | $V_{DD}$                     | $V_{DD}$                     |
| fast flashing | 8Hz (1 : 1)*                 | 2Hz (1 : 1)*                 |
| slow flashing | 1Hz (1 : 1)*                 | 1Hz (3 : 1)*                 |
| on            | GND                          | GND                          |

Note: \* denotes the duty cycle 'high' : 'low'.

## Appendix: Differences between Q- and T-SMINT,I

### 7.2 U-Transceiver

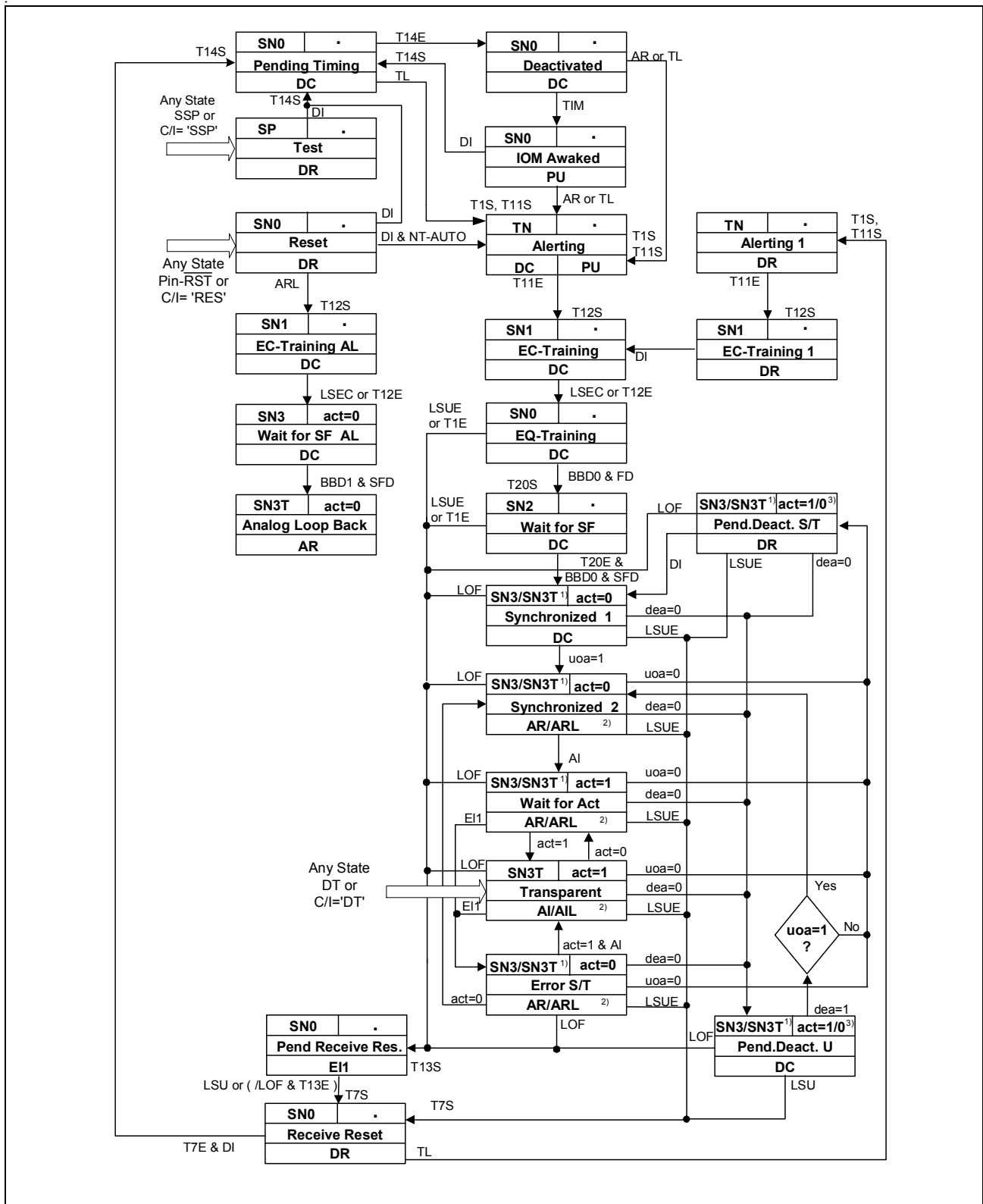
#### 7.2.1 U-Interface Conformity

**Table 42 Related Documents to the U-Interface**

|                                                                 | <b>Q-SMINT<sup>®</sup>I: 2B1Q</b>                      | <b>T-SMINT<sup>®</sup>I: 4B3T</b> |
|-----------------------------------------------------------------|--------------------------------------------------------|-----------------------------------|
| ETSI: TS 102 080                                                | conform to annex A<br>compliant to 10 ms interruptions | conform to annex B                |
| ANSI: T1.601-1998<br>(Revision of ANSI T1.601-1992)             | conform<br>MLT input and decode logic                  | not required                      |
| CNET: ST/LAA/ELR/DNP/822                                        | conform                                                | not required                      |
| RC7355E                                                         | conform                                                | not required                      |
| FTZ-Richtlinie 1 TR 220                                         | not required                                           | conform                           |
| FTZ TS 0284/96<br>'Intelligenter Netzabschluss (iNT)' März 2001 | not required                                           | conform                           |

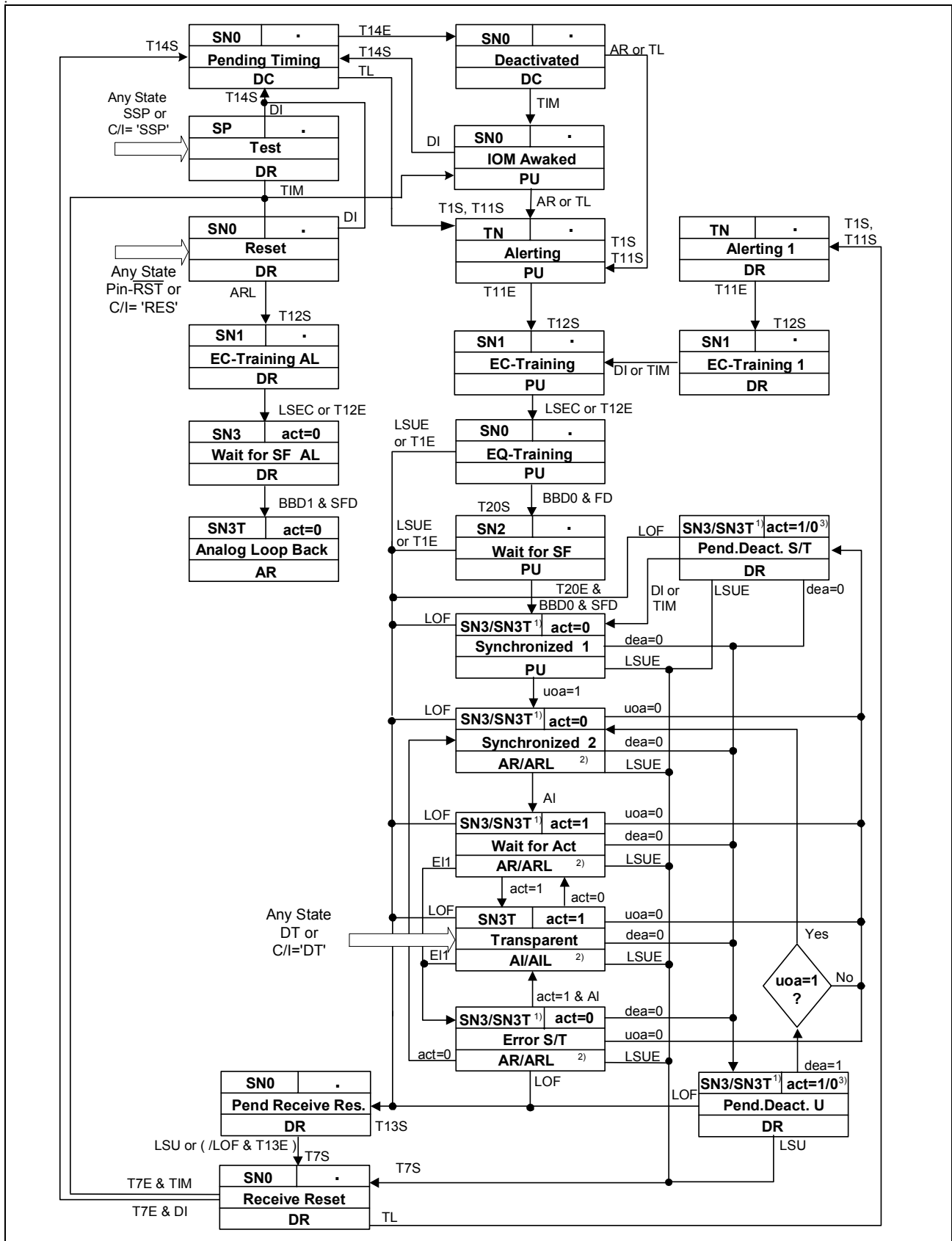
## Appendix: Differences between Q- and T-SMINT,I

### 7.2.2 U-Transceiver State Machines



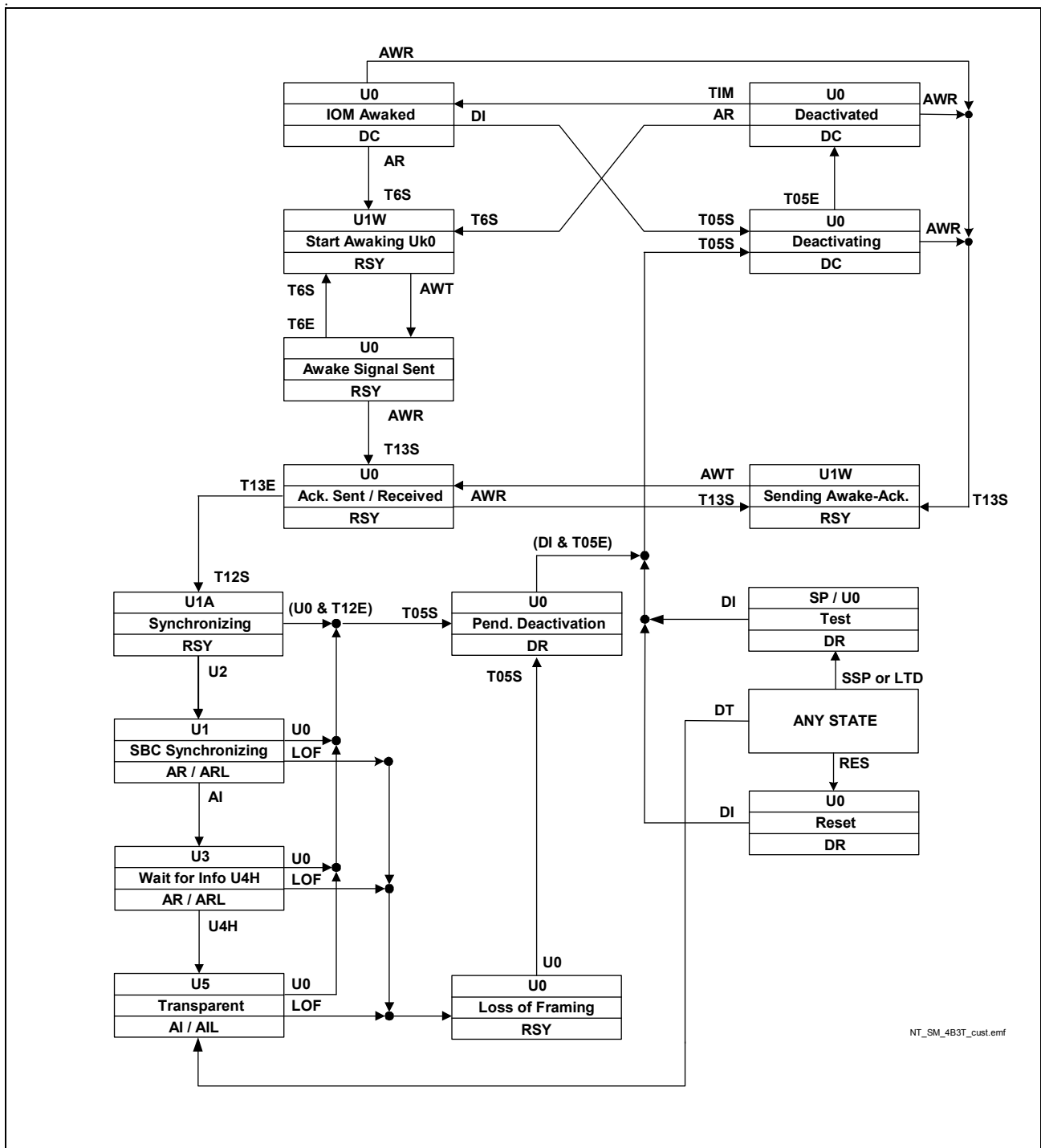
**Figure 74** NTC-Q Compatible State Machine Q-SMINT<sup>®</sup>I: 2B1Q

# Appendix: Differences between Q- and T-SMINT,I



**Figure 75** Simplified State Machine Q-SMINT® I: 2B1Q

## Appendix: Differences between Q- and T-SMINT,I



**Figure 76 IEC-T/NTC-T Compatible State Machine T-SMINT<sup>®</sup>I: 4B3T**

Both the Q- and the T-SMINT® I U-transceiver can be controlled via state machines, which are compatible to those defined for the old NT generation INTC-Q and NTC-T. Additionally, the Q-SMINT® I possesses a newly defined, so called ‘simplified’ state machine. This simplified state machine can be used optionally instead of the INTC-Q compatible state machine and eases the U-transceiver control by software. Such a simplified state machine is not available for the T-SMINT® I.

## Appendix: Differences between Q- and T-SMINT,I

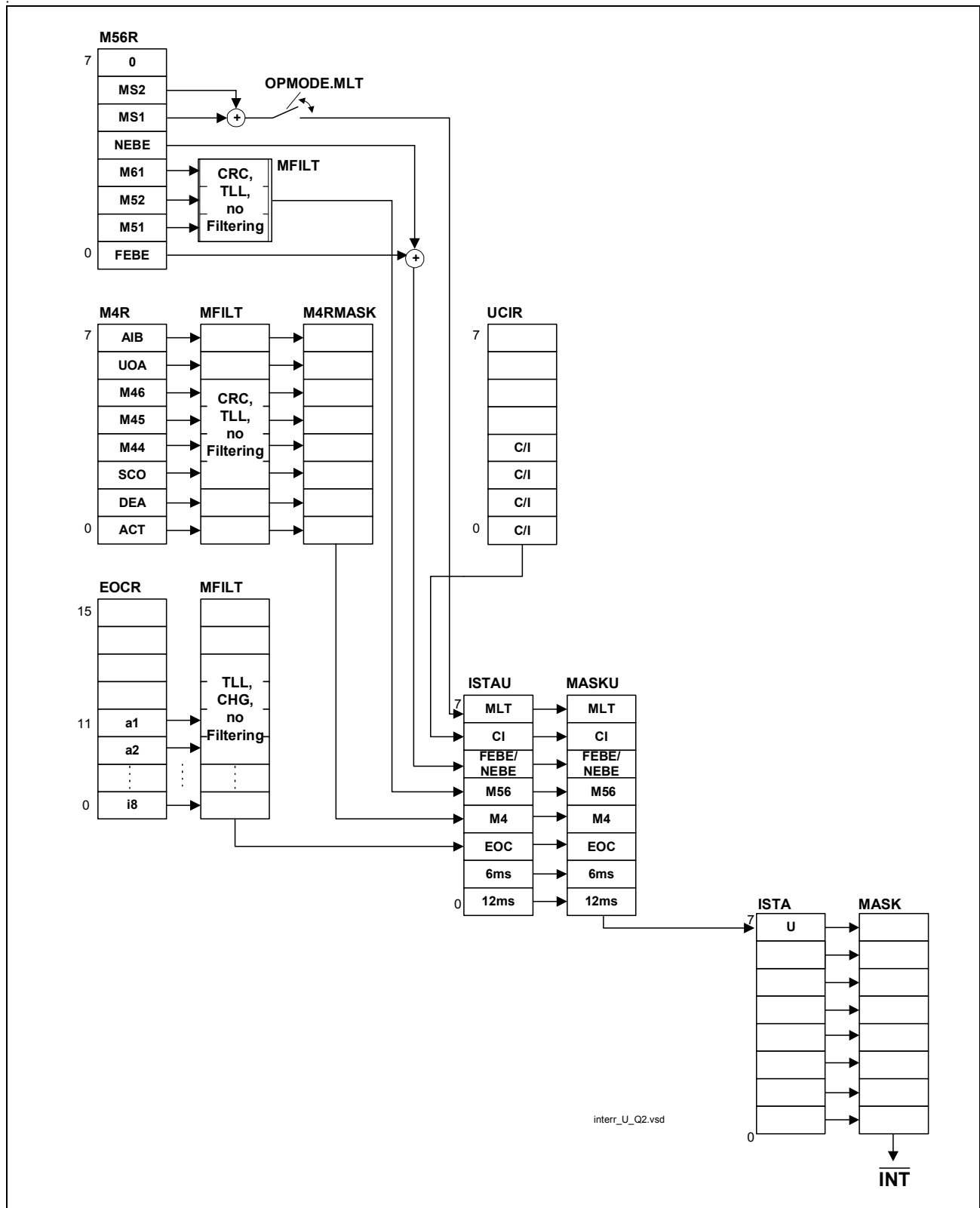
### 7.2.3 Command/Indication Codes

**Table 43 C/I Codes**

| Code | Q-SMINT <sup>®</sup> I: 2B1Q |     | T-SMINT <sup>®</sup> I: 4B3T |     |
|------|------------------------------|-----|------------------------------|-----|
|      | IN                           | OUT | IN                           | OUT |
| 0000 | TIM                          | DR  | TIM                          | DR  |
| 0001 | RES                          | –   | –                            | –   |
| 0010 | –                            | –   | –                            | –   |
| 0011 | –                            | –   | LTD                          | –   |
| 0100 | EI1                          | EI1 | –                            | RSY |
| 0101 | SSP                          | –   | SSP                          | –   |
| 0110 | DT                           | –   | DT                           | –   |
| 0111 | –                            | PU  | –                            | –   |
| 1000 | AR                           | AR  | AR                           | AR  |
| 1001 | –                            | –   | –                            | –   |
| 1010 | ARL                          | ARL | –                            | ARL |
| 1011 | –                            | –   | –                            | –   |
| 1100 | AI                           | AI  | AI                           | AI  |
| 1101 | –                            | –   | RES                          | –   |
| 1110 | –                            | AIL | –                            | AIL |
| 1111 | DI                           | DC  | DI                           | DC  |

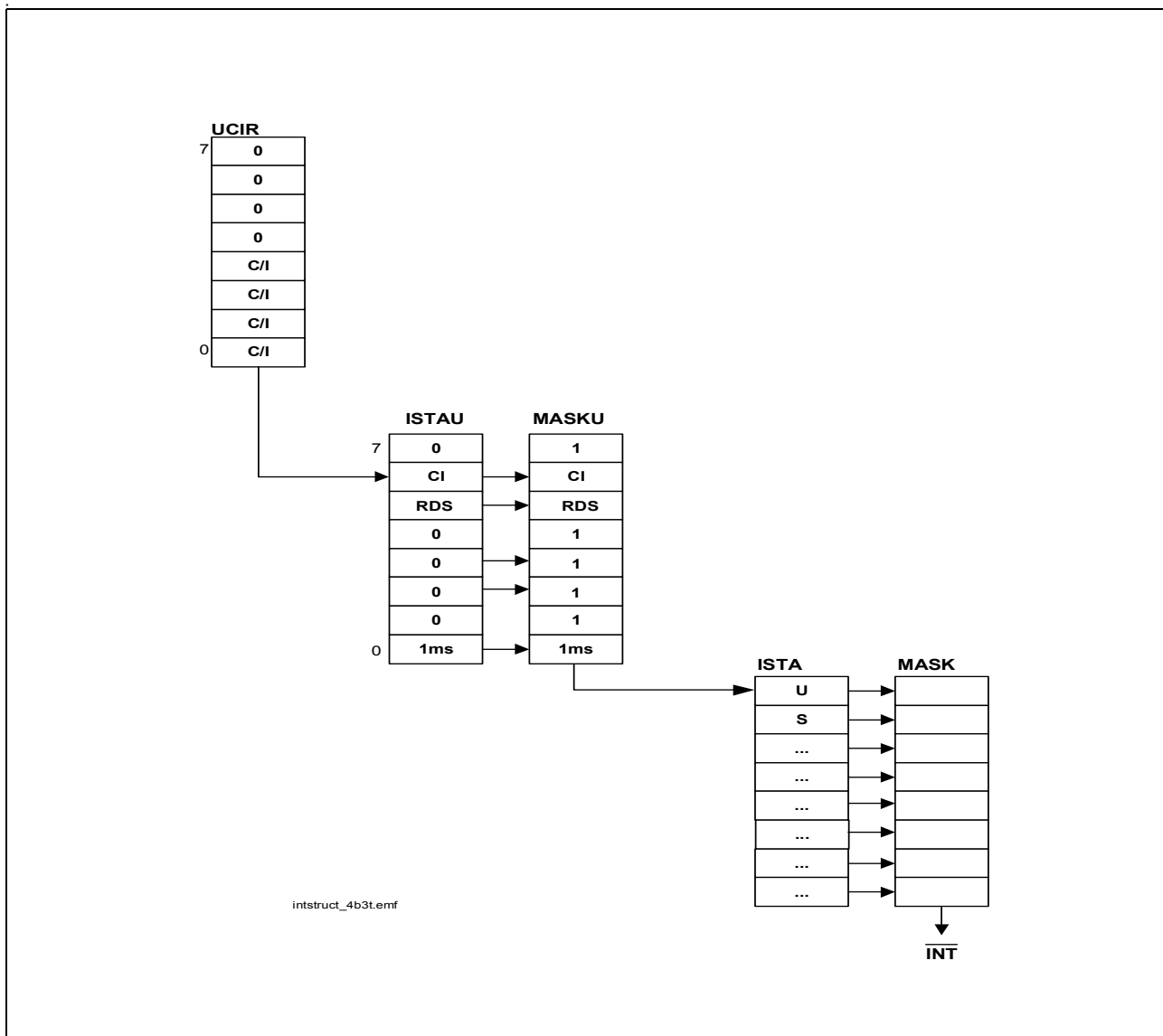
## Appendix: Differences between Q- and T-SMINT,I

### 7.2.4 Interrupt Structure



**Figure 77** Interrupt Structure U-Transceiver Q-SMINT® I: 2B1Q

## Appendix: Differences between Q- and T-SMINT,I



**Figure 78** Interrupt Structure U-Transceiver T-SMINT® I: 4B3T

**Appendix: Differences between Q- and T-SMINT,I**
**7.2.5 Register Summary U-Transceiver**
**U-Interface Registers Q-SMINT®I: 2B1Q**

| Name    | 7                                                | 6   | 5         | 4      | 3               | 2           | 1   | 0      | ADDR                                 | R/W  | RES             |
|---------|--------------------------------------------------|-----|-----------|--------|-----------------|-------------|-----|--------|--------------------------------------|------|-----------------|
| OPMODE  | 0                                                | UCI | FEBE      | MLT    | 0               | CI_SEL      | 0   | 0      | 60 <sub>H</sub>                      | R*/W | 14 <sub>H</sub> |
| MFILT   | M56 FILTER                                       |     | M4 FILTER |        |                 | EOC FILTER  |     |        | 61 <sub>H</sub>                      | R*/W | 14 <sub>H</sub> |
|         | reserved                                         |     |           |        |                 |             |     |        | 62 <sub>H</sub>                      |      |                 |
| EOCR    | 0                                                | 0   | 0         | 0      | a1              | a2          | a3  | d/m    | 63 <sub>H</sub>                      | R    | 0F              |
|         | i1                                               | i2  | i3        | i4     | i5              | i6          | i7  | i8     | 64 <sub>H</sub>                      |      | FF <sub>H</sub> |
| EOCW    | 0                                                | 0   | 0         | 0      | a1              | a2          | a3  | d/m    | 65 <sub>H</sub>                      | W    | 01 <sub>H</sub> |
|         | i1                                               | i2  | i3        | i4     | i5              | i6          | i7  | i8     | 66 <sub>H</sub>                      |      | 00 <sub>H</sub> |
| M4RMASK | M4 Read Mask Bits                                |     |           |        |                 |             |     |        | 67 <sub>H</sub>                      | R*/W | 00 <sub>H</sub> |
| M4WMASK | M4 Write Mask Bits                               |     |           |        |                 |             |     |        | 68 <sub>H</sub>                      | R*/W | A8 <sub>H</sub> |
| M4R     | verified M4 bit data of last received superframe |     |           |        |                 |             |     |        | 69 <sub>H</sub>                      | R    | BE <sub>H</sub> |
| M4W     | M4 bit data to be send with next superframe      |     |           |        |                 |             |     |        | 6A <sub>H</sub>                      | R*/W | BE <sub>H</sub> |
| M56R    | 0                                                | MS2 | MS1       | NEBE   | M61             | M52         | M51 | FEBE   | 6B <sub>H</sub>                      | R    | 1F <sub>H</sub> |
| M56W    | 1                                                | 1   | 1         | 1      | M61             | M52         | M51 | FEBE   | 6C <sub>H</sub>                      | W    | FF <sub>H</sub> |
| UCIR    | 0                                                | 0   | 0         | 0      | C/I code output |             |     |        | 6D <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| UCIW    | 0                                                | 0   | 0         | 0      | C/I code input  |             |     |        | 6E <sub>H</sub>                      | W    | 01 <sub>H</sub> |
| TEST    | 0                                                | 0   | 0         | 0      | CCRC            | +1<br>Tones | 0   | 40 KHz | 6F <sub>H</sub>                      | R*/W | 00 <sub>H</sub> |
| LOOP    | 0                                                | DLB | TRANS     | U/IOM® | 1               | LBBD        | LB2 | LB1    | 70 <sub>H</sub>                      | R*/W | 08 <sub>H</sub> |
| FEBE    | FEBE Counter Value                               |     |           |        |                 |             |     |        | 71 <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| NEBE    | NEBE Counter Value                               |     |           |        |                 |             |     |        | 72 <sub>H</sub>                      | R    | 00 <sub>H</sub> |
|         | reserved                                         |     |           |        |                 |             |     |        | 73 <sub>H</sub> ~<br>79 <sub>H</sub> |      |                 |

**Appendix: Differences between Q- and T-SMINT,I**

| Name           | 7                 | 6  | 5             | 4   | 3  | 2   | 1   | 0    | ADDR                                 | R/W  | RES             |
|----------------|-------------------|----|---------------|-----|----|-----|-----|------|--------------------------------------|------|-----------------|
| ISTAU          | MLT               | CI | FEBE/<br>NEBE | M56 | M4 | EOC | 6ms | 12ms | 7A <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| MASKU          | MLT               | CI | FEBE/<br>NEBE | M56 | M4 | EOC | 6ms | 12ms | 7B <sub>H</sub>                      | R*/W | FF <sub>H</sub> |
| FW_<br>VERSION | reserved          |    |               |     |    |     |     |      | 7C <sub>H</sub>                      |      |                 |
|                | FW Version Number |    |               |     |    |     |     |      | 7D <sub>H</sub>                      | R    | 6x <sub>H</sub> |
|                | reserved          |    |               |     |    |     |     |      | 7E <sub>H</sub> -<br>7F <sub>H</sub> |      |                 |

## Appendix: Differences between Q- and T-SMINT,I

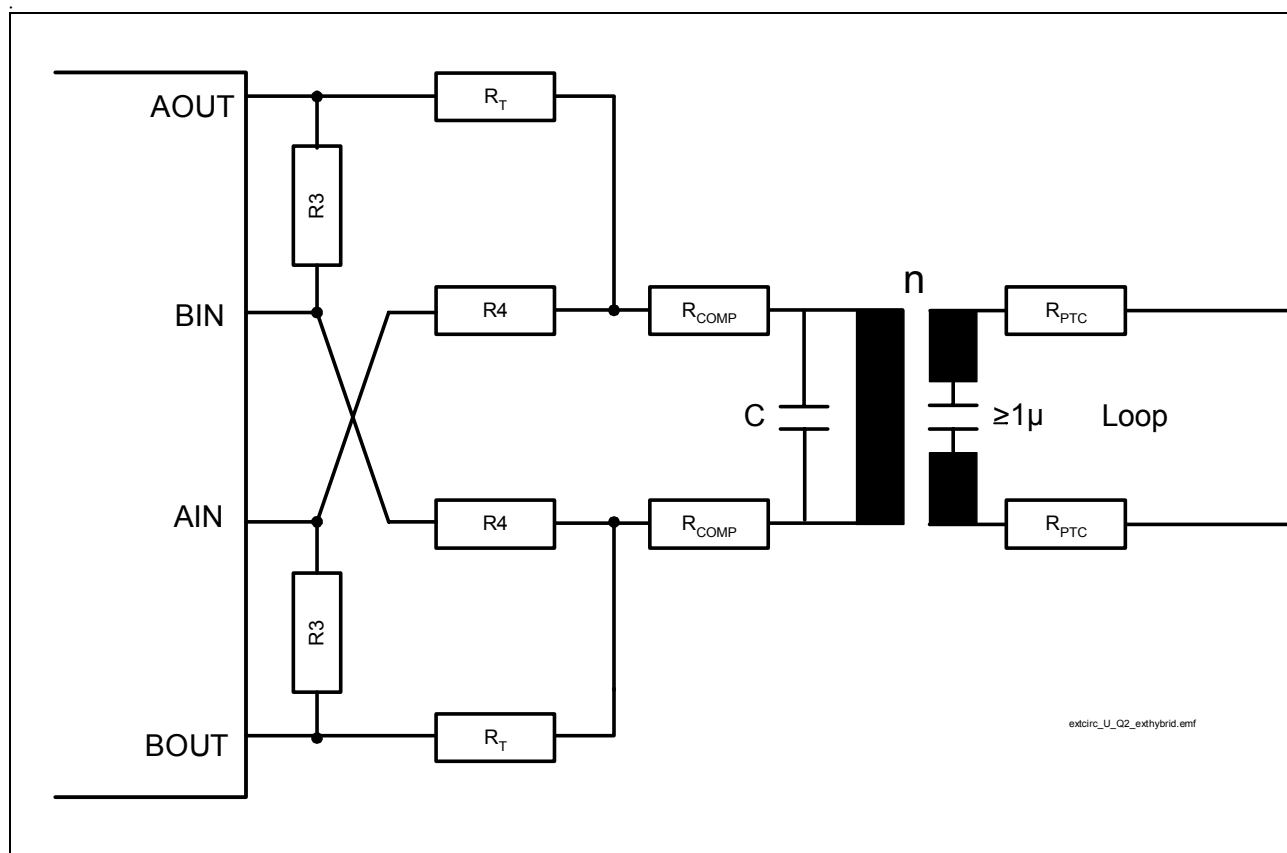
### U-Interface Registers T-SMINT®I: 4B3T

| Name           | 7                         | 6   | 5                       | 4 | 3               | 2 | 1   | 0    | ADDR                                 | R/W  | RES             |
|----------------|---------------------------|-----|-------------------------|---|-----------------|---|-----|------|--------------------------------------|------|-----------------|
| OPMODE         | 0                         | UCI | 0                       | 0 | 0               | 0 | 0   | 0    | 60 <sub>H</sub>                      | R*/W | 00 <sub>H</sub> |
|                | reserved                  |     |                         |   |                 |   |     |      | 61 <sub>H</sub> -<br>6C <sub>H</sub> |      |                 |
| UCIR           | 0                         | 0   | 0                       | 0 | C/I code output |   |     |      | 6D <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| UCIW           | 0                         | 0   | 0                       | 0 | C/I code input  |   |     |      | 6E <sub>H</sub>                      | W    | 01 <sub>H</sub> |
| LOOP           | reserved                  |     |                         |   |                 |   |     |      | 6F <sub>H</sub>                      |      |                 |
|                | 0                         | 0   | TRANSU/IOM <sup>®</sup> | 1 | LBB             | D | LB2 | LB1  | 70 <sub>H</sub>                      | R*/W | 08 <sub>H</sub> |
|                | reserved                  |     |                         |   |                 |   |     |      | 71 <sub>H</sub>                      |      |                 |
| RDS            | Block Error Counter Value |     |                         |   |                 |   |     |      | 72 <sub>H</sub>                      | R    | 00 <sub>H</sub> |
|                | reserved                  |     |                         |   |                 |   |     |      | 73 <sub>H</sub> -<br>79 <sub>H</sub> |      |                 |
| ISTAU          | 0                         | CI  | RDS                     | 0 | 0               | 0 | 0   | 1 ms | 7A <sub>H</sub>                      | R    | 00 <sub>H</sub> |
| MASKU          | 1                         | CI  | RDS                     | 1 | 1               | 1 | 1   | 1 ms | 7B <sub>H</sub>                      | R*/W | FF <sub>H</sub> |
|                | reserved                  |     |                         |   |                 |   |     |      | 7C <sub>H</sub>                      |      |                 |
| FW_<br>VERSION | FW Version Number         |     |                         |   |                 |   |     |      | 7D <sub>H</sub>                      | R    | 3x <sub>H</sub> |
|                | reserved                  |     |                         |   |                 |   |     |      | 7E <sub>H</sub> -<br>7F <sub>H</sub> |      |                 |

## Appendix: Differences between Q- and T-SMINT,I

### 7.3 External Circuitry

The external circuitry of the Q- and T-SMINT<sup>®</sup>I is equivalent; however, some external components of the U-transceiver hybrid must be dimensioned different for 2B1Q and 4B3T. All information on the external circuitry is preliminary and may be changed in future documents.



**Figure 79 External Circuitry Q- and T-SMINT<sup>®</sup>I**

Note: the necessary protection circuitry is not displayed in [Figure 79](#).

**Table 44 Dimensions of External Components**

| Component                              | Q-SMINT <sup>®</sup> I: 2B1Q       | T-SMINT <sup>®</sup> I: 4B3T                    |
|----------------------------------------|------------------------------------|-------------------------------------------------|
| Transformer:<br>Ratio                  | 1:2                                | 1:1.6                                           |
| Main Inductivity                       | 14.5 mH                            | 7.5 mH                                          |
| Resistance                             | 1.3 kΩ                             | 1.75 kΩ                                         |
| Resistance                             | 1.0 kΩ                             | 1.0 kΩ                                          |
| Resistance                             | 9.5 Ω                              | 25 Ω                                            |
| Capacitor C                            | 27 nF                              | 15 nF                                           |
| R <sub>PTC</sub> and R <sub>Comp</sub> | $2R_{PTC} + 8R_{Comp} = 40 \Omega$ | $n^2 \times (2R_{COMP} + R_B) + R_L = 20\Omega$ |

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