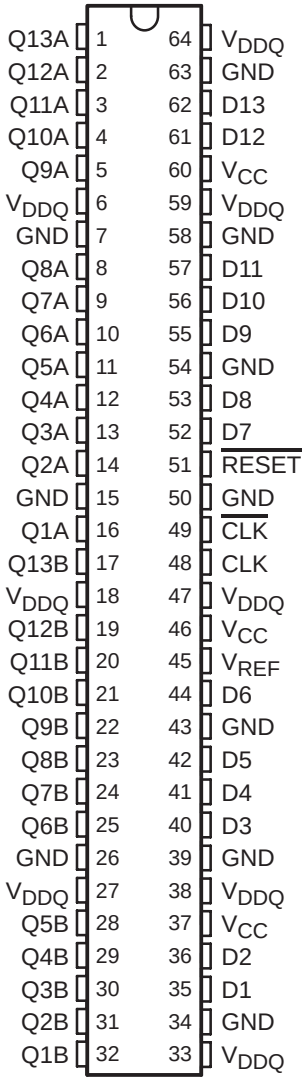
- **Member of the Texas Instruments Widebus™ Family**
- **Operates at 2.3 V to 2.7 V for PC1600, PC2100, and PC2700**
- **Operates at 2.5 V to 2.7 V for PC3200 (QFN Package)**
- **Pinout and Functionality Compatible With JEDEC Standard SSTV16859**
- **600 ps Faster (Simultaneous Switching) Than the JEDEC Standard SSTV16859 in PC2700 DIMM Applications**
- **1-to-2 Outputs to Support Stacked DDR DIMMs**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line**
- **Outputs Meet SSTL_2 Class I Specifications**
- **Supports SSTL_2 Data Inputs**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
- **Pinout Optimizes DIMM PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN – RGQ (Tin-Pb Finish)	Tape and reel	SN74SSTVF16859SR	SSF859
	QFN – RGQ (Matte-Tin Finish)		SN74SSTVF16859S8	
	TSSOP – DGG	Tape and reel	SN74SSTVF16859GR	SSTVF16859

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

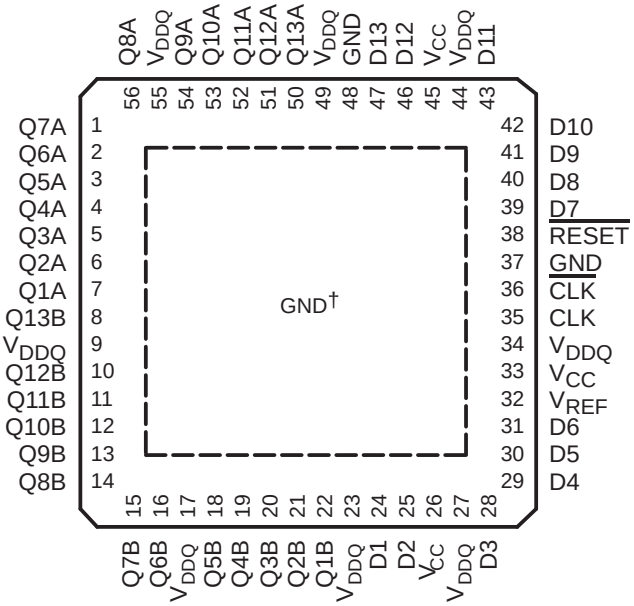
All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTVF16859 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

RGQ PACKAGE
(TOP VIEW)

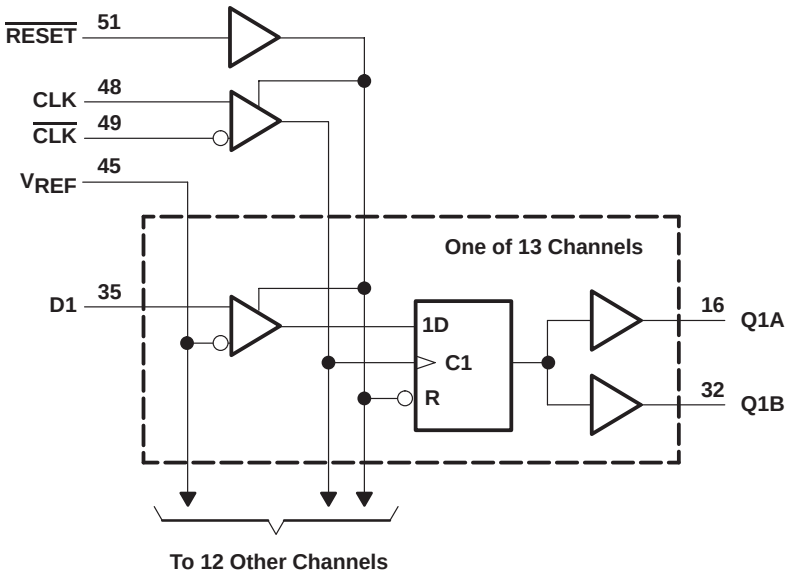


† The center die pad must be connected to GND.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

logic diagram (positive logic)



Pin numbers shown are for the DGG package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ} . . . . . −0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . −0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 55°C/W
(see Note 4): RGQ package . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	PC1600, PC2100, PC2700	2.3		2.7	V
		PC3200	2.5		2.7	
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)	PC1600, PC2100, PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF}+310mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF}−310mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF}+150mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF}−150mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				−16	mA
I_{OL}	Low-level output current				16	
T_A	Operating free-air temperature		0		70	°C

NOTE 5: The $\overline{\text{RESET}}$ input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics for PC1600, PC2100, and PC2700 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP‡	MAX	UNIT
V_{IK}		I_I = −18 mA		2.3 V			−1.2	V
V_{OH}		I_{OH} = −100 μA		2.3 V to 2.7 V	V_{DDQ}−0.2			V
		I_{OH} = −8 mA		2.3 V	1.95			
V_{OL}		I_{OL} = 100 μA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.3 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND		2.7 V			±5	μA
I_{CC}	Static standby	$\overline{\text{RESET}}$ = GND	I_O = 0	2.7 V			10	μA
	Static operating	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					25	mA
I_{CCD}	Dynamic operating − clock only	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	I_O = 0	2.5 V		19		μA/ MHz
	Dynamic operating − per each data input	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7		μA/ clock MHz/ D input
C_i§	Data inputs	$V_I = V_{REF} \pm 310$ mV		2.5 V	2.5	3	3.5	pF
	CLK, $\overline{\text{CLK}}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360mV			2.5	3	3.5	
	$\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND			2.3	3	3.5	

† For this test condition, V_{DDQ} always is equal to V_{CC}.
‡ All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
§ Measured at 50-MHz input frequency

electrical characteristics for PC3200 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP‡	MAX	UNIT
V_{IK}		I_I = −18 mA		2.5 V			−1.2	V
V_{OH}		I_{OH} = −100 µA		2.5 V to 2.7 V	V_{DDQ}−0.2			V
		I_{OH} = −8 mA		2.5 V	1.95			
V_{OL}		I_{OL} = 100 µA		2.5 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.5 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND		2.7 V			±5	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	2.7 V			10	µA
	Static operating	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					25	mA
I_{CCD}	Dynamic operating − clock only	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	2.6 V		19		µA/ MHz
	Dynamic operating − per each data input	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7		µA/ clock MHz/ D input
C_i§	Data inputs	$V_I = V_{REF}$ ± 310 mV		2.6 V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360mV			2.5	3	3.5	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND			2.3	3	3.5	

† For this test condition, V_{DDQ} always is equal to V_{CC}.
‡ All typical values are at V_{CC} = 2.6 V, T_A = 25°C.
§ Measured at 50-MHz input frequency

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 2.5 V ± 0.2 V†		V_{CC} = 2.6 V ± 0.1 V†		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				500		500	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low			1		1		ns
t_{act}	Differential inputs active time (see Note 6)				22		22	ns
t_{inact}	Differential inputs inactive time (see Note 7)				22		22	ns
t_{su}	Setup time	Fast slew rate (see Notes 8 and 10)	Data before CLK↑, $\overline{CLK}$↓	0.65		0.65		ns
		Slow slew rate (see Notes 9 and 10)		0.75		0.75		
t_h	Hold time	Fast slew rate (see Notes 8 and 10)	Data after CLK↑, $\overline{CLK}$↓	0.65		0.65		ns
		Slow slew rate (see Notes 9 and 10)		0.8		0.8		

† For this test condition, V_{DDQ} always is equal to V_{CC}.

NOTES: 6. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
7. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.
8. For data signal input slew rate ≥1 V/ns.
9. For data signal input slew rate ≥0.5 V/ns and <1 V/ns.
10. CLK, $\overline{CLK}$ signals input slew rates are ≥1 V/ns.

switching characteristics for TSSOP over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V†		UNIT
			MIN	MAX	
f_{max}			500		MHz
t_{pd}‡	CLK and $\overline{CLK}$	Q	1.1	2.5	ns
t_{PHL}	$\overline{RESET}$	Q		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.
‡ Single-bit switching

switching characteristics for QFN over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V†		V_{CC} = 2.6 V ± 0.1 V†		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			500		500		MHz
t_{pd}‡	CLK and $\overline{CLK}$	Q	1.1	2.5	1.1	2.2	ns
t_{PHL}	$\overline{RESET}$	Q		5		5	ns

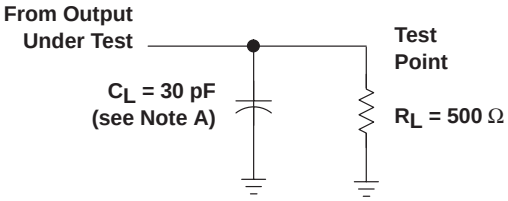
† For this test condition, V_{DDQ} always is equal to V_{CC}.
‡ Single-bit switching

output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

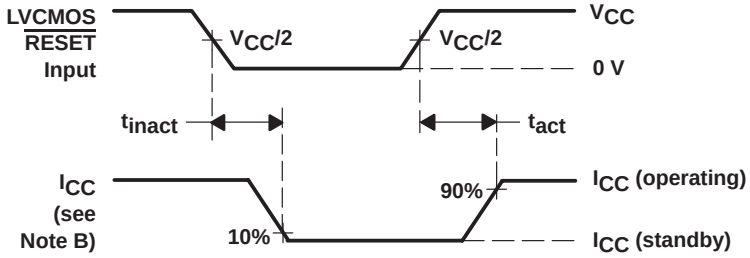
PARAMETER	FROM	TO	V_{CC} = 2.5 V ± 0.2 V†		V_{CC} = 2.6 V ± 0.1 V†		UNIT
			MIN	MAX	MIN	MAX	
dV/dt_r	20%	80%	1	4	1	4	V/ns
dV/dt_f	80%	20%	1	4	1	4	V/ns
dV/dt_Δ§	20% or 80%	80% or 20%		1		1	V/ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.
§ Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

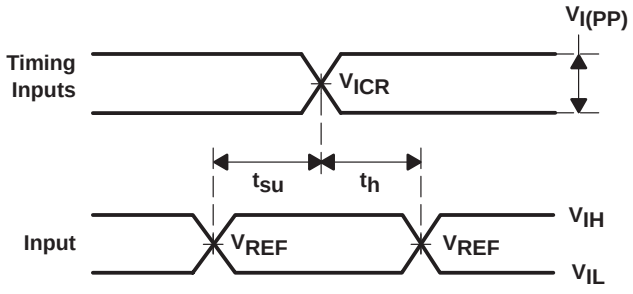
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V AND V_{CC} = 2.6 V ± 0.1 V



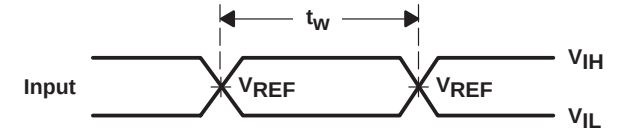
LOAD CIRCUIT



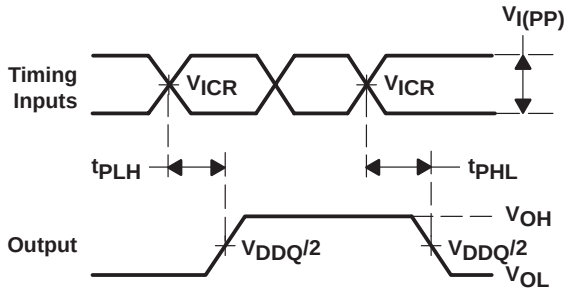
VOLTAGE AND CURRENT WAVEFORMS
INPUTS ACTIVE AND INACTIVE TIMES



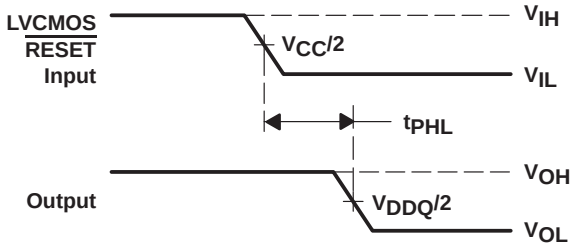
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



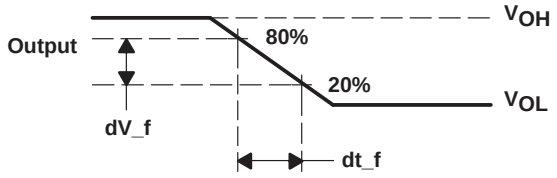
VOLTAGE WAVEFORMS
PULSE DURATION



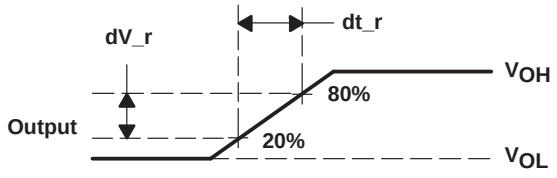
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

NOTES: A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time, with one transition per measurement.
E. $V_{TT} = V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ − 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

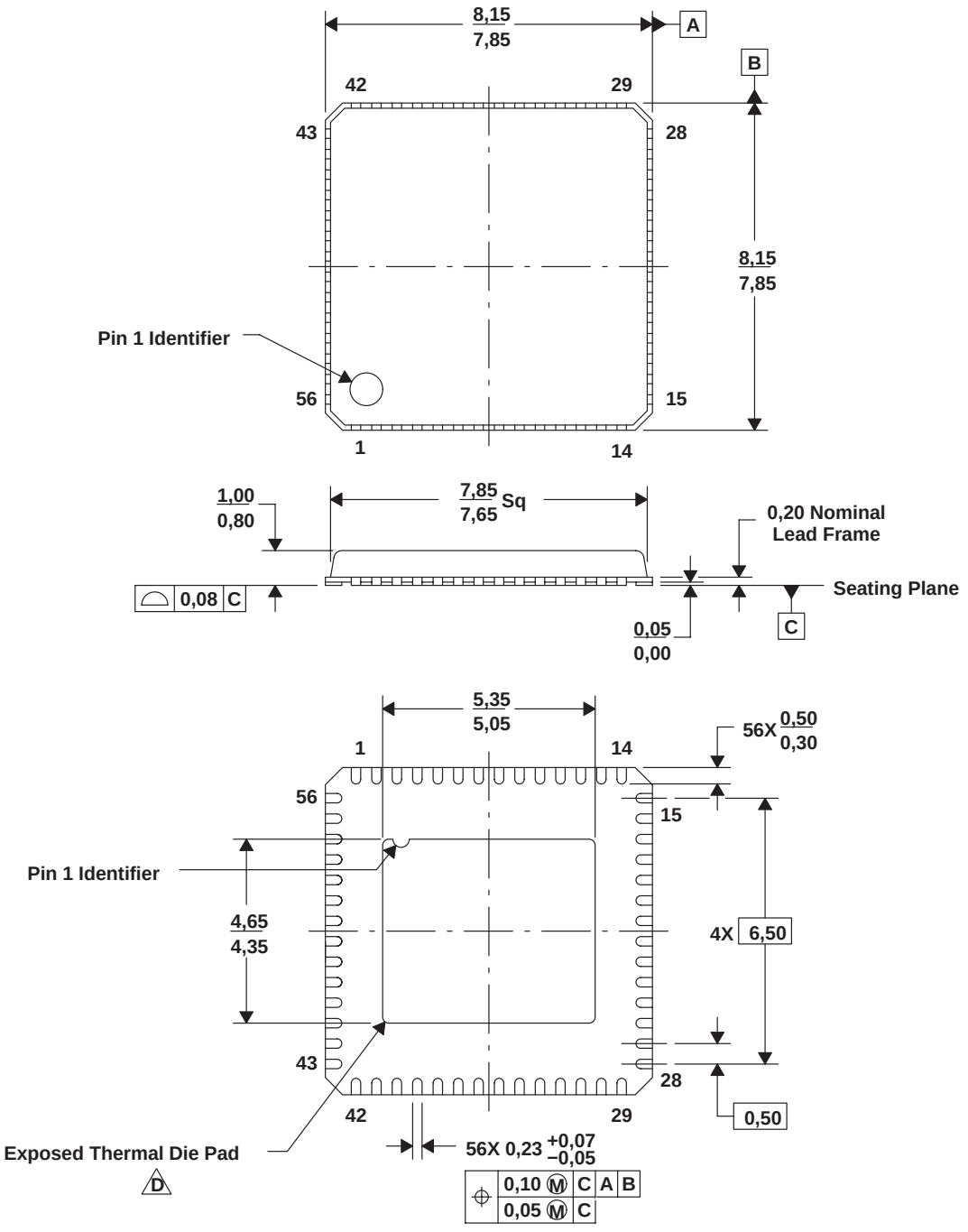
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74SSTVF16859GR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-250C-UNLIM
SN74SSTVF16859S8	ACTIVE	QFN	RGQ	56	2000	None	CU	Level-3-235C-168 HR
SN74SSTVF16859SR	ACTIVE	QFN	RGQ	56	2000	None	CU	Level-3-235C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

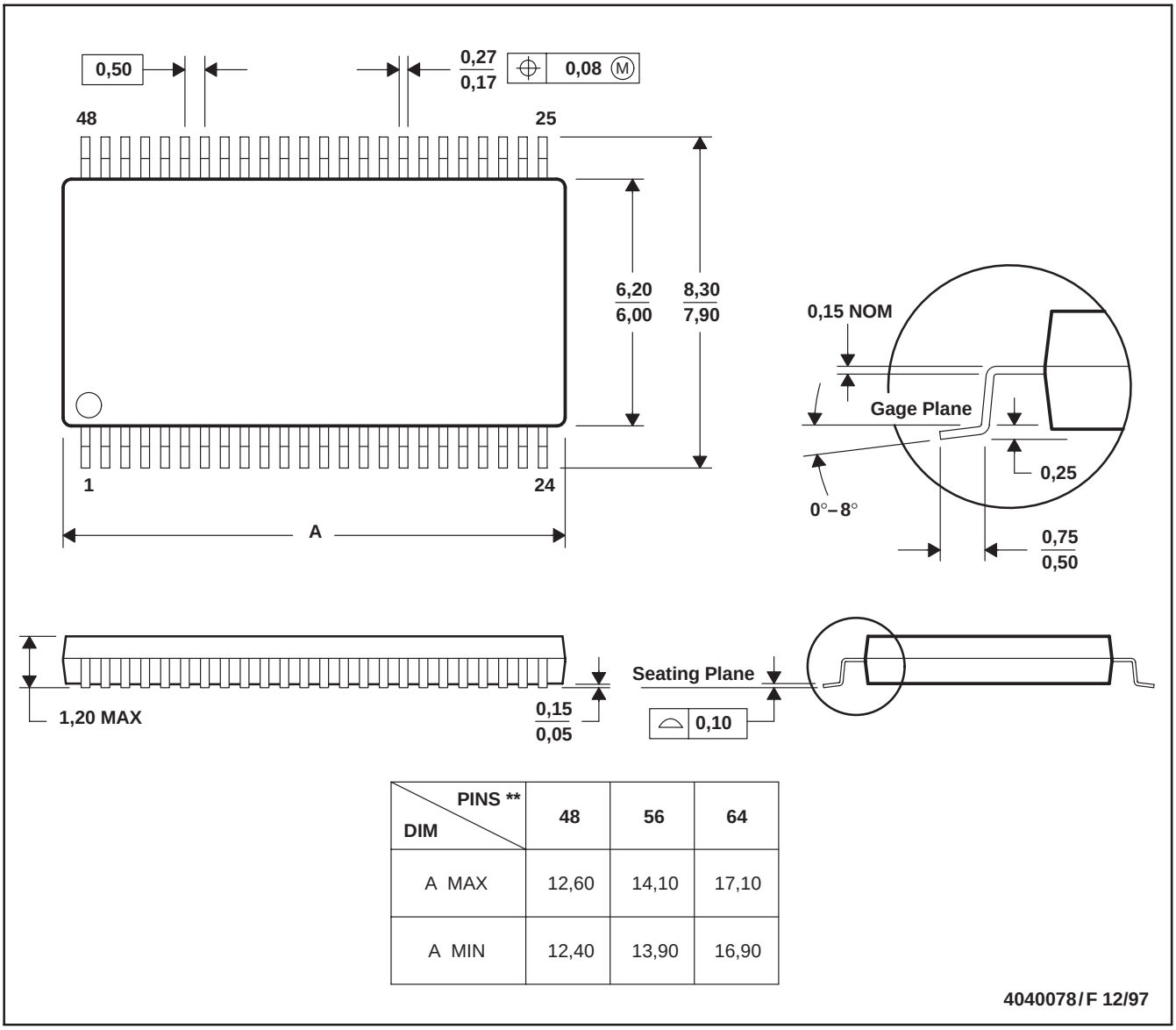
RGQ (S−PQFP−N56) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad may be electrically connected to ground.
E. Package registration with JEDEC MO-220 variation VLLD-2.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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