

74LV4051

8-channel analog multiplexer/demultiplexer

Rev. 5 — 17 September 2014

Product data sheet

1. General description

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). It is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC4051 and 74HCT4051. With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 V to 6.0 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features and benefits

- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low ON resistance:
 - ◆ 145 Ω (typical) at $V_{CC} - V_{EE} = 2.0$ V
 - ◆ 80 Ω (typical) at $V_{CC} - V_{EE} = 3.0$ V
 - ◆ 60 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
- Logic level translation:
 - ◆ To enable 3 V logic to communicate with ± 3 V analog signals
- Typical 'break before make' built in
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

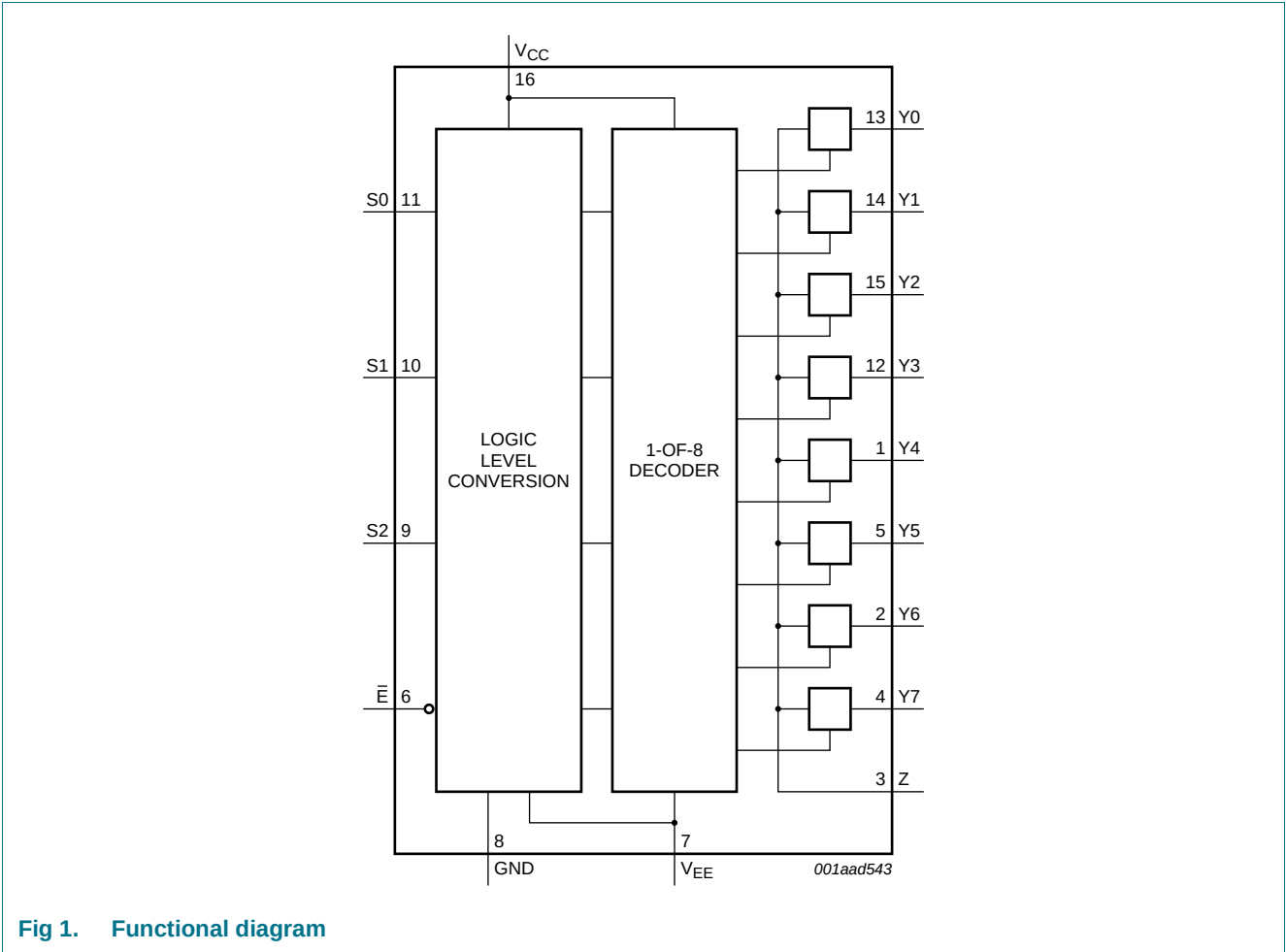


3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4051N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4051D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4051DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4051PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4051BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



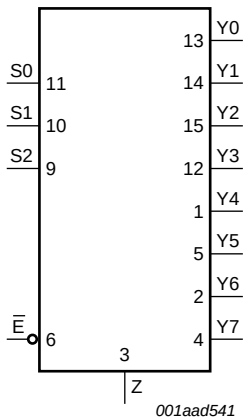


Fig 2. Logic symbol

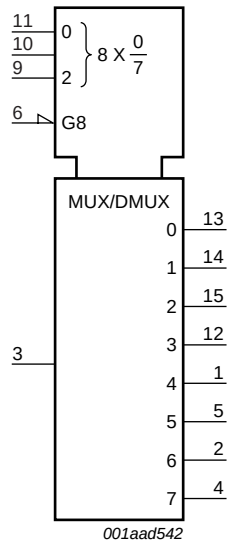


Fig 3. IEC logic symbol

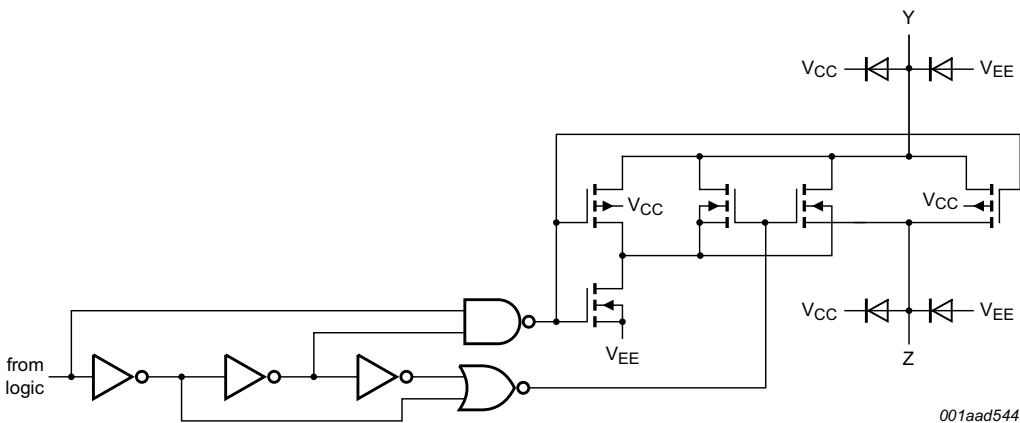
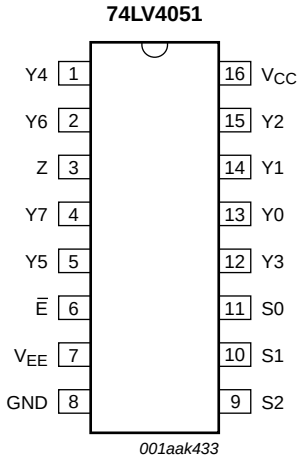


Fig 4. Schematic diagram (one switch)

5. Pinning information

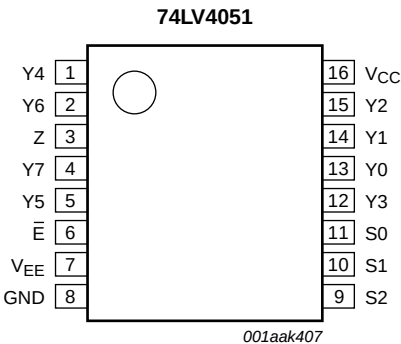
5.1 Pinning



74LV4051

Y4 1, Y6 2, Z 3, Y7 4, Y5 5, $\bar{E}$ 6, VEE 7, GND 8, 16 VCC, 15 Y2, 14 Y1, 13 Y0, 12 Y3, 11 S0, 10 S1, 9 S2

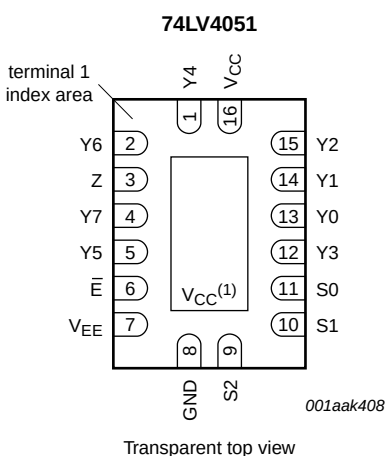
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Y4 1, Y6 2, Z 3, Y7 4, Y5 5, $\bar{E}$ 6, VEE 7, GND 8, 16 VCC, 15 Y2, 14 Y1, 13 Y0, 12 Y3, 11 S0, 10 S1, 9 S2

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74LV4051

terminal 1 index area, Y4 1, VCC 16, Y6 2, Z 3, Y7 4, Y5 5, $\bar{E}$ 6, VEE 7, 8 GND, 9 S2, 15 Y2, 14 Y1, 13 Y0, 12 Y3, 11 S0, 10 S1

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Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to VCC.

Fig 5. Pin configuration SOT38-4 and SOT109-1

Fig 6. Pin configuration SOT338-1 and SOT403-1

Fig 7. Pin configuration for SOT763-1

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	6	enable input (active LOW)
VEE	7	supply voltage
GND	8	ground supply voltage
S0, S1, S2	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
VCC	16	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Input				Channel ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		^[1] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	^[2] -	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	^[2] -	±20	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	^[2] -	±25	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3]		
		DIP16 package	-	750	mW
		SO16 package	-	500	mW
		TSSOP16 package	-	500	mW
		DHVQFN16 package	-	500	mW

- [1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n , and in this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE} .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage	see Figure 8	1	3.3	6	V
V _I	input voltage		0	-	V _{CC}	V
V _{SW}	switch voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

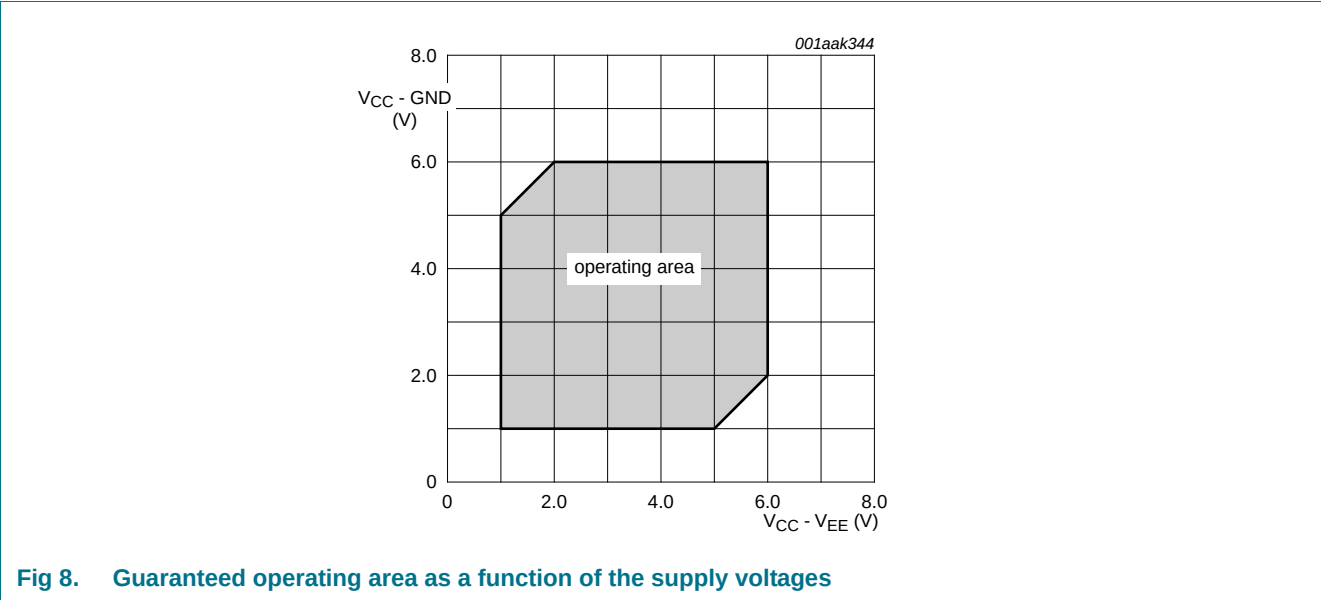


Fig 8. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

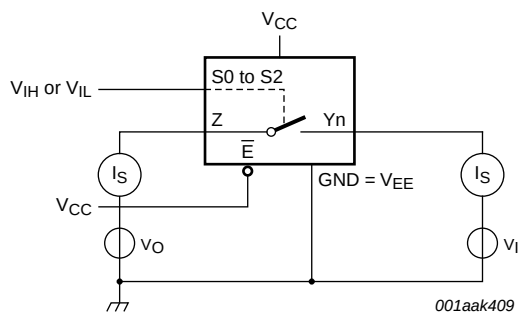
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V _{CC} = 6.0 V	4.20	-	-	4.20	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	-	1.80	V
I _I	input leakage current	V _I = V _{CC} or GND						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(OFF)}	OFF-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 9						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 10						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A						
		V _{CC} = 3.6 V	-	-	20	-	40	μA
		V _{CC} = 6.0 V	-	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} – 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{SW}	switch capacitance	independent pins Y _n	-	5	-	-	-	pF
		common pin Z	-	25	-	-	-	pF

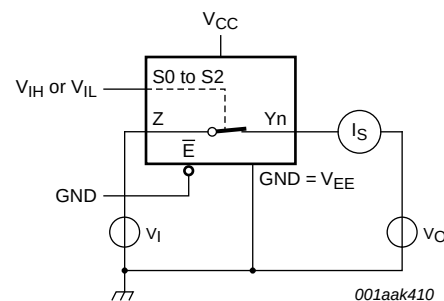
[1] Typical values are measured at T_{amb} = 25 °C.

9.1 Test circuits



$V_I = V_{CC}$ or V_{EE} and $V_O = V_{EE}$ or V_{CC} .

Fig 9. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or V_{EE} and $V_O = \text{open circuit}$.

Fig 10. Test circuit for measuring ON-state leakage current

9.2 ON resistance

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 11](#) and [Figure 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$	[2]	-	-	-	-	Ω
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	145	325	-	375	Ω
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	90	200	-	235	Ω
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	80	180	-	210	Ω
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	60	135	-	160	Ω
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	55	125	-	145	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$	[2]	-	-	-	-	Ω
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	5	-	-	-	Ω
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	3	-	-	-	Ω
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	2	-	-	-	Ω

Table 7. ON resistance ...continued

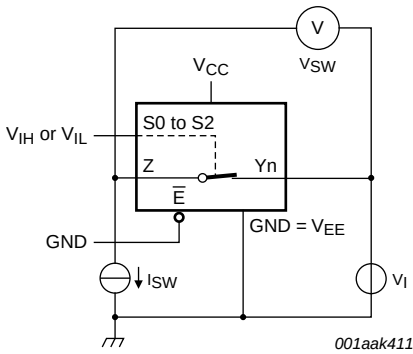
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 11](#) and [Figure 12](#).

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ ^[1]	Max	Min	Max	
R _{ON(rail)}	ON resistance (rail)	V _I = GND							
		V _{CC} = 1.2 V; I _{SW} = 100 µA	[2]	-	225	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA		-	110	235	-	270	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA		-	70	145	-	165	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA		-	60	130	-	150	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA		-	45	100	-	115	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA		-	40	85	-	100	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = V _{CC} – V _{EE}							
		V _{CC} = 1.2 V; I _{SW} = 100 µA	[2]	-	250	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA		-	120	320	-	370	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA		-	75	195	-	225	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA		-	70	175	-	205	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA		-	50	130	-	150	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA		-	45	120	-	135	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

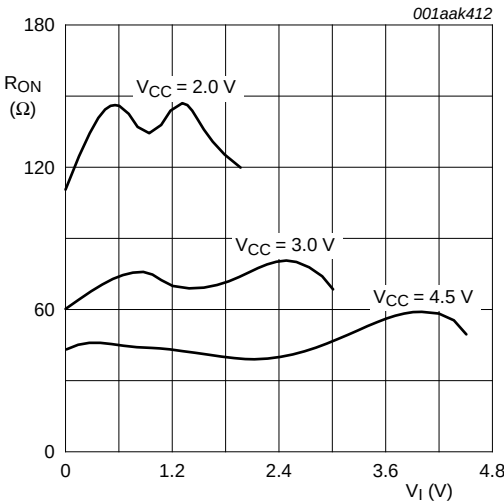
[2] When supply voltages (V_{CC} – V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3 On resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 11. Test circuit for measuring R_{ON}



$V_I = 0 \text{ V to } V_{CC} - V_{EE}$

Fig 12. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 15](#).

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	Yn to Z, Z to Yn; see Figure 13	[2]						
		V _{CC} = 1.2 V		-	25	-	-	-	ns
		V _{CC} = 2.0 V		-	9	17	-	20	ns
		V _{CC} = 2.7 V		-	6	13	-	15	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	5	10	-	12	ns
		V _{CC} = 4.5 V		-	4	9	-	10	ns
		V _{CC} = 6.0 V		-	3	8	-	8	ns
t _{en}	enable time	$\overline{E}$ to Yn, Z; see Figure 14	[2]						
		V _{CC} = 1.2 V		-	145	-	-	-	ns
		V _{CC} = 2.0 V		-	49	94	-	112	ns
		V _{CC} = 2.7 V		-	36	69	-	83	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	[3]	-	23	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	28	55	-	66	ns
		V _{CC} = 4.5 V		-	25	47	-	56	ns
		V _{CC} = 6.0 V		-	19	38	-	43	ns
		Sn to Yn; see Figure 14	[2]						
		V _{CC} = 1.2 V		-	140	-	-	-	ns
		V _{CC} = 2.0 V		-	48	90	-	107	ns
		V _{CC} = 2.7 V		-	35	66	-	79	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	[3]	-	22	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	27	53	-	63	ns
		V _{CC} = 4.5 V		-	24	45	-	54	ns
		V _{CC} = 6.0 V		-	18	34	-	41	ns

Table 8. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 15](#).

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ ^[1]	Max	Min	Max	
t _{dis}	disable time	$\bar{E}$ to Y _n , Z; see Figure 14	[2]						
		V _{CC} = 1.2 V		-	145	-	-	-	ns
		V _{CC} = 2.0 V		-	51	93	-	110	ns
		V _{CC} = 2.7 V		-	38	69	-	82	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	[3]	-	25	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	30	56	-	66	ns
		V _{CC} = 4.5 V		-	29	48	-	56	ns
		V _{CC} = 6.0 V		-	21	37	-	44	ns
		Sn to Y _n ; see Figure 14	[2]						
		V _{CC} = 1.2 V		-	115	-	-	-	ns
		V _{CC} = 2.0 V		-	41	73	-	90	ns
		V _{CC} = 2.7 V		-	31	54	-	67	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	[3]	-	20	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	24	44	-	54	ns
		V _{CC} = 4.5 V		-	22	37	-	46	ns
		V _{CC} = 6.0 V		-	17	29	-	36	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC}	[4]	-	25	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.[2] t_{pd} is the same as t_{PLH} and t_{PHL}.t_{en} is the same as t_{PZL} and t_{PZH}.t_{dis} is the same as t_{PLZ} and t_{PHZ}.[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).P_D = C_{PD} × V_{CC}² × f_i × N + Σ((C_L + C_{SW}) × V_{CC}² × f_o) where:f_i = input frequency in MHz, f_o = output frequency in MHzC_L = output load capacitance in pFC_{SW} = maximum switch capacitance in pF;V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1 Waveforms

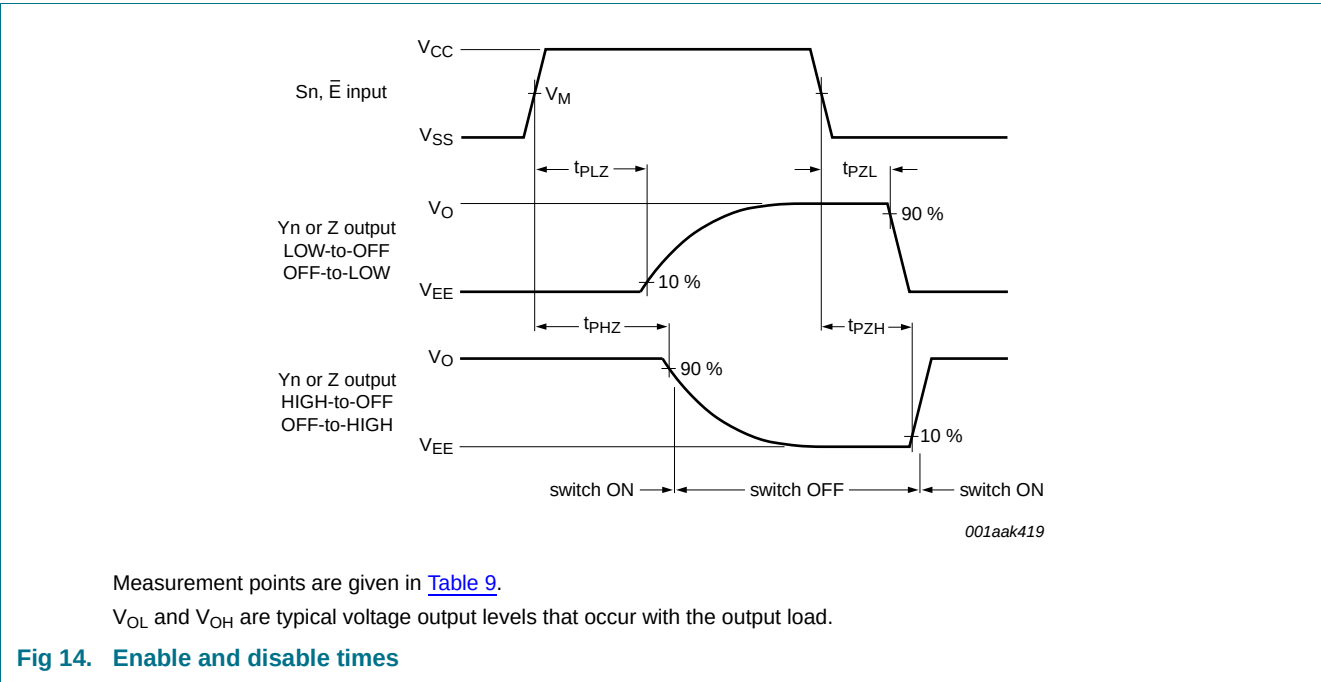
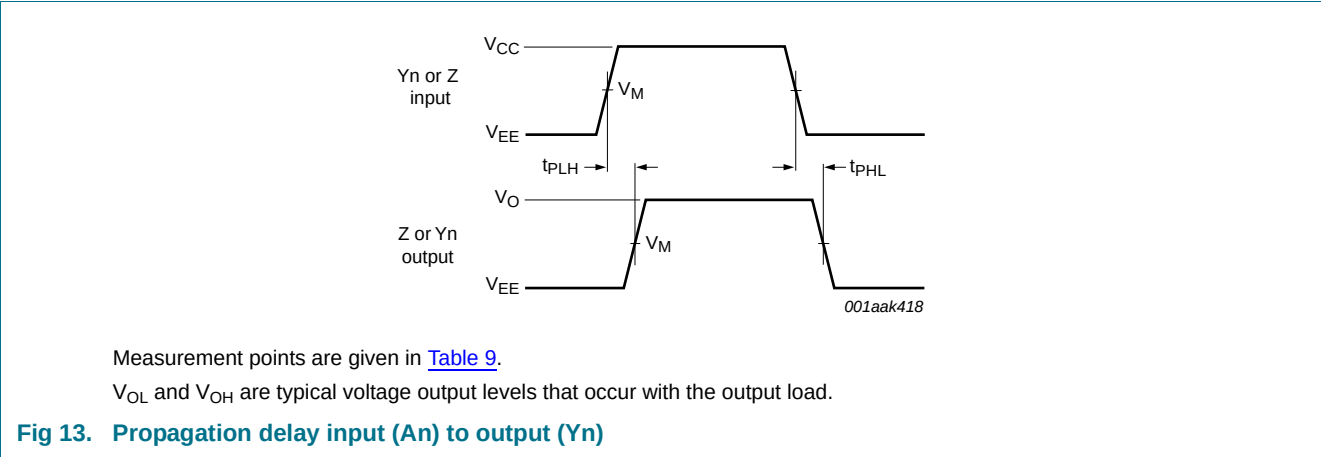
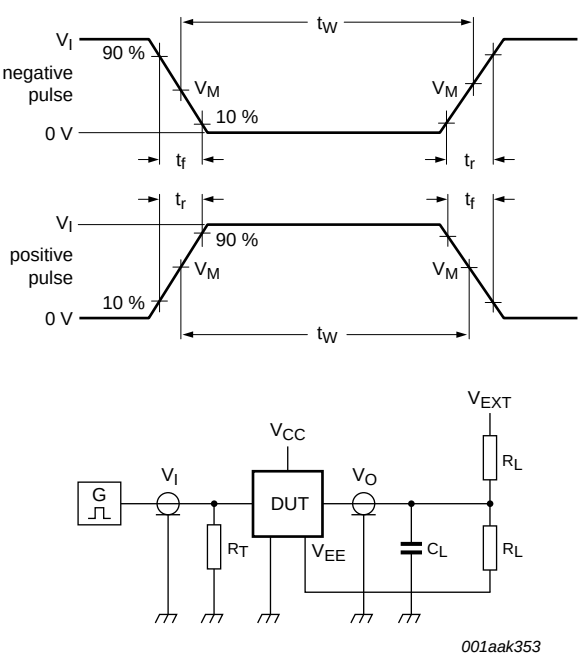


Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$

10.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

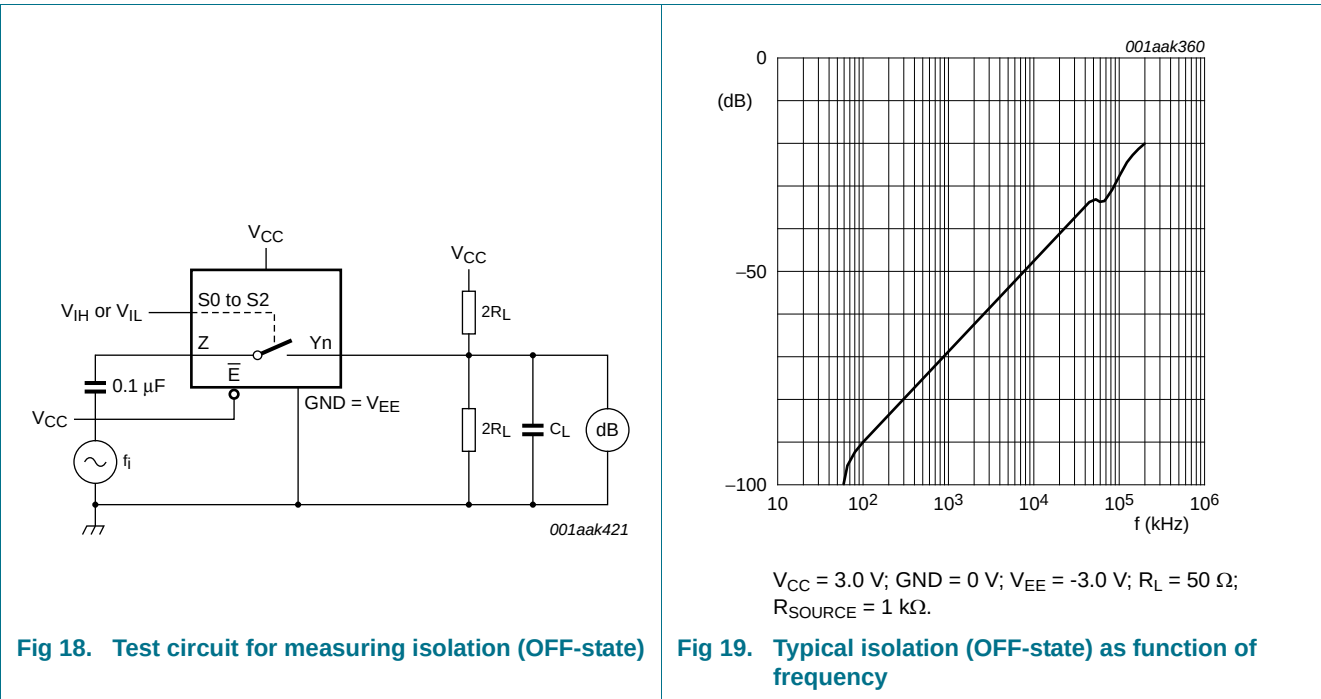
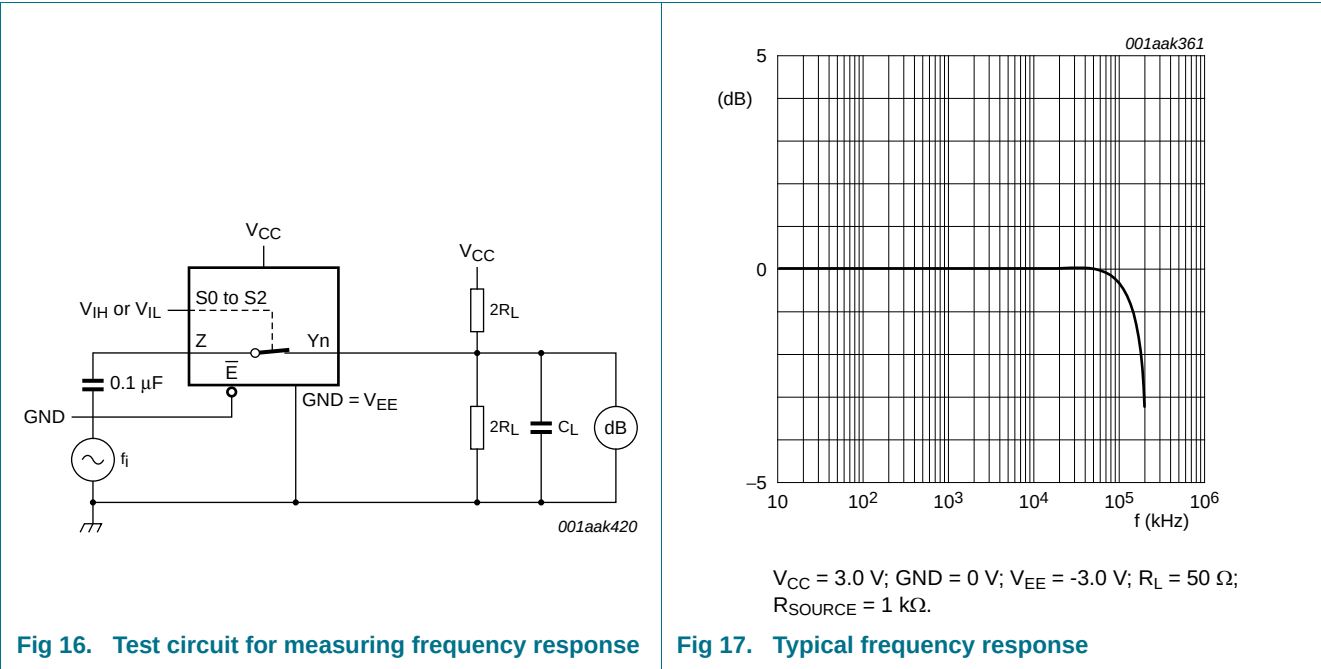
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0 \text{ ns}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Figure 20					
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$		-	0.8	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$		-	0.4	-	%
		$f_i = 10 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Figure 20					
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$		-	2.4	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$		-	1.2	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$C_L = 50 \text{ pF}$; $R_L = 50 \text{ }\Omega$; see Figure 16	[1]				
		$V_{CC} = 3.0 \text{ V}$		-	180	-	MHz
		$V_{CC} = 6.0 \text{ V}$		-	200	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Figure 18	[2]				
		$V_{CC} = 3.0 \text{ V}$		-	-50	-	dB
		$V_{CC} = 6.0 \text{ V}$		-	-50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Figure 21	[2]				
		$V_{CC} = 3.0 \text{ V}$		-	0.11	-	V
		$V_{CC} = 6.0 \text{ V}$		-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Figure 22					
		$V_{CC} = 3.0 \text{ V}$		-	-60	-	dB
		$V_{CC} = 6.0 \text{ V}$		-	-60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).

[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.2.1 Test circuits



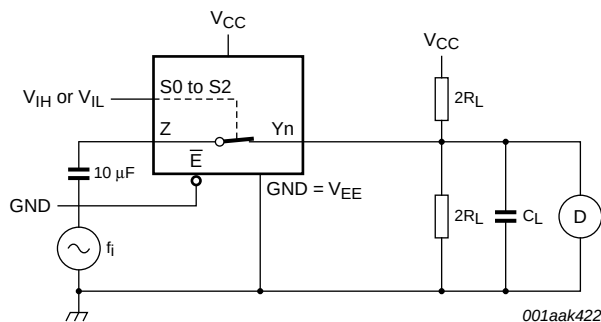
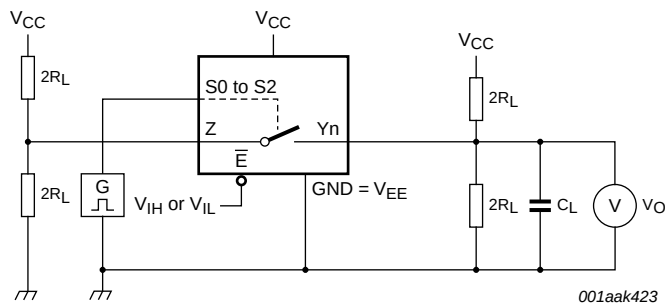
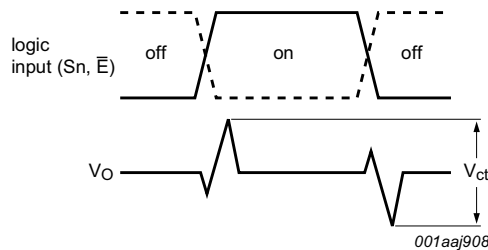


Fig 20. Test circuit for measuring total harmonic distortion



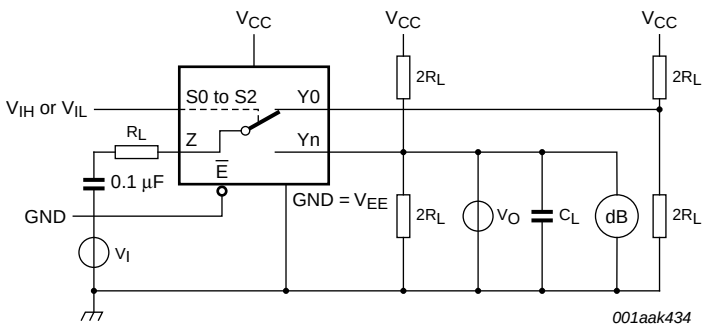
a. Test circuit



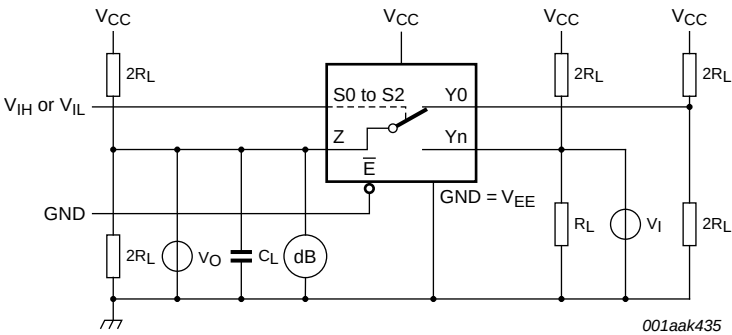
b. Input and output pulse definitions

V_I may be connected to S_n or $\bar{E}$.

Fig 21. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Fig 22. Test circuit for measuring crosstalk between switches

11. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

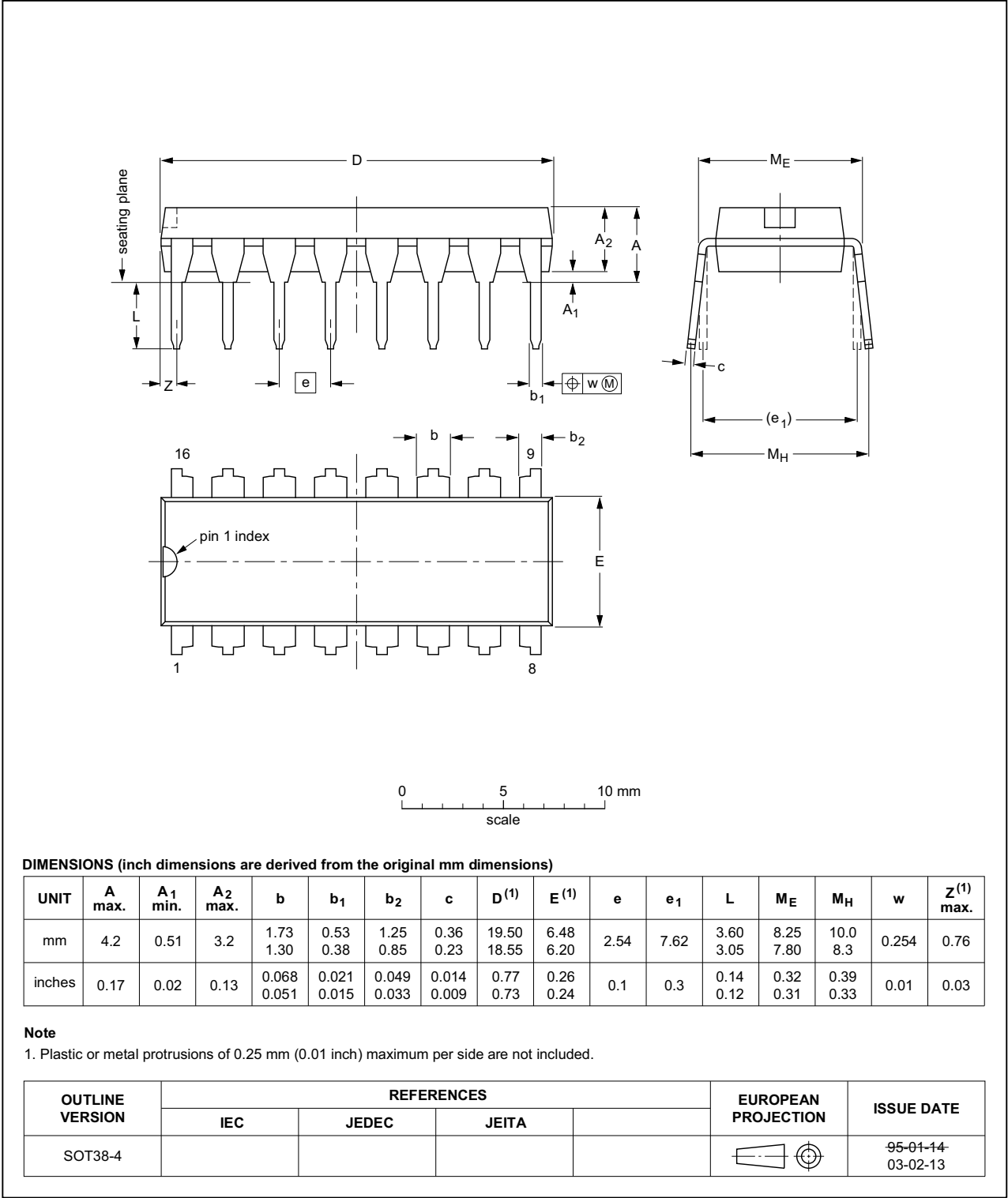


Fig 23. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

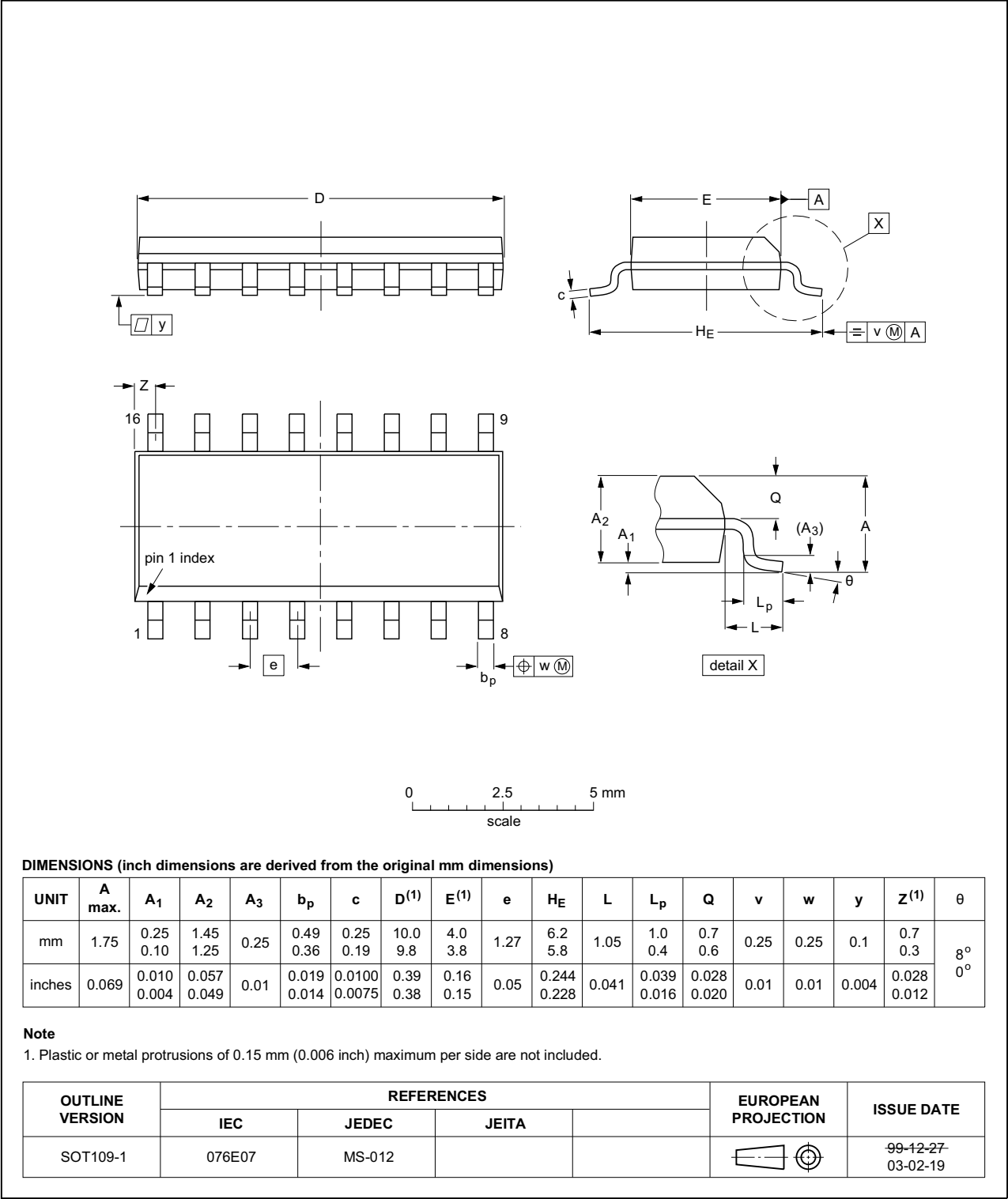


Fig 24. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

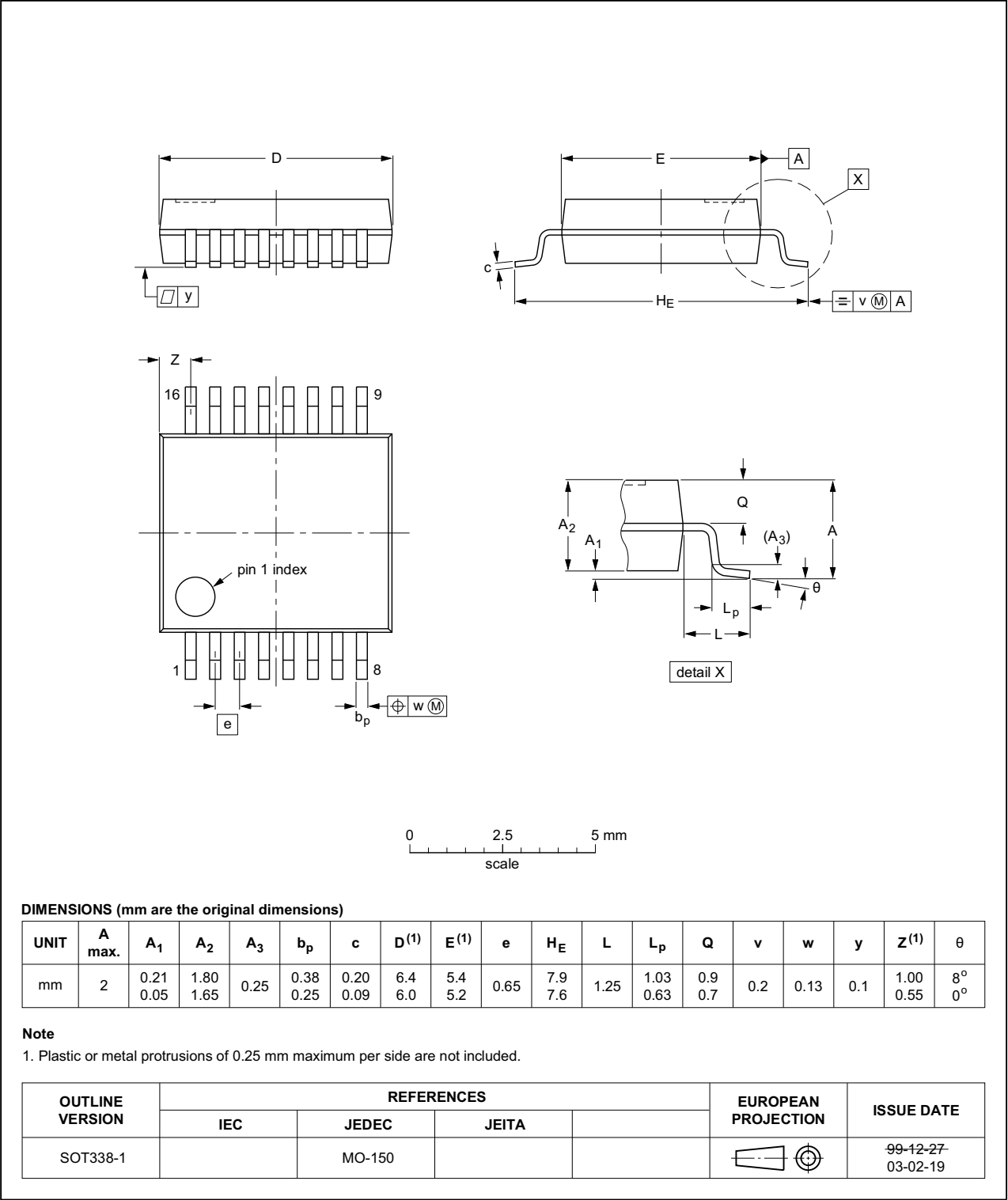


Fig 25. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

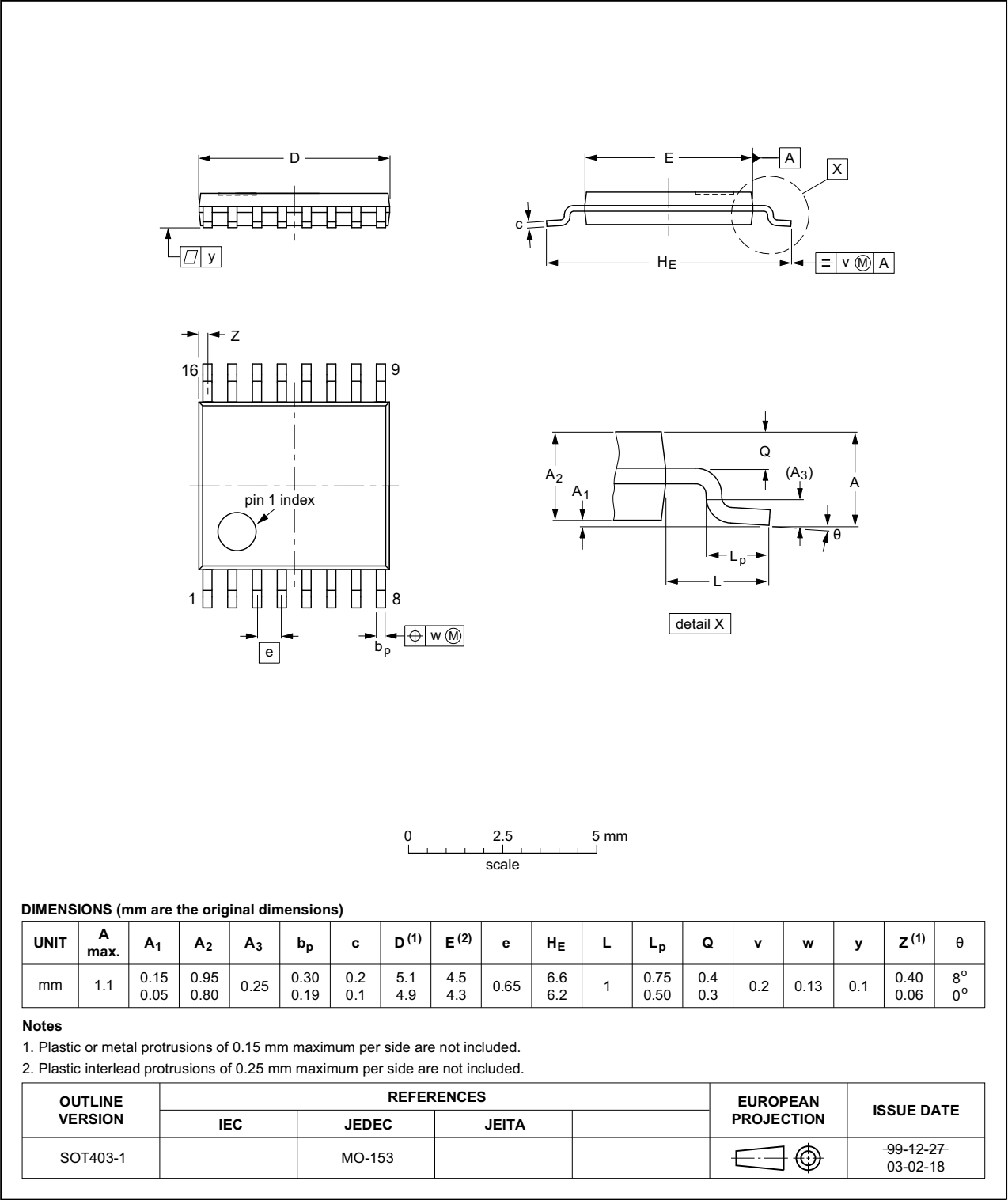


Fig 26. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

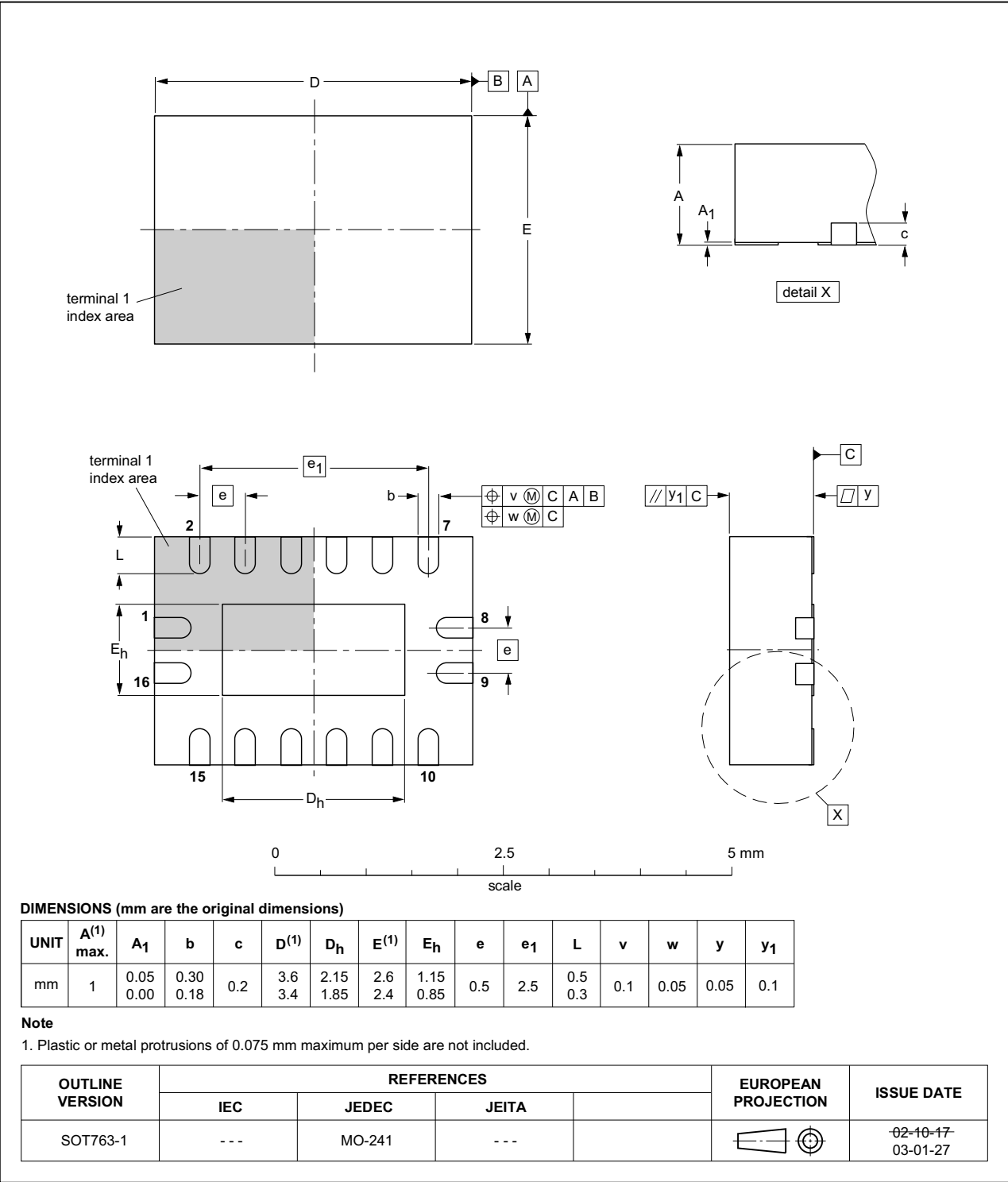


Fig 27. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4051 v.5	20140917	Product data sheet	-	74LV4051 v.4
Modifications:	Figure 7: Figure note added for DHVQFN16 package			
74LV4051 v.4	20090810	Product data sheet	-	74LV4051 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Added type number 74LV4051BQ (DHVQFN16 package)			
74LV4051 v.3	19960623	Product specification	-	74LV4051 v.2
74LV4051 v.2	19970715	Product specification	-	74LV4051 v.1

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 17 September 2014

Document identifier: 74LV4051

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