

FEATURES

- *Guaranteed Offset Voltage*
0°C to 70°C
- Low Drift
- *Guaranteed Bias Current*
70°C Warmed Up
- *Guaranteed Slew Rate*

1.5mV Max.
 2.2mV Max.
 4 μ V/°C Typ.

400pA Max.
 9V/ μ s Min.

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters
- Fast, Precision Sample and Hold

DESCRIPTION

The LT1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time in an SO package, 14V/ μ s slew rate and 5.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 0.5mV, 4 μ V/°C drift, and bias currents of 60pA at 70°C.

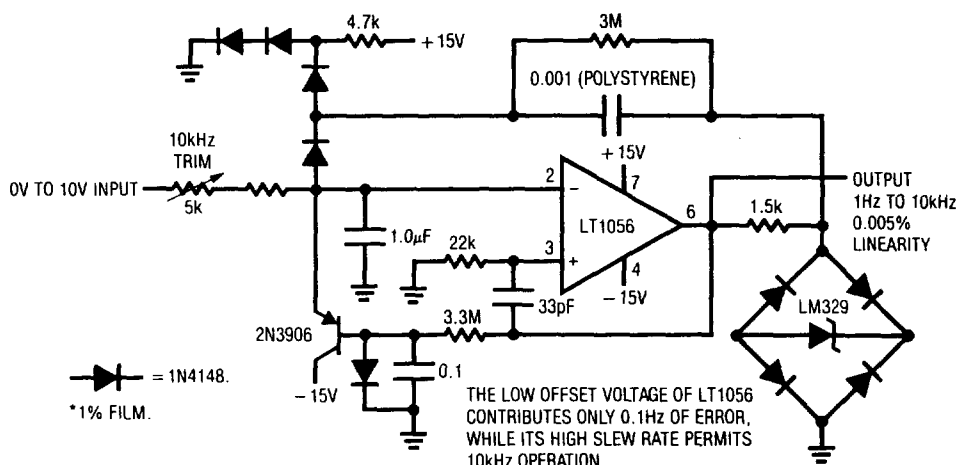
The 1.5mV maximum offset voltage specification is the best available on any JFET input operational amplifier in the plastic SO package.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage to frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

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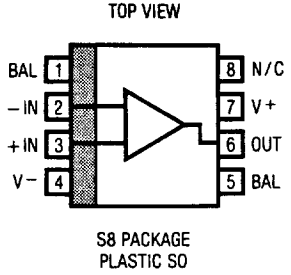
0 to 10kHz Voltage-to-Frequency Converter



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 20V$
Differential Input Voltage	$\pm 40V$
Input Voltage	$\pm 20V$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Devices	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>S8 PACKAGE PLASTIC SO</p>	ORDER PART NUMBER	
	LT1055S8 LT1056S8	
	PART MARKING	
	1055 1056	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055S8 LT1056S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)			500	1500	μV
I_{OS}	Input Offset Current	Fully Warm Up		5	30	pA
I_B	Input Bias Current	Fully Warm Up $V_{CM} = +10V$		± 30 30	± 100 150	pA pA
	Input Resistance — Differential	$V_{CM} = -11V$ to $+8V$ $V_{CM} = +8V$ to $+11V$		0.4		$T\Omega$
	— Common-Mode			0.4		$T\Omega$
				0.05		$T\Omega$
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055 LT1056		2.5 3.5		$\mu Vp-p$ $\mu Vp-p$
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 2) $f_o = 1kHz$ (Note 2)		35 15	70 22	nV/\sqrt{Hz} nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz, 1kHz$ (Note 3)		2.5	10	fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 2k$ $R_L = 1k$	120 100	400 300		V/mV V/mV
	Input Voltage Range		± 11	± 12		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	83	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	104		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13.2		V
SR	Slew Rate	LT1055 LT1056	7.5 9.0	12 14		$V/\mu s$ $V/\mu s$
GBW	Gain-Bandwidth Product	$f = 1MHz$ LT1055 LT1056		4.5 5.5		MHz MHz
I_S	Supply Current	LT1055 LT1056		2.8 5.0	4.0 7.0	mA mA
	Offset Voltage Adjustment Range	$R_{POT} = 100k$		± 5		mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055S8/1056S8			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)		●		800	2200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		4	15	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up $T_A = 70^\circ C$	●		18	150	pA
I_B	Input Bias Current	Warmed Up $T_A = 70^\circ C$	●		± 60	± 400	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	60	250		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	103		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 13.1		V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured under two different conditions:

(a) approximately 0.5 seconds after application of power; (b) at $T_A = 25^\circ C$ only, with the chip heated to approximately $38^\circ C$ for the LT1055 and to $45^\circ C$ for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to $1G\Omega$ swamps the contribution of current noise.

Note 4: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+ .

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