

Low-Voltage Octal Buffer/Line Driver with 5 V Tolerant Inputs and Outputs

74LCX541

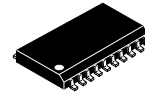
The LCX541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The LCX541 is a non-inverting option of the LCX540.

This device is similar in function to the LCX244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

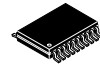
The LCX541 is designed for low voltage applications with capability of interfacing to a 5 V signal environment. The LCX541 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Input and Outputs
- 1.65 V–5.5 V V_{CC} Specifications Provided
- 6.5 ns t_{PD} Max. ($V_{CC} = 3.3$ V), 10 μ A I_{CC} Max.
- Power-down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal
- ± 24 mA Output Drive ($V_{CC} = 3.0$ V)
- Implements Proprietary Noise/ EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance
 - ◆ Human Body Model > 2000 V
- Pb-Free DQFN Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

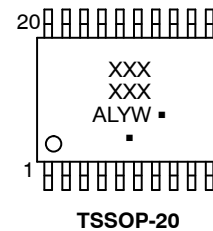
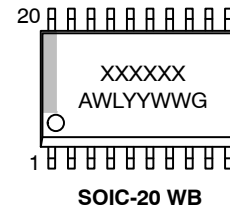


SOIC-20 WB
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Connection Diagrams

Pin Assignments for
SOIC, SOP, SSOP, TSSOP

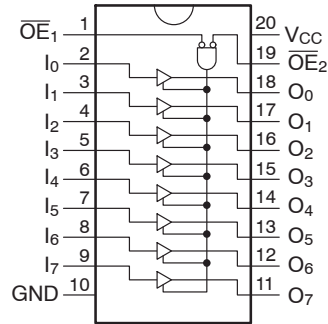


Figure 1.

Logic Symbol

IEEE/IEC

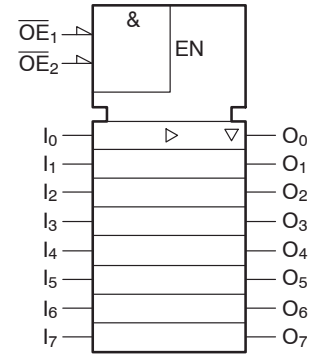
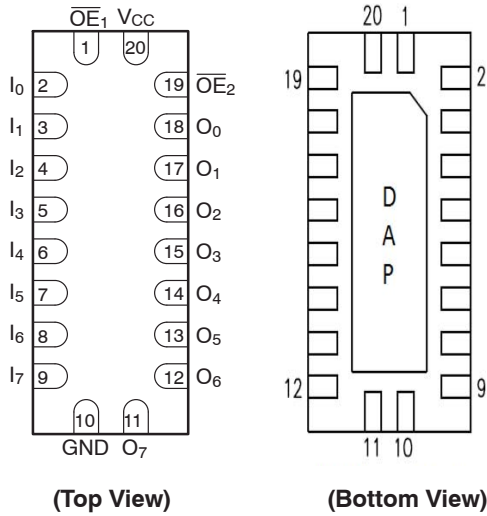


Figure 2.

Pad Assignment for DQFN



(Top View)

(Bottom View)

Figure 3.

PIN DESCRIPTION

Pin	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0 – I_7	Inputs
O_0 – O_7	Outputs
DAP	No Connect

TRUTH TABLE

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I_n	O_n
L	L	H	H
L	X	X	Z
X	H	X	Z
L	L	L	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance State

74LCX541

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)	-0.5 to +6.5	V
V_O	DC Output Voltage (Note 1) Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC}+0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SOIC-20W WQFN20 TSSOP-20	96 99 150	°C/W
P_D	Power Dissipation in Still Air SOIC-20W WQFN20 TSSOP-20	1302 1256 833	mW
MSL	Moisture Sensitivity SOIC-20W All Other Packages	Level 3 Level 1	-
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Digital Input Voltage	0	5.5	V
V_O	Output Voltage Active Mode (High or Low State) Tri-State Mode Power Down Mode ($V_{CC} = 0$ V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature	-40	+125	°C
t_r, t_f	Input Rise or Fall Rate $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0$ V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

74LCX541

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V _{CC}		0.65 x V _{CC}		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V _{CC}		0.7 x V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65 to 1.95		0.35 x V _{CC}		0.35 x V _{CC}	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V _{CC}		0.3 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}						V
		I _{OH} = -100 μA	1.65 to 5.5	V _{CC} - 0.1	-	V _{CC} - 0.1	-	
		I _{OH} = -4 mA	1.65	1.2	-	1.2	-	
		I _{OH} = -8 mA	2.3	1.8	-	1.8	-	
		I _{OH} = -12 mA	2.7	2.2	-	2.2	-	
		I _{OH} = -16 mA	3.0	2.4	-	2.4	-	
		I _{OH} = -24 mA	3.0	2.2	-	2.2	-	
		I _{OH} = -32 mA	4.5	3.8		3.8		
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL}						V
		I _{OL} = 100 μA	1.65 to 5.5	-	0.1	-	0.1	
		I _{OL} = 4 mA	1.65	-	0.45	-	0.45	
		I _{OL} = 8 mA	2.3	-	0.6	-	0.6	
		I _{OL} = 12 mA	2.7	-	0.4	-	0.4	
		I _{OL} = 16 mA	3.0	-	0.4	-	0.4	
		I _{OL} = 24 mA	3.0	-	0.55	-	0.55	
		I _{OL} = 32 mA	4.5		0.6		0.6	
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	-	±5.0	-	±5.0	μA
I _{OZ}	3-State Output Leakage Current	V _I = V _{IH} or V _{IL} , V _O = 0 V to 5.5 V	3.6	-	±5.0	-	±5.0	μA
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V or V _O = 5.5 V	0	-	10	-	10	μA
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	2.3 to 3.6	-	10	-	10	μA
		3.6 V ≤ V _I , V _O ≤ 5.5 V (Note 5)			±10.0		±10.0	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6 V	2.3 to 3.6	-	500	-	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Outputs disabled or 3-STATE only.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, D to O	See Figures 4 and 5	1.65 to 1.95	–	10.3	–	10.3	ns
			2.3 to 2.7	–	7.8	–	7.8	
			2.7	–	7.5	–	7.5	
			3.0 to 3.6	–	6.5	–	6.5	
			4.5 to 5.5	–	5.9	–	5.9	
t _{PZH} , t _{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 4 and 5	1.65 to 1.95	–	13.0	–	13.0	ns
			2.3 to 2.7	–	10.5	–	10.5	
			2.7	–	9.5	–	9.5	
			3.0 to 3.6	–	8.5	–	8.5	
			4.5 to 5.5	–	7.3	–	7.3	
t _{PHZ} , t _{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 4 and 5	1.65 to 1.95	–	11.0	–	11.0	ns
			2.3 to 2.7	–	9.0	–	9.0	
			2.7	–	8.5	–	8.5	
			3.0 to 3.6	–	7.5	–	7.5	
			4.5 to 5.5	–	6.5	–	6.5	
t _{OSHL} , t _{OSLH}	Output to Output Skew (Note 6)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_{in} + I_{CC} \times V_{CC}$.

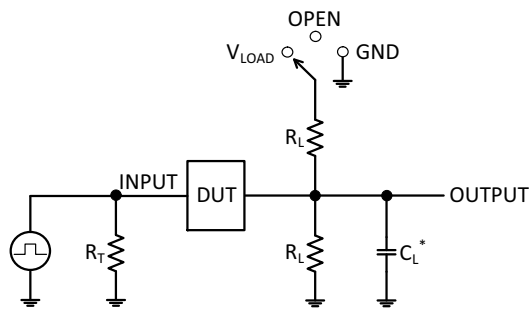
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C	Unit
				Typ	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	–0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	–0.6	

CAPACITANCE

Symbol	Parameter	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0 V or V _{CC}	7.0	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8.0	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC} , f = 10 MHz	25.0	pF

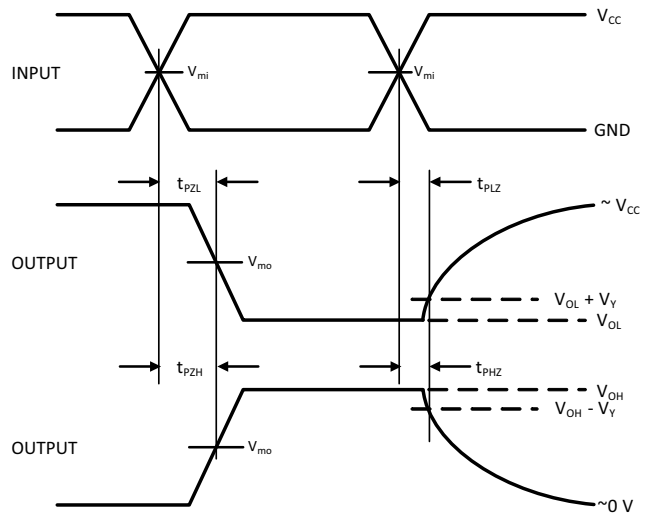
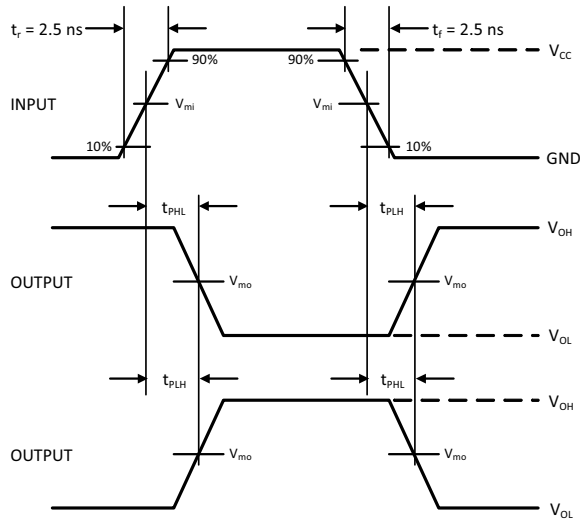
74LCX541



* C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

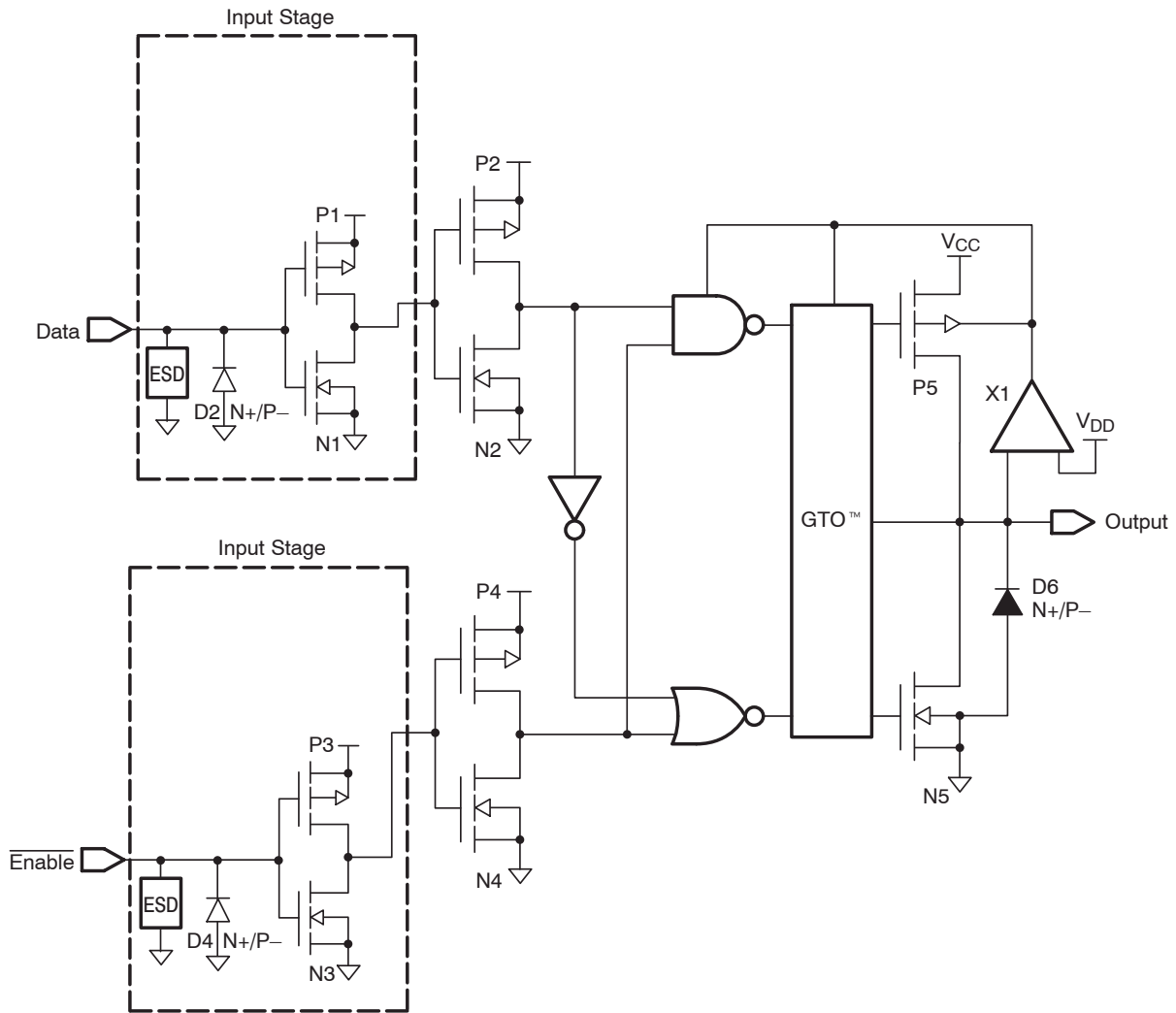
Figure 4. Test Circuit



V_{CC} , V	R_L , Ω	C_L , pF	V_{LOAD}	V_{mi} , V	V_{mo} , V	V_Y , V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	$V_{CC}/2$	0.3
3.0 to 3.6	500	50	6 V	1.5	$V_{CC}/2$	0.3
4.5 to 4.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	$V_{CC}/2$	0.3

Figure 5. Switching Waveforms

74LCX541



**Figure 6. Schematic Diagram
(Generic for LCX Family)**

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LCX541WMX	LCX541	SOIC-20 WB	1000 / Tape & Reel
74LCX541MTC	LCX 541	TSSOP-20	75 Units / Tube
74LCX541MTCX	LCX 541	TSSOP-20	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales