12G UHD-SDI Cable Driver

Key Features

- Dual non-inverted 75Ω cable interface with on-chip termination
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 11.88Gb/s
- Cable driver features:
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Manual output slew rate control
  - Manual or automatic Mute or disable on LOS
- Trace equalizer features:
  - Integrated 100Ω, differential input termination
  - Automatic power down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace equalization to compensate for up to 15" FR4 at 11.88Gb/s
  - Input offset compensation

Additional Features

- Single 1.8V power supply for analog and digital core
- 2.5V or 3.3V for cable driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40ºC to +85ºC
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS and WEEE compliant package
- Pin compatible with the GS12181, GS12182, GS12281, and GS3281

Applications

Next Generation 12G UHD-SDI infrastructures designed to support UHDTV1, UHDTV2, 4K D-Cinema and 3D HFR and HDR production image formats. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

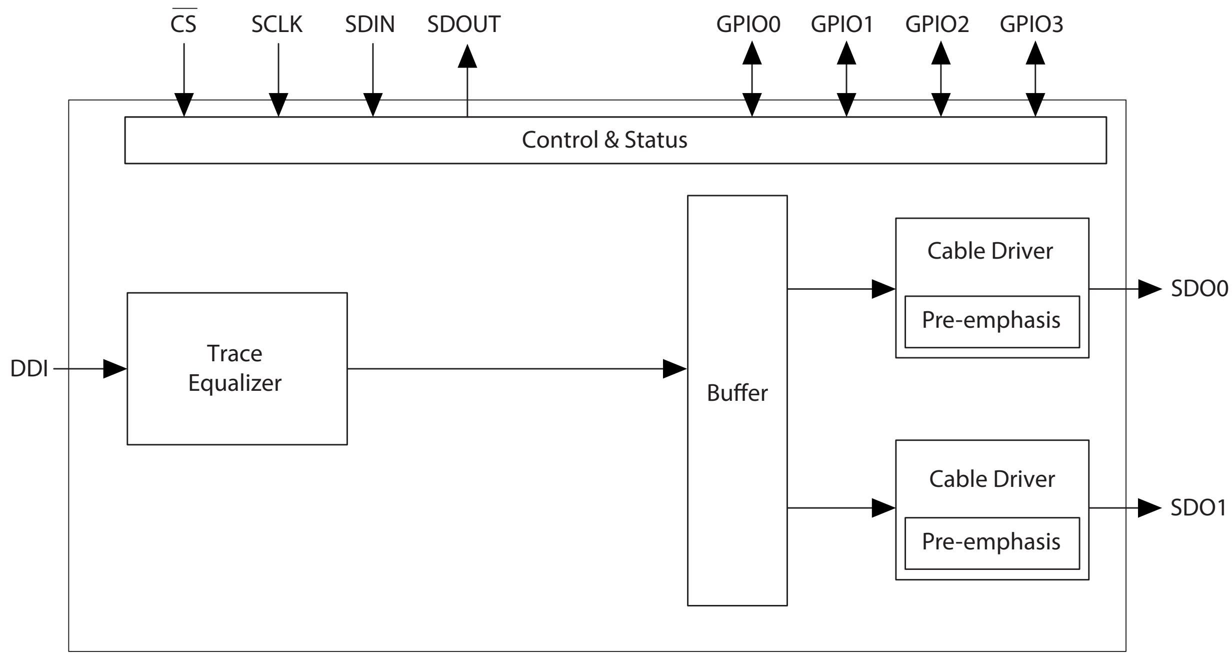
Description

The GS12081 is a low-power, multi-rate, cable driver supporting rates up to 12G UHD-SDI. It is designed to receive 100Ω differential input signals, and transmit the signal over 75Ω coaxial cables. The 100Ω trace input supports up to 17dB of insertion loss.

The two cable drivers have highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses. Additionally, user selectable output slew rate control is provided for each cable driver output.

The GS12081 is pin compatible with the GS12181 and GS12281 single input, and the GS12182 dual input 12G UHD-SDI Multi-rate Re-timing Cable Drivers, as well as the GS3281 3G SDI Multi-rate Re-timing Cable Driver.

Note: For the GS12081 to be pin compatible with the GS12182, careful design considerations are required. Contact for your local Semtech FAE for details.



GS12081 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	038689	—	September 2017	Updated values in Table 2-2 and Table 2-3.
2	037841	—	August 2017	Added Section 4.5.12, and Section 4.3.2. Updated Section 4.5.13.
1	034026	—	November 2016	Figure 4-1, Section 4.4 updated. Added Section 4.5.11. Updates made to register map, Section 5.
0	031406	—	July 2016	New Document.

Contents

1. Pin Out

1.1 GS12081 Pin Assignment

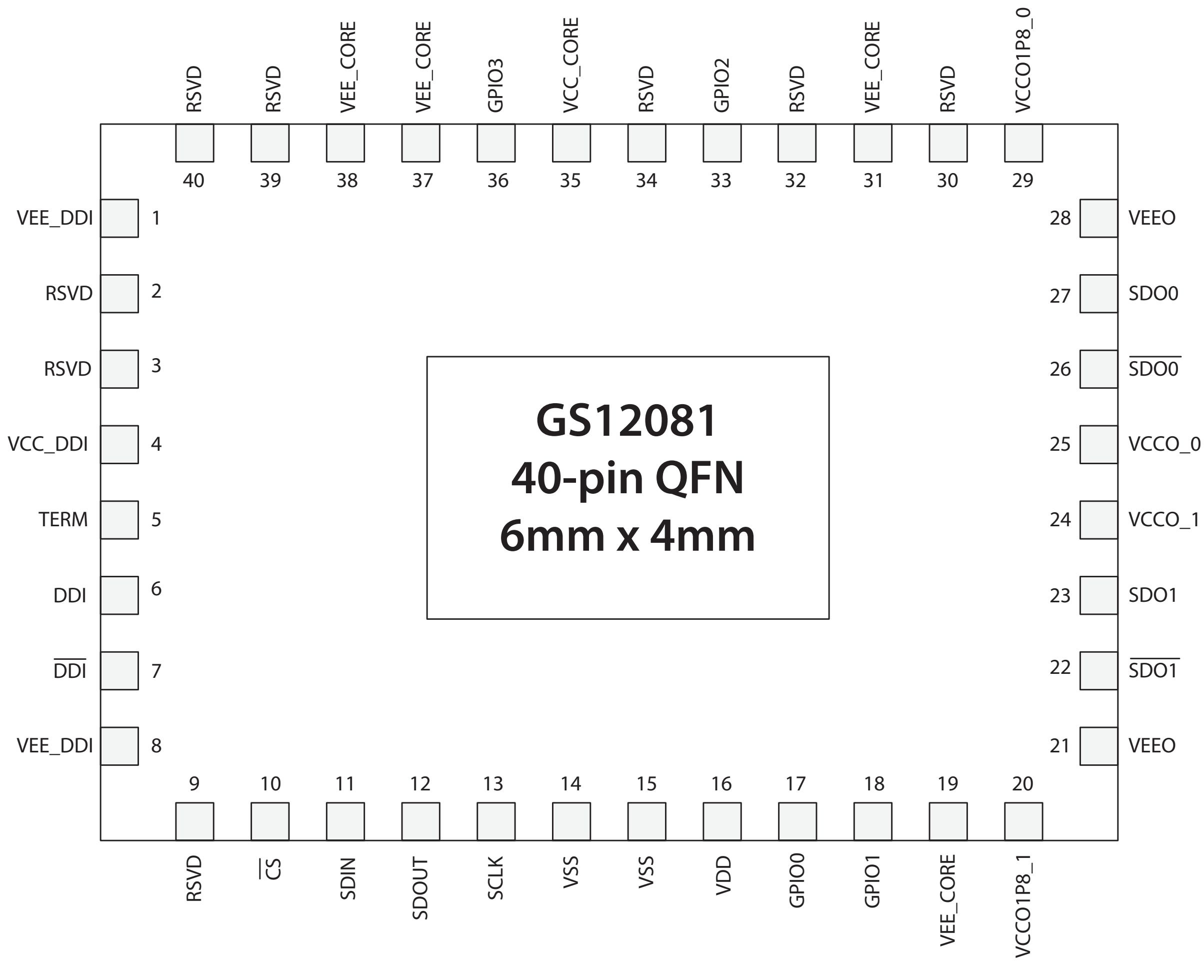


Figure 1-1: GS12081 Pin Assignment

1.2 GS12081 Pin Descriptions

Table 1-1: GS12081 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the Trace Equalizer. Connect to ground.
2, 3, 9, 30, 32, 34, 39, 40	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS12241.
4	VCC_DDI	Power	Most positive power supply connection for the Trace Equalizer. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
5	TERM	—	Input Common Mode termination. Decouple to ground. See Section 6.1 Typical Application Circuit for values.
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
10	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.5.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.5.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS12081 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = Unassigned. Configure to the most appropriate GPIO function for the intended application. Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	$\overline{\text{SDO1}}$,SDO1	Output	Differential CML output with two internal 75Ω pull-ups. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
24	VCCO_1	Power	Most positive power supply connection for the SDO1/ $\overline{\text{SDO1}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
25	VCCO_0	Power	Most positive power supply connection for the SDO/$\overline{\text{SDO0}}$ output driver. Connect to 2.5V or 3.3V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
26, 27	$\overline{\text{SDO0}}$, SDO0	Output	Differential CML output with two internal 75Ω pull-ups. **Note:** If one of the two outputs is not used by the application, ensure that it is connected to ground through a capacitor and resistor. See Section 6.1 Typical Application Circuit for values.
29	VCCO1P8_0	Power	Most positive power supply connection for cable driver pre driver. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set high to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V and decouple to ground. See Section 6.1 Typical Application Circuit for values.

Table 1-1: GS12081 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set high to disable SDO1/$\overline{\text{SDO1}}$ Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not commended to connect device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage—Core (VCC_DDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage—Output Driver (VCCO_0, VCCO_1)	-0.5V to +3.65V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (DDI, $\overline{\text{DDI}}$)	-0.3 to (VCC_DDI +0.3)V
Input Voltage Range (GPIO2, GPIO3 REF_CLK)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{\text{CS}}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_DDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		2.38	2.5	2.63	V	—
			3.14	3.3	3.47	V	—
Power - Mission Mode (SDO0/$\overline{\text{SDO0}}$ enabled SDO1/$\overline{\text{SDO1}}$ disabled)	P_D	VCCO_0 = 2.5V, Output Swing = 800mV_{pp}	—	170	—	mW	1
		VCCO_0 = 2.5V, Output Swing = 800mV_{pp} with pre-emphasis set to setting of 15	—	185	—	mW	—
		VCCO_0 = 3.3V, Output Swing = 800mV_{pp}	—	190	—	mW	1
		VCCO_0 = 3.3V, Output Swing = 800mV_{pp} with pre-emphasis set to setting of 15	—	210	—	mW	—
Power - Mission Mode (SDO0/$\overline{\text{SDO0}}$ disabled SDO1/$\overline{\text{SDO1}}$ disabled)	P_D		—	75	—	mW	1
Power - Sleep Mode	P_D	Sleep	—	40	—	mW	—
Supply Current - Cable Driver	I_{CCO_0}, I_{CCO_1}	VCCO_0 = 2.5V, Output Swing = 800mV_{pp}	—	23	34	mA	1,4
		VCCO_0 = 2.5V, Output Swing = 800mV_{pp}, with pre-emphasis set to setting of 15	—	29	38	mA	4
		VCCO_0 = 3.3V, Output Swing = 800mV_{pp}	—	24	35	mA	1,4
		VCCO_0 = 3.3V, Output Swing = 800mV_{pp}, with pre-emphasis set to a setting of 15	—	30	39	mA	4
	I_{CCO1P8_0}, I_{CCO1P8_1}	Output Swing = 800mV_{pp}	—	20	28	mA	4
Supply Current – Analog Core	I_{CC_CORE}	SDO0/$\overline{\text{SDO0}}$ disabled, SDO1/$\overline{\text{SDO1}}$ disabled	—	6	12	mA	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current - Trace Equalizer	I_{CC_DDI}		—	21	32	mA	—
Supply Current - Digital Logic	I_{DD}		—	15	18	mA	—
DDI Input Common Mode Voltage	V_{CMIN}		0.94	—	2.525	V	2
SDO Output Common Mode Voltage	V_{CMOUT}		—	$V_{CMOUT} = V_{CCO} - \Delta V_{SDO}/2$	—		—
DDI Input Termination		Differential	—	100	—	Ω	—
SDO Output Termination		Between SDO and GND	—	75	—	Ω	3
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.
2. 0.94V is when trace EQ is DC coupled to upstream driver running from 1.2V supply, and 2.525V is when trace EQ is DC coupled to upstream driver running from 2.5V supply.
3. Applies to both SDO0 and SDO1.
4. The specifications provided are per symbol, not a combined value.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDI}	—	0.001	—	11.88	Gb/s	—
Serial Output Voltage Swing	V_{SDO}	—	720	800	880	mV_{pp}	3
Differential Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	—
Input Trace Equalization	—	12G	—	15	—	Inches	14dB, 5,7
		6G	—	20	—	Inches	12dB, 5
		3G	—	40	—	Inches	13dB, 5
		HD	—	40	—	Inches	6dB, 5
		SD	—	40	—	Inches	3dB, 5
		MADI	—	40	—	Inches	3dB, 5
Intrinsic Input Jitter Tolerance Square Wave Modulation	IIJT	12G	0.7	0.85	—	UI	—
		MADI/SD/HD/3G/6G	0.8	0.95	—	UI	—
SDO/$\overline{SDO}$ Rise/Fall Time	$t_{riseSDO}$, $t_{fallSDO}$	SD	400	—	1000	ps	4
		HD/3G	—	—	70	ps	4
		6G/12G	—	—	40	ps	4
SDO/$\overline{SDO}$ Mismatch in Rise/Fall Time	—	SD	—	—	100	ps	4
		HD/3G	—	—	20	ps	4
		6G/12G	—	—	10	ps	4
SDO/$\overline{SDO}$ Eye Cross Shift	—	SD	—	—	5	%	4
		HD/3G	—	—	8	%	4
		6G/12G	—	—	9	%	4
SDO/$\overline{SDO}$ Overshoot	—	—	—	—	10	%	4
Output Return Loss	—	5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
		2.97GHz to 5.94GHz	—	—	-8	dB	1
		5.94GHz to 11.88GHz	—	—	-5	dB	1

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD = 1.8V ±5% and VCCO_0, VCCO_1 = +2.5/3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Output Jitter (SDO/$\overline{SDO}$)	$t_{OJ(11.88Gb/s)}$	Pattern = PRBS	—	0.06	0.2	UI_{pp}	2, 4, 6
	$t_{OJ(5.94Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(2.97Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(1.485Gb/s)}$		—	0.03	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(270Mb/s)}$		—	0.04	0.15	UI_{pp}	2, 4, 6
	$t_{OJ(125Mb/s)}$		—	0.02	0.1	UI_{pp}	2, 4, 6

Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default driver swing Setting.
4. This specification applies to SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$.
5. Trace insertion loss was measured with FR4 material using 7 mil stripline traces using a PRBS23 signal.
6. Measured under minimal trace loss conditions.
7. Measured with an input launch swing of 800mVpp and trace equalizer set to 8.

Note: For GSPI Timing see Table 4-4: GSPI Timing Parameters.

3. Input/Output Circuits

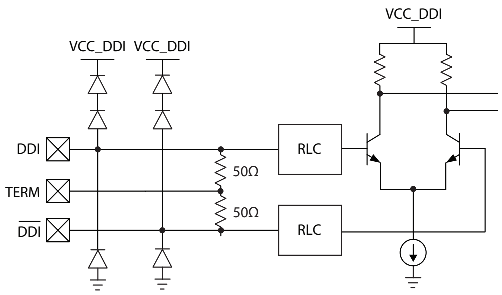


Figure 3-1: DDI, $\overline{\text{DDI}}$

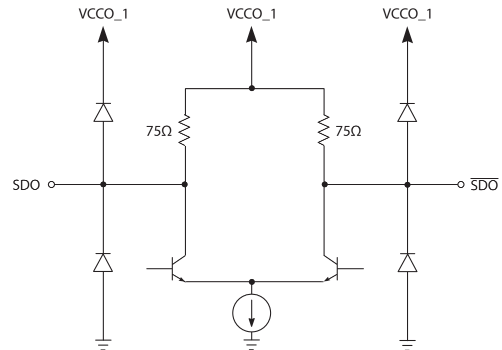


Figure 3-2: SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$

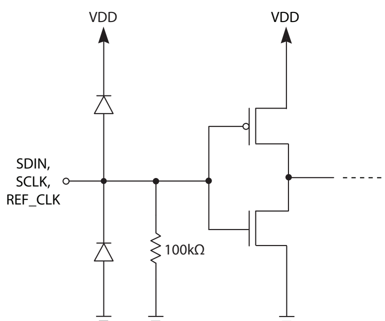


Figure 3-3: SDIN, SCLK

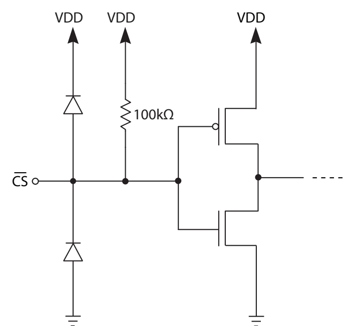


Figure 3-4: $\overline{\text{CS}}$

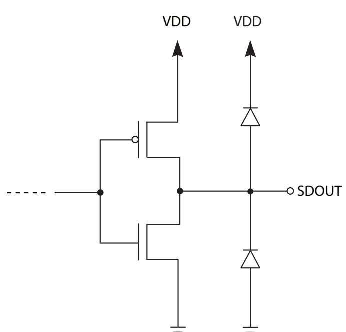


Figure 3-5: SDOUT

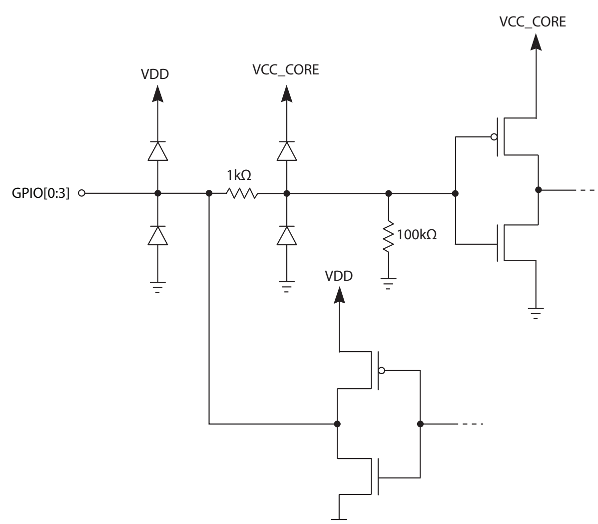


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS12081 is a dual output SMPTE compliant cable driver with integrated 75Ω internal terminations. It includes a 100Ω differential trace equalizer to receive the outgoing signal from the system. The Trace Equalizer has manual offset correction and boost control, which can compensate for 17dB of insertion loss at 5.94GHz. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The pre-emphasis control is two dimensional, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.1.1 Sleep Mode

To enable low power operation, the GS12081 has manual and automatic sleep mode control.

The default mode is automatic sleep mode on LOS (Loss of signal). The device can also be manually put into sleep mode. When the device is in sleep mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The cable driver can be configured to be disabled or muted during sleep.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (auto sleep). While in auto sleep mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b manual sleep control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default GPIO pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

4.2 Trace Equalizer

The GS12081 features a differential input buffer with 100Ω differential input termination, which includes a trace equalizer that can be configured to compensate for up to 15" of 7-mil stripline of FR4 at 11.88Gb/s and up to 40" at 3Gb/s.

The differential input signal can be either DC-coupled or AC-coupled and is capable of operation with any binary coded signal that between 1Mb/s and 11.88Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC coupled using industry standard 100Ω differential termination circuitry.

The trace equalizer includes a manual input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the trace equalizer.

Note: The parameters referred to within Section 4.2.1 to Section 4.2.2 are linked to their respective registers in Table 4-1. For a complete list of registers and functions, please see Section 5.

4.2.1 Input Trace Equalization

The trace equalizer can compensate for up to 17dB of insertion loss at 5.94GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (2_h). Please refer to Figure 4-1 for recommended boost setting.

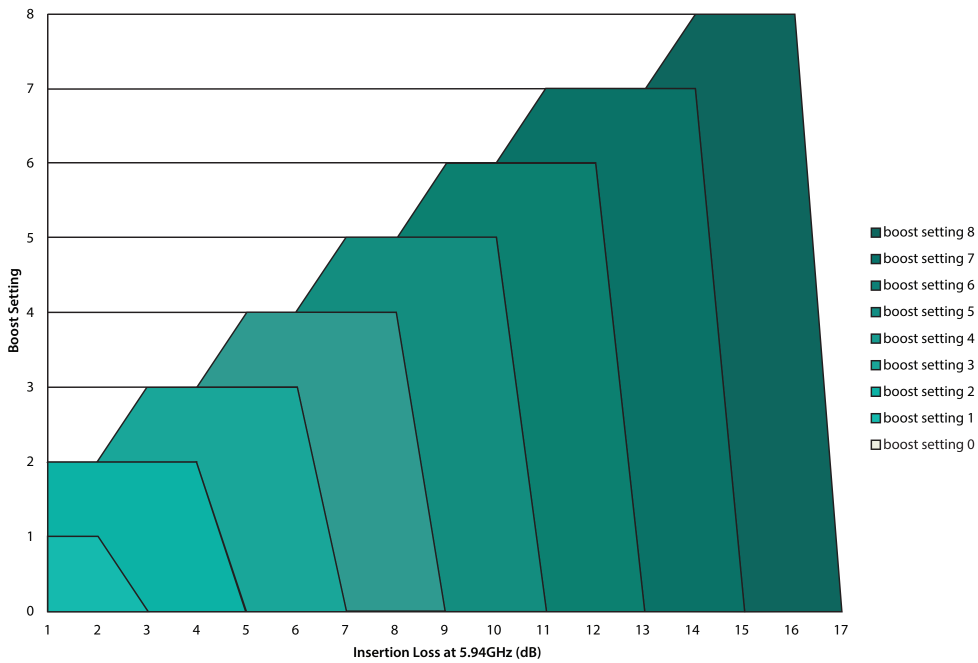


Figure 4-1: GS12081 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7-mil stripline in FR4 material at high frequencies.

Note: Although not a requirement, launch swing of $800mV_{ppd}$ is recommended for trace lengths longer than 5".

4.2.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including mute on LOS, which will be covered in the output section of this document.

The default settings of the trace equalizer Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the trace equalizer is highly configurable and allows the system designer to optimize the sensitivity and hysteresis of the Carrier Detection mechanism to meet specific system requirements.

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main input signal, controlled by **CFG_TREQ0_BOOST**, by setting **CFG_TREQ0_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the output.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are is 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register 0x49). See Section 4.3.4 for more details.

Given a differential input trace with 17dB of insertion loss at 5.94GHz and **CFG_TREQ0_CD_BOOST** = 0_b, Figure 4-2 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 11.88Gb/s.

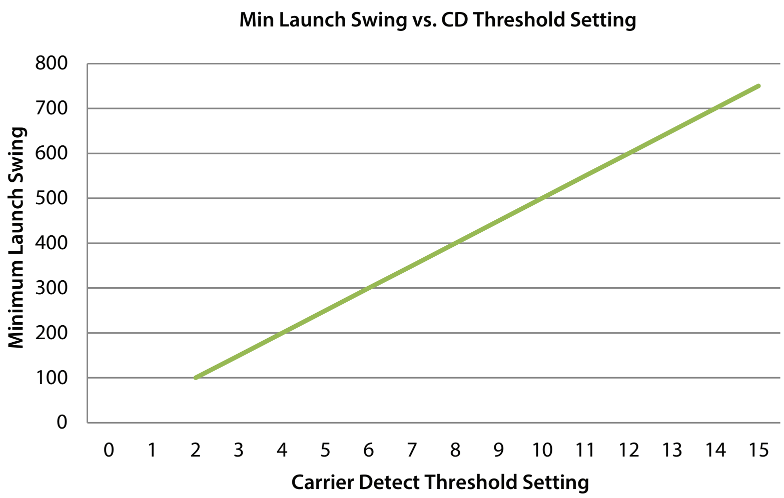


Figure 4-2: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-1: Trace Equalizer Configuration and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
1F, TREQ0_CD_ HYSTERESIS	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.
	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
1E, TREQ0_ INPUT_BOOST	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.
	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary carrier detection status.

4.3 Output Drivers

The GS12081 features two independently configurable output drivers (see Figure 3-3). The two drivers provide highly configurable amplitude and pre-emphasis control. The signal on the outputs can be inverted to help with signal polarity when layout requires trace inversion. The LOS (Loss of Signal) status from the equalizer stage can be used to automatically mute or disable the outputs on their assertion. The cable drivers can be configured to mute or disable during sleep. The sleep control modes take precedence over the manual or automatic LOS output control modes.

Note: The <n> in the control parameter names refers to the output number. Output 0 is the cable driver output *SDO0*/$\overline{SDO0}$, and output 1 is the cable driver output *SDO1*/$\overline{SDO1}$.

4.3.1 Output Driver Polarity Inversion

The signal polarity may be inverted at the outputs through the **CTRL_OUTPUT<n>_ DATA_ INVERT** parameters in register 0x48. This may be useful to compensate for an inverted upstream signal or to facilitate board signal routing. To invert the polarity of either of the two output drivers, write 1_b to control parameter **CTRL_OUTPUT<n>_DATA_ INVERT**.

4.3.2 Output Driver Data Rate Selection

By default the GS12081 will use the 6G/12G output driver and slew rate group settings for all data rates.

If the application will be using data rates other than 6G/12G, it is recommended that specific data rate group settings are used at all times for optimal performance.

To use specific data rate group settings, the host will need to set **CTRL_OUTPUT<n>_MANUAL_SLEW** to the required rate group. The slew rate options are as follows:

0 = SD/MADI
1 = HD/3G
2 = 6G/12G (default)

Note: It is recommended to enable offset correction for rates HD through 12G to minimize output jitter. This is done by setting **CFG_OFFSET_MANUAL_ENA** = 1 in register 0x1B.

4.3.3 Amplitude and Pre-Emphasis Control

The two output drivers offer very granular amplitude and pre-emphasis control. For optimal loss compensation, both the pre-emphasis pulse amplitude and the pre-emphasis pulse width can be independently configured on both output drivers. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of interconnect composed of trace, connector and via losses. The swing and pre-emphasis can be independently configured for specific data rates.

Note: The following are important points regarding this section.

- The parameters referred to within this section are linked to their respective registers in Table 4-2. For a complete list of registers and functions, see Section 5.
- To configure the GS12081 for specific rate group settings, see Section 4.3.2.

The output swing can be configured for the following three rate groups:

CFG_OUTPUT<n>_CD_SD_DRIVER_SWING (MADI and SD)
CFG_OUTPUT<n>_CD_HD_DRIVER_SWING (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_DRIVER_SWING (6G and 12G)

The output pre-emphasis can be configured for the following two rate groups:

CFG_OUTPUT<n>_CD_HD_PREEMPH_WIDTH (HD and 3G)
CFG_OUTPUT<n>_CD_HD_PREEMPH_AMPL (HD and 3G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_WIDTH (6G and 12G)
CFG_OUTPUT<n>_CD_UHD_PREEMPH_AMPL (6G and 12G)

The default swing setting is 800mVpp single ended into an external 75Ω load. The swing can be adjusted in ~20mV increments. Applications where maximum output swing and pre-emphasis range are desired, it is recommended that the output supplies *VCCO_0* and *VCCO_1* be connected to a 3.3V supply. For most applications with short trace between GS12081 and output BNC, 2.5V power supply can be used.

4.3.3.1 Pre-Emphasis Optimization

The goal of pre-emphasis is to open the eye at the downstream receiver as much as possible. This means minimizing ISI jitter while meeting sufficient inner eye amplitude to meet a receiver's input sensitivity. The cable driver has the additional requirement to meet the SMPTE output specification.

The GS12081 has a high level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. The default cable driver settings should meet SMPTE output specification for most applications with short (1 to 2 inch) trace between the GS12081 and the output BNC. However, the pre-emphasis values may be adjusted to produce a better-looking eye. It is difficult to provide guidance regarding dB, as a 12G eye diagram looks different depending on the video test equipment used. The designer must optimize for their targets.

Table 4-2: Output Swing and Pre-Emphasis Control Parameters

Register Name and Address$_h$	Parameter Name	Description
0x2B/0x29, OUTPUT_ PARAM_CD_ SD_3/ OUTPUT_ PARAM_CD_ SD_1	CFG_OUTPUT<n>_CD_ SD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For SD and MADI rates on SDO0. <n> = 1: For SD and MADI rates on SDO1.
0x2D/0x2F OUTPUT_ PARAM_ CD_HD_1/ OUTPUT_ PARAM_ CD_HD_3	CFG_OUTPUT<n>_CD_ HD_DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x2C/0x2E OUTPUT_ PARAM_ CD_HD_0/ OUTPUT_ PARAM_ CD_HD_2	CFG_OUTPUT<n>_CD_HD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
	CFG_OUTPUT<n>_CD_HD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For HD and 3G rates on SDO0. <n> = 1: For HD and 3G rates on SDO1.
0x31/0x33 OUTPUT_ PARAM_ CD_UHD_1/ OUTPUT_ PARAM_ CD_UHD_3	CFG_OUTPUT<n>_CD_UHD_ DRIVER_SWING	Output amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
0x30/0x32 OUTPUT_ PARAM_ CD_UHD_0/ OUTPUT_ PARAM_ CD_UHD_2	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_PWRDWN	Output pre-emphasis power down configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n> = 0: For 6G and 12G rates on SDO0. <n> = 1: For 6G and 12G rates on SDO1.
4B CONTROL_ OUTPUT_ SLEW	CTRL_OUTPUT0_MANUAL_SLEW	Manually set the slew rate and output driver rate group to be used for SDO0/$\overline{\text{SDO0}}$ when CTRL_OUTPUT0_SLEW_SEL= 0.
	CTRL_OUTPUT1_MANUAL_SLEW	Manually set the slew rate and output driver rate group to be used for SDO1/$\overline{\text{SDO1}}$ when CTRL_OUTPUT1_SLEW_SEL = 0.

4.3.4 Output State Control Modes

The GS12081 provides several output state control modes to meet specific application requirements. The cable driver has the following three output modes: operational, muted, disabled, or balanced. During non-sleep, if the control modes are configured such that multiple output modes are enabled, the priorities of the control modes from highest to lowest are the following: balanced, disabled, and then muted.Section 4.3.4.1 through Section 4.3.4.3 describe how to configure the output control modes that are enabled during non-sleep. If the device enters sleep, either manually or automatically, the sleep output control modes take precedence over the non-sleep control modes. The default cable driver configuration is for it to be disabled during sleep; however the cable driver can be configured to mute during sleep by setting the **CFG_SLEEP_OUTPUT<n>_MUTE** parameter in register 0x5 to 1_b.

4.3.4.1 Output Mute Control Mode

Each of the outputs on the GS12081 have independent mute control modes, which can be configured through the host interface.

The following are the three output mute control modes:

1. The outputs automatically mute on LOS (default).
2. The outputs never mute.
3. The outputs are always muted.

The first mute control mode listed above is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_MUTE** control parameter in register 0x49 is set to 1_b). In this mode, the outputs will automatically mute on the assertion of LOS.

The outputs can be manually configured to never mute by setting both the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters in register 0x49 to 0_b. Alternatively, the outputs can be manually configured to always be muted by setting the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_ MANUAL_MUTE** control parameters to 0_b and 1_b respectively.

4.3.4.2 Output Disable Control Mode

Each of the outputs on the GS12081 also have independent disable control modes, which can be configured through the host interface.

The following are the three output disable control modes:

1. The outputs are never disabled (default).
2. The outputs are automatically disabled on LOS.
3. The outputs are always disabled.

The first disable control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_DISABLE** and **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameters in register 0x49 are both set to 0_b). In this mode, the outputs will never disable. By setting the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter in register 0x49 to 1_b, the outputs will automatically disable on the assertion of LOS.

The output can be manually disabled by leaving the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter set to 0_b and setting the **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameter to 1_b.

The disable control mode takes precedence over the output mute control mode.

4.3.4.3 Output Balanced Control Mode

The GS12081 has a feature designed to facilitate reliable Output Return Loss (ORL) measurement while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while ORL is being measured. BALANCE mode can be enabled through the host interface, by setting control parameter **CTRL_OUTPUT<n>_ BALANCED** in register 4D to 1_b. This control mode takes precedence over both the output mute and output disable control modes.

4.3.5 Output Waveform Specifications

The Duty Cycle Distortion (DCD) of the serial digital differential outputs is less than 12ps. DCD is defined as the difference in the width of an output logic "1" versus that of output logic "0" as measured at the 50% point of the output waveform.

The DCD of the serial digital single ended outputs is less than 30ps.

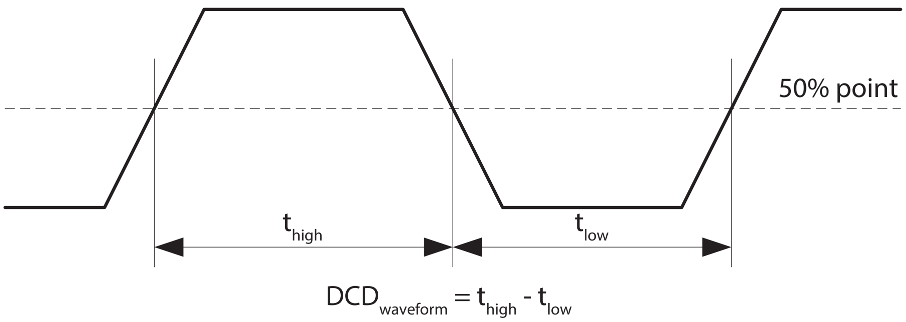


Figure 4-3: Traditional Waveform Definition of DCD

4.4 GPIO Controls

There are four configurable *GPIO* pins which can independently be configured as inputs or outputs. Each GPIO has a default function which can be re-configured through the host interface.

If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a *GPIO* pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. The logic HIGH and LOW levels of the *GPIO[3:0]* pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For a list of available functions and configuration details of *GPIO[3:0]*, please refer to the GPIO Configuration registers in Section 5.

4.5 GSPI Host Interface

The GS12081 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*SDIN* pin), serial data output signal (*SDOUT* pin), an active-LOW chip select ($\overline{CS}$ pin) and a burst clock (*SCLK* pin).

The GS12081 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.5.1 $\overline{\text{CS}}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-LOW signal provided by the host processor to the GS12081.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS12081.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS12081.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.5.2 SDIN Pin

The *SDIN* pin is the GSPI serial data input pin of the GS12081.

The 32-bit Command and 16-bit Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{\text{CS}}$ pin is LOW.

4.5.3 SDOUT Pin

The *SDOUT* pin is the GSPI serial data output of the GS12081.

All data transfers out of the GS12081 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the *SDOUT* pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{\text{CS}}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *SDOUT* pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{\text{CS}}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.5.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the **GSPI_LINK_DISABLE** bit in **CONTROL_REG**. When disabled, any data appearing at the *SDIN* pin will not appear at the *SDOUT* pin and the *SDOUT* pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd\_GSPI\_config}$ (4 SCLK cycles).

Table 4-3: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

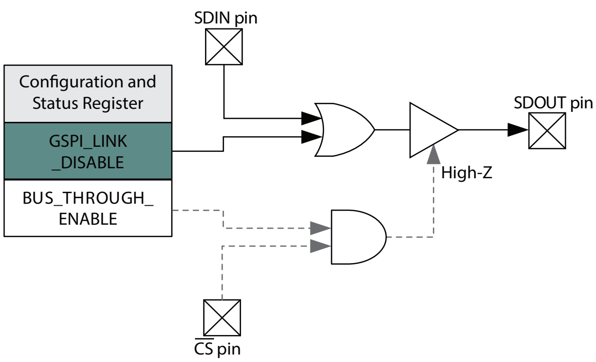


Figure 4-4: GSPI_LINK_DISABLE Operation

4.5.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS12081 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting **GSPI_BUS_THROUGH_ENABLE** bit to 1, the *SDOUT* pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the *SDOUT* pin will be driven and will follow regular read and write operation as described in Section 4.5.3.

Multiple chains of GS12081 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

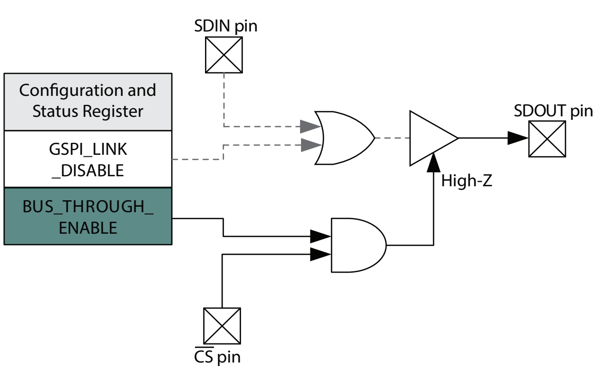


Figure 4-5: GSPI_BUS_THROUGH_ENABLE Operation

4.5.4 SCLK Pin

The *SCLK* pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS12081 *SDIN* pin on the rising edge of SCLK. Serial data is clocked out of the device from the *SDOUT* pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{\text{CS}}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.5.5 Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select ($\overline{CS}$) pin of the GS12081.

The format of the Command Words and Data Word are shown in Figure 4-6.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.5.5.1 R/$\overline{\text{W}}$ bit—B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{\text{W}}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{\text{W}}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.5.5.2 B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B’CAST ALL is set to 1, the following Data Word (**AUTOINC** = 0) or Data Words (**AUTOINC** = 1) are written to the register specified by the ADDRESS field of the Command Words (and subsequent addresses when **AUTOINC** = 1), regardless of the setting of the UNIT ADDRESS(es).

When B’CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

4.5.5.3 EMEM—B13 Command Word 1

The EMEM bit must be set to 1 in Command Word 1. When EMEM is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

4.5.5.4 AUTOINC—B12 Command Word 1

When **AUTOINC** is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When **AUTOINC** is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in **CONTROL_REG**.

4.5.5.5 UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed **DEV_UNIT_ADDRESS** in **CONTROL_REG**.

By default at power-up or after a device reset, the **DEV_UNIT_ADDRESS** is set to 00_h.

4.5.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 4-6 and Figure 4-7 below.

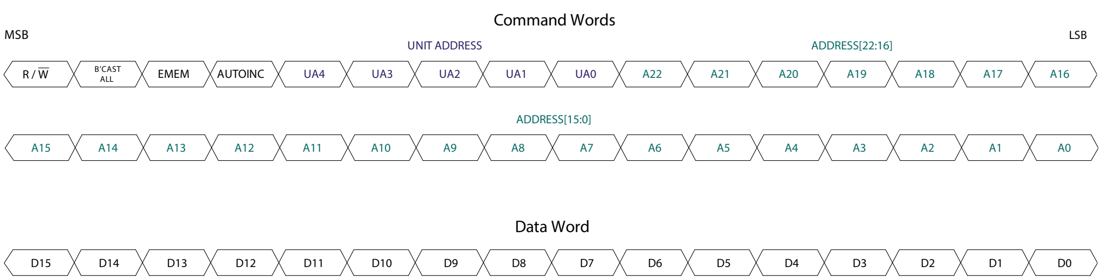


Figure 4-6: Command and Data Word Format

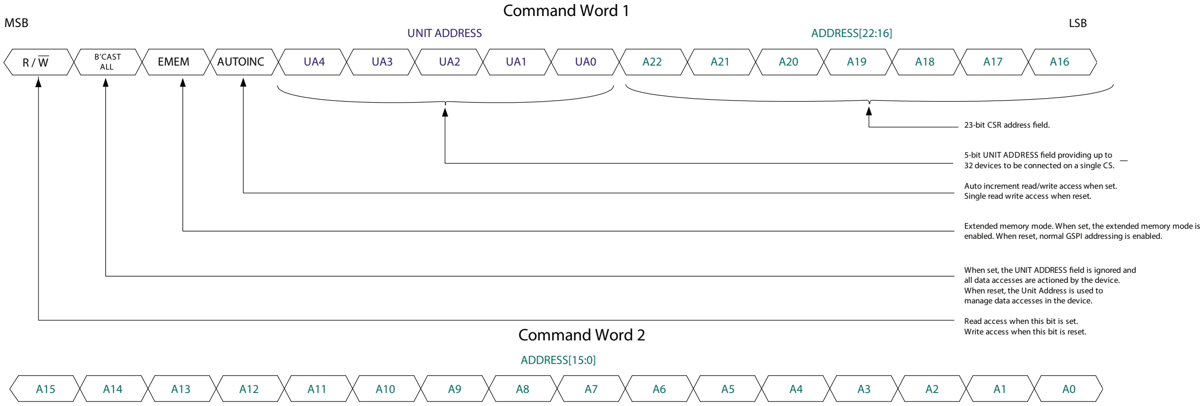


Figure 4-7: Command Word 1 and Command Word 2 Details

4.5.6 GSPI Transaction Timing

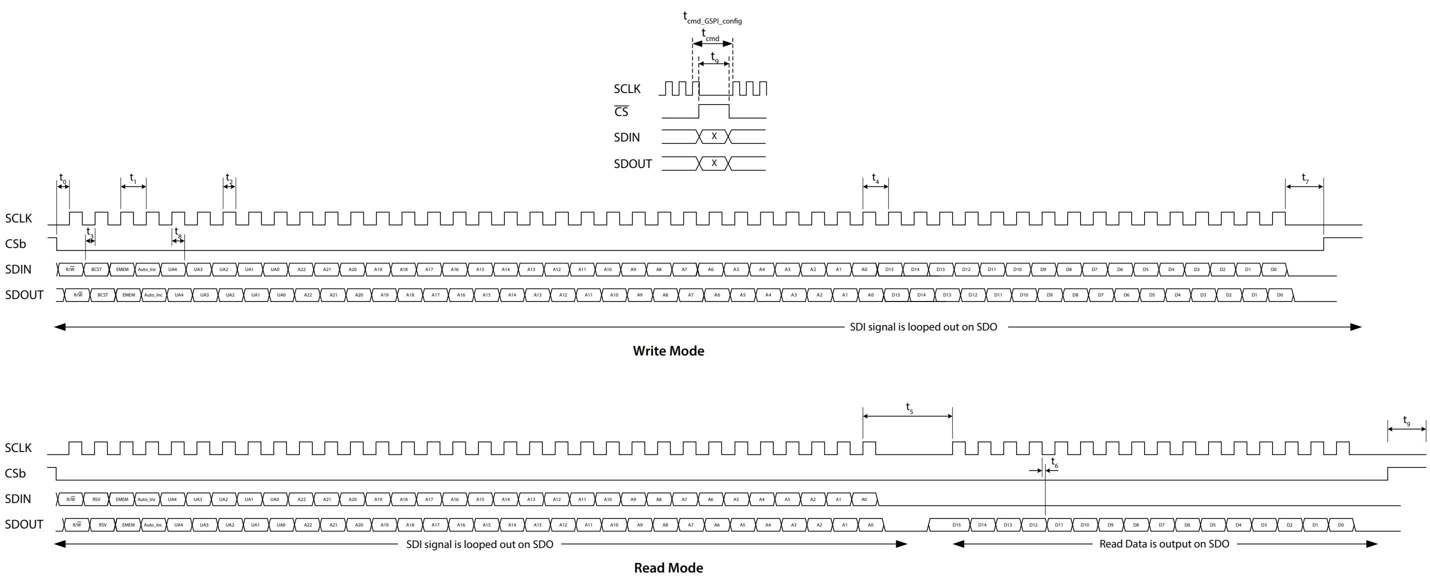


Figure 4-8: GSPI External Interface Timing

Table 4-4: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK Frequency	—	—	—	—	27	MHz
$\overline{CS}$ LOW Before SCLK Rising Edge	t_0	—	1.7	—	—	ns
SCLK Period	t_1	—	37	—	—	ns
SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2.3	—	—	ns
SCLK Idle Time – Write	t_4	1	1/SCLK	—	—	ns
SCLK Idle Time – Read	t_5	—	138	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	115	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd\_GSPI\_conf}$[1]	4	139	—	—	ns
SDOUT After SCLK Falling Edge	t_6	—	1.3	—	6.4	ns
CS HIGH After Final SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1.2	—	—	ns
$\overline{CS}$ HIGH Time	t_9	—	58	—	—	ns
SDIN to SDOUT Combinatorial Delay	—	—	—	—	3.4	ns
Max chips daisy-chained at max SCLK frequency (26 MHz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	8	# of compatible Semtech devices
Max frequency for 32 daisy-chained devices	When host clocks in SDOUT data on falling edge of SCLK		—	—	7.5	MHz

Note:

1. $t_{cmd\_GSPI\_conf}$ inter-command delay must be used whenever modifying **CONTROL_REG** register at address 0x00.

4.5.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-9 to Figure 4-13.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a HIGH-to-LOW transition of the $\overline{CS}$ pin. The read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in **CONTROL_REG**, the inter-command delay time, $t_{cmd\_GSPI\_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 27MHz.

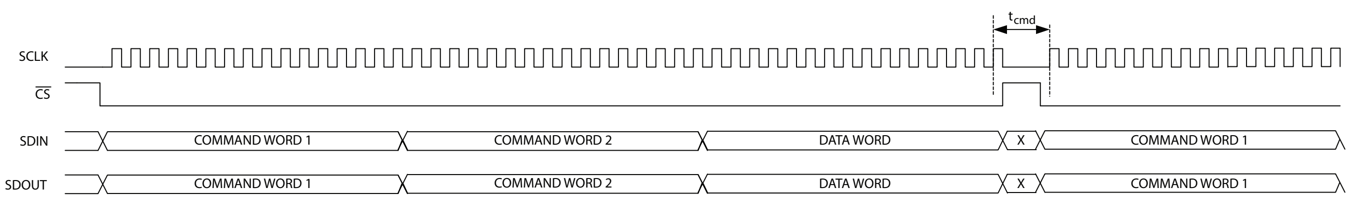


Figure 4-9: GSPI Write Timing—Single Write Access with Loop-Through Operation (default)

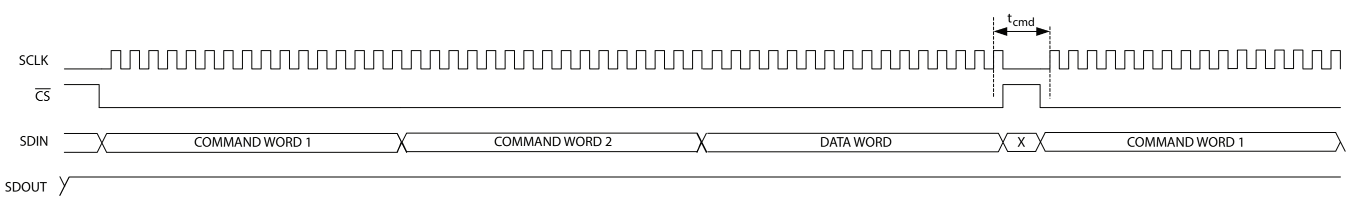


Figure 4-10: GSPI Write Timing—Single Write Access with GSPI Link-Disable Operation

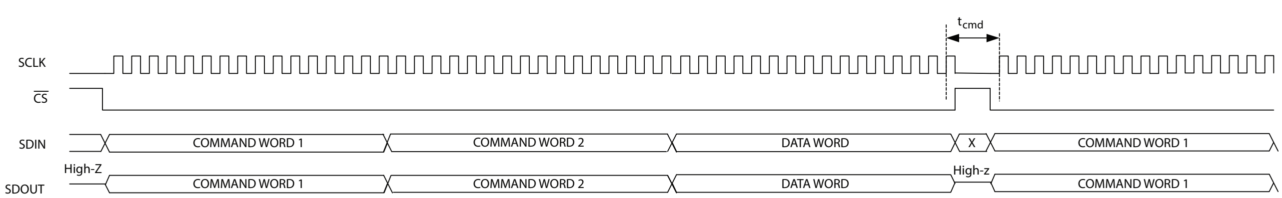


Figure 4-11: GSPI Write Timing—Single Write Access with Bus-Through Operation

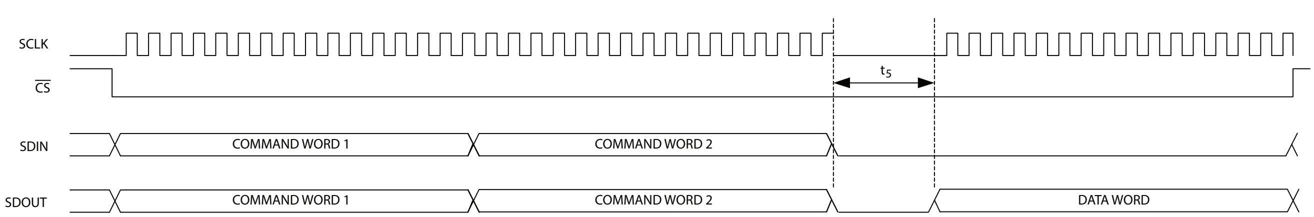


Figure 4-12: GSPI Read Timing—Single Read Access with Loop-Through Operation (default)

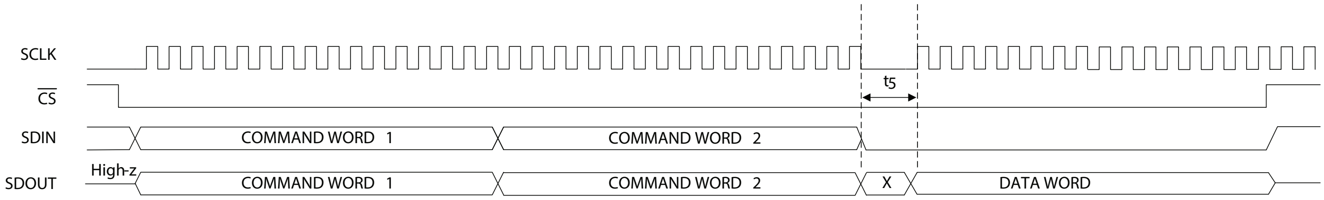


Figure 4-13: GSPI Read Timing—Single Read Access with Bus-Through Operation

4.5.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-14 to Figure 4-18.

Auto-increment mode is enabled by the setting the **AUTOINC** bit of Command Word 1.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of two Command Words and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

Note: Writing to **CONTROL_REG** using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the second Command Word to the start of the data output of the first Data Word as defined by t_5 will be no less than 4 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

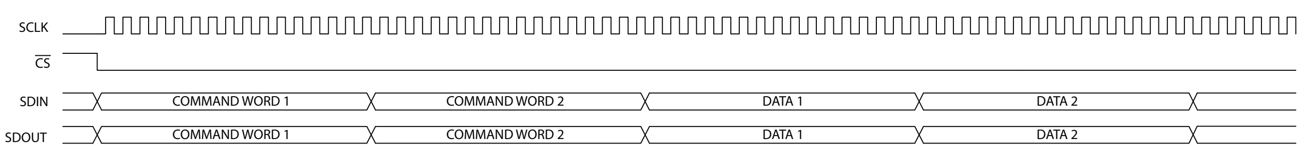


Figure 4-14: GSPI Write Timing—Auto-Increment with Loop-Through Operation (default)

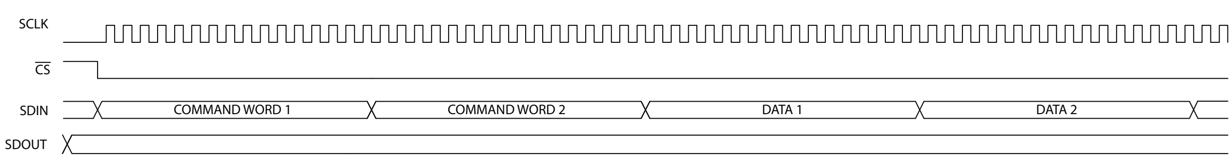


Figure 4-15: GSPI Write Timing—Auto-Increment with GSPI Link Disable Operation

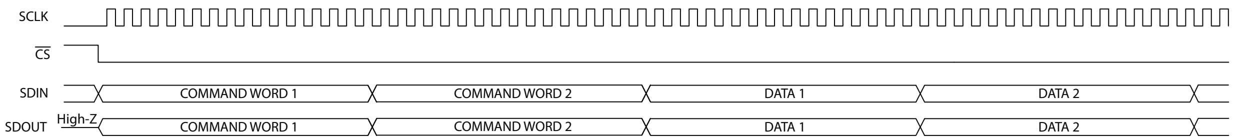


Figure 4-16: GSPI Write Timing—Auto-Increment with Bus-Through Operation

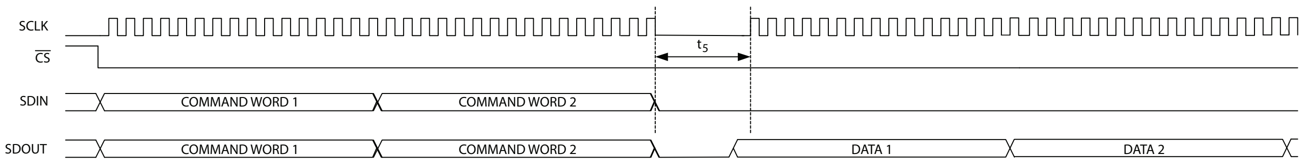


Figure 4-17: GSPI Read Timing—Auto-Increment Read with Loop-Through Operation (default)

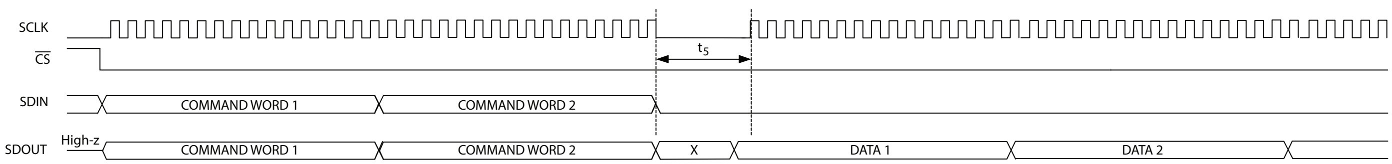


Figure 4-18: GSPI Read Timing—Auto-Increment Read with Bus-through Operation

4.5.9 Setting a Device Unit Address

Multiple (up to 32) GS12081 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the **DEV_UNIT_ADDRESS** of each device is set to 0_h and the SDIN→SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEV_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEV_UNIT_ADDRESS** field set to 0. This disables the direct SDIN→SDOUT non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting **CONTROL_REG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEV_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEV_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEV_UNIT_ADDRESS** value 0.
3. Repeat step 2 using new, unique values for the **DEV_UNIT_ADDRESS** field in **CONTROL_REG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd\_GSPI\_conf}$ delay must be observed after every write that modifies **CONTROL_REG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEV_UNIT_ADDRESS** in **CONTROL_REG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.5.10 Default GSPI Operation

By default at power up or after a device reset, the GS12081 is set for Loop-Through Operation and the internal **DEV_UNIT_ADDRESS** field of the device is set to 0.

Figure 4-19 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS12081.

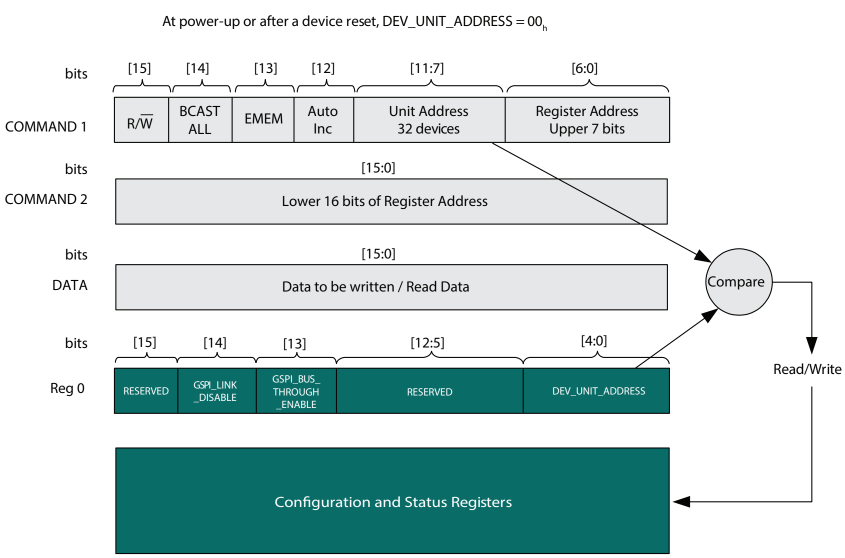


Figure 4-19: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access (R/$\overline{W}$ = 0); set Auto Increment; set the Unit Address field in the Command Word 1 to match the configured **DEV_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEV_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEV_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

4.5.11 Clear Sticky Counts Through Four Way Handshake

There are four sticky counters that keep count of changes in status of primary and secondary carriers. The counters can be read from the following two parameters in register 0x84 and 0x85: **STAT_CNT_PRI_CD_CHANGES,** and **STAT_CNT_SEC_CD_CHANGES**. The counters saturate at 255 (0xFF) and must be cleared before additional status changes can be counted. The following four way handshake procedures clears the counters.

1. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 0 (idle), then set **CTRL_CLEAR_COUNTS** = 1 (clear sticky counts).
2. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 2 (cleared), then reset **CTRL_CLEAR_COUNTS** to 0.

The device will now reset **STAT_CLEAR_COUNTS_STATUS** to 0 (idle) and the clearing process can be repeated at any time.

4.5.12 Device Power Up Sequence

The device does not require a specific power supply initialization sequence, and all chip supplies can be powered up simultaneously.

If all power supplies cannot be guaranteed to power up simultaneously, ensure that *VCC_DDI* powers up first. Note that there is no minimum time requirement between power supply initializations after *VCC_DDI* is energized.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.5.12.1 Power-Up Timing Sequence

The following timing sequence must be observed after power-up when no external configuration loading is required. See Figure 4-20 for the timing requirements of Steps 1 and 2 below.

Step 1 – No GSPI Access Allowed

a) Device supply reaches 90% of target. POR (Power On Reset) is activated.

b) Internal blocks reset, default device configuration boot-up begins.

c) Default device configuration boot-up process.

Step 2 – GSPI Access Allowed

a) If there are multiple devices on the GSPI chain, the host should configure the unit address of each device. See Section 4.5.9 for further information on unit addressing.

b) Host sets custom application specific settings.

c) Normal operation begins.

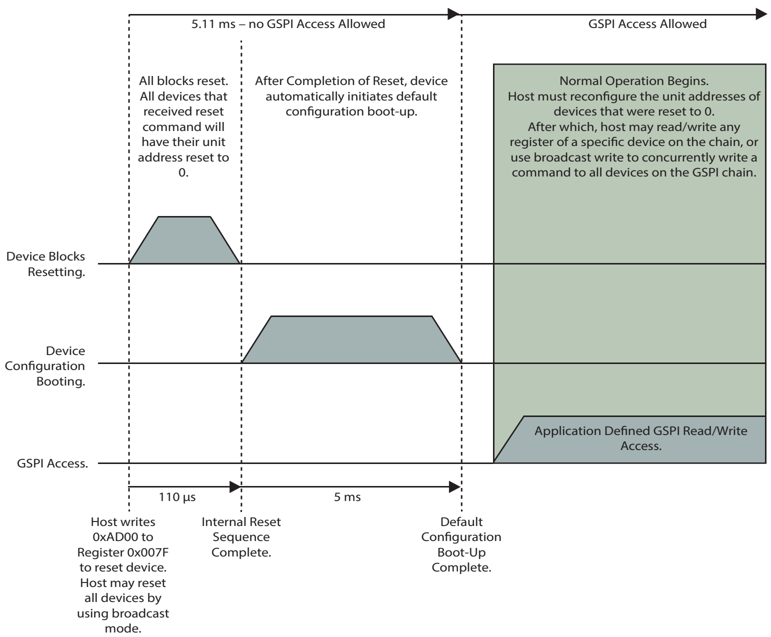


Figure 4-20: Power-Up Sequence.

4.5.13 Host Initiated Device Reset

The GS12081 includes a reset function accessible via the device's host interface, which reverts all internal logic and register values to their default values.

The device can be reset with a single write of $AD00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register, which will assert and de-assert the device reset within the duration of the GSPI write access Data Word.

The device can be placed and held in reset by writing $AA00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register. Subsequent writes of $DD00_h$ to the **RESET_CONTROL** bits will de-assert device reset.

The current state of user-initiated device reset can be read from the **RESET_CONTROL** bits of **CONTROL_RESET** register.

While in reset, host interface access to any other register will not be functional and all logic and configuration registers will be in reset state. While in reset, serial digital differential output behaviour is undefined. The digital logic and registers within the device will exit the reset state 5ms after device reset is de-asserted.

The following timing sequence must be observed to initiate a device reset.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.5.13.1 Host Initiated Device Reset Timing Sequence

The following timing sequence must be observed after a Host Initiated Device Reset when no external configuration loading is required. See Figure 4-21 for the timing requirements of the Steps 1 to 3 below.

Step 1 – GSPI Access Allowed

a) Host writes 0xAD00 to register 0x007F to reset selected devices, or all devices using broadcast.

Step 2– No GSPI Access Allowed

a) Internal blocks reset, default device configuration boot-up begins.

b) Default device configuration boot-up completes.

Step 3 – GSPI Access Allowed

a) If there are multiple devices on the GSPI chain, host must reconfigure unit address of each device that was reset. See Section 4.5.9 for further information on unit addressing.

b) Host sets custom application specific settings.

c) Normal operation begins.

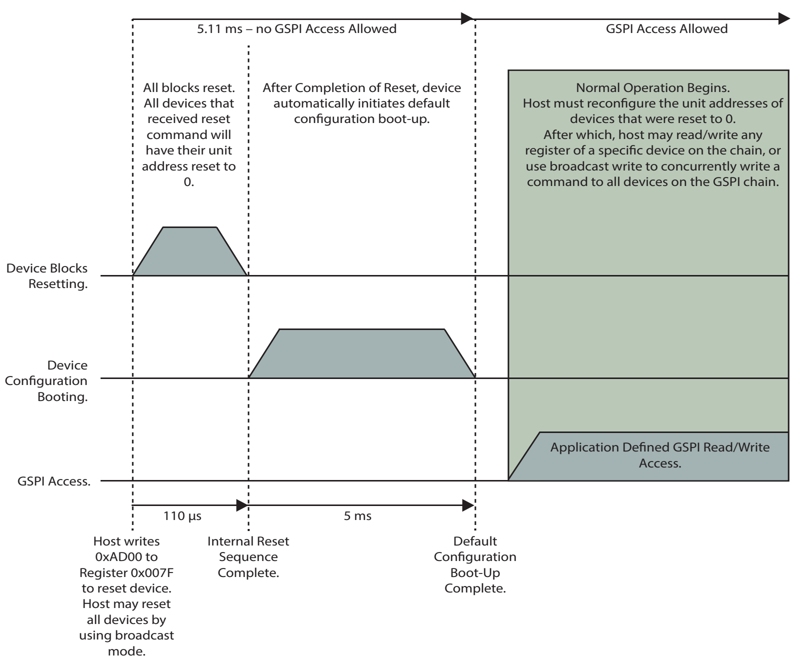


Figure 4-21: Host Initiated Device Reset Timing Sequence.

5. Register Map

The host interface on the GS12081 provides users complete control of key features such as GPIO configuration, carrier detection, trace equalization, bypass modes, output swing controls, mute functions, pre-emphasis control and many others.

It also includes a wide selection of Status registers which allow the user to read back several key metrics of information from the GS12081 to add more flexibility to their designs. Section 5.1 to Section 5.3 cover each Control and Status register in detail.

5.1 Control Registers

Table 5-1: Control Registers

GSPI $Address_h$	Register Name	R/W
0	CONTROL_ REG	RW
1	DEVICE_ID	RO
2	RSVD	RW
7F	CONTROL_ RESET	RW
3	CONTROL_ SLEEP	RW
4	MISC_CNTRL	RW
5	MISC_CFG	RW
6 to 9	RSVD	RW
0A to 0F	RSVD	RW
GPIO Configuration		
10	GPIO0_CFG	RW
11	GPIO1_CFG	RW
12	GPIO2_CFG	RW
13	GPIO3_CFG	RW
Equalizer Configuration		
14 to 1A	RSVD	RW
1B	OFFSET_ CORRECTION_ MODE	RW
1C to 1D	RSVD	RW
1E	TREQ0_ INPUT_BOOST	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
1F	TREQ0_CD_ HYSTERESIS	RW
20 to 25	RSVD	RW
Output Configuration		
26 to 27	RSVD	RW
28	OUTPUT_ PARAM_CD_ SD_0	RW
29	OUTPUT_ PARAM_CD_ SD_1	RW
2A	OUTPUT_ PARAM_CD_ SD_2	RW
2B	OUTPUT_ PARAM_CD_ SD_3	RW
2C	OUTPUT_ PARAM_ CD_HD_0	RW
2D	OUTPUT_ PARAM_ CD_HD_1	RW
2E	OUTPUT_ PARAM_ CD_HD_2	RW
2F	OUTPUT_ PARAM_ CD_HD_3	RW
30	OUTPUT_ PARAM_ CD_UHD_0	RW
31	OUTPUT_ PARAM_ CD_UHD_1	RW
32	OUTPUT_ PARAM_ CD_UHD_2	RW
33	OUTPUT_ PARAM_ CD_UHD_3	RW
34 to 47	RSVD	RW
Output Control		
48	OUTPUT_ SIG_SELECT	RW
49	CONTROL_ OUTPUT_ MUTE	RW
4A	CONTROL_ OUTPUT_ DISABLE	RW
4B	CONTROL_ OUTPUT_ SLEW	RW
4C	RSVD	RW
4D	CONTROL_ BALANCED_ MODE	RW
4E to 4F	RSVD	RW
50 to 59	RSVD	RW
5A to 5D	RSVD	RW
Internal Only Configuration		
5E to 7E	RSVD	RW

5.2 Status Registers

Table 5-2: Status Registers

GSPI $Address_h$	Register Name	R/W
80	RSVD	RW
81	VERSION_0	RW
82	VERSION_1	RW
83	VERSION_2	RW
84	STICKY_ COUNTS_0	RW
85	RSVD	RW
86	CURRENT_ STATUS_0	RW
87	CURRENT_ STATUS_1	RW
88 to BF	RSVD	RW

5.3 Register Descriptions

Table 5-3: Control Register Descriptions

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
Device Configuration And Control						
0	CONTROL_ REG	RSVD	15	R/W	0	Reserved do not modify.
		GSPI_LINK_DISABLE	14	R/W	0	0 = Enable loop-through. SDIN pin is looped through to the SDOUT pin. 1 = Disable loop-through. Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.
		GSPI_BUS_THROUGH_ ENABLE	13	R/W	0	0 = Disable bus-through mode 1 = Enable bus-through mode
		DEV_UNIT_ADDRESS	4:0	R/W	0	Device address programmed by application. See Section 4.5.9 for further information
1	DEVICE_ID	DEVICE_VERSION	15:0	RO	—	This register contains the device's identification, including revision. Contact the local technical sales representative for more details.
2	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
7F	CONTROL_RESET	RESET_CONTROL	15:0	R/W	DD00	Device Reset, Reverts all internal logic and register values to defaults. Write Values: $AA00_h$ = Asserts device reset $DD00_h$ = De-assert device reset $AD00_h$ = Assert/de-assert device reset in a single write Read Values: $AA00_h$ = User-initiated reset is asserted $DD00_h$ = User-initiated reset is de-asserted See Section 4.5.13 for further information
3	CONTROL_SLEEP	RSVD	15:2	R/W	0	Reserved - do not modify.
		CTRL_MANUAL_SLEEP	1	R/W	0	Sleep manual mode control: 0 = Never Sleep 1 = Always Sleep Controls sleep mode when auto sleep (CTRL_AUTO_SLEEP) is disabled.
		CTRL_AUTO_SLEEP	0	R/W	1	Sleep auto mode control: 0 = Disable auto sleep mode 1 = Enable auto sleep mode If CTRL_AUTO_SLEEP = 0 (manual sleep mode), then CTRL_MANUAL_SLEEP controls sleep. If CTRL_AUTO_SLEEP = 1 (auto sleep mode), sleep is automatically entered on loss of signal.
4	MISC_CNTRL	RSVD	15:1	R/W	0	Reserved - do not modify.
		CTRL_CLEAR_COUNTS	0	R/W	0	Clear sticky counts control register. 0 = no action 1 = clear sticky counts. Part of a four way handshake with STAT_CLEAR_COUNTS_STATUS. See Section 4.5.11 for more details on implementing the four way handshake for this operation.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
5	MISC_CFG	RSVD	15:4	R/W	0	Reserved - do not modify.
		CFG_SLEEP_ OUTPUT1_MUTE	3	R/W	0	Controls whether cable driver (SDO1) is muted or disabled (powered down) during sleep: 0 = disable (power down) output during sleep. 1 = mute output during sleep.
		CFG_SLEEP_ OUTPUT0_MUTE	2	R/W	0	Controls whether cable driver (SDO0) is muted or disabled (powered down) during sleep: 0 = disable (power down) output during sleep. 1 = mute output during sleep.
		RSVD	1:0	R/W	0	Reserved - do not modify.
6	RSVD	RSVD	15:0	R/W	FE01	Reserved - do not modify.
7	RSVD	RSVD	15:0	R/W	3	Reserved - do not modify.
8	RSVD	RSVD	15:0	R/W	3	Reserved - do not modify.
9	RSVD	RSVD	15:0	R/W	70	Reserved - do not modify.
0A	RSVD	RSVD	15:0	R/W	808	Reserved - do not modify.
0B	RSVD	RSVD	15:0	R/W	808	Reserved - do not modify.
0C	RSVD	RSVD	15:0	R/W	1C08	Reserved - do not modify.
0D	RSVD	RSVD	15:0	R/W	8	Reserved - do not modify.
0E to 0F	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
		GPIO Configuration				
10	GPIO0_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO0_ OUTPUT_ENA	8	R/W	1	GPIO0 buffer mode control. 0 = GPIO pin is configured as an input (tri-stated / high impedance). 1 = GPIO pin is configured as an output.
		CFG_GPIO0_FUNCTION	7:0	R/W	80	Function select for GPIO0 pin. GPIO0 output functions: 0x00 = Output driven LOW 0x01 = Output driven HIGH 0x02 = Reserved - do not modify. 0x03 to 0x7E = Reserved - do not use. 0x80 = LOS equivalent to inverse of STAT_PRI_CD (Default mode for GPIO0) 0x81 = carrier detect status (STAT_PRI_CD) 0x82 = Sleep mode status (HIGH — Device in sleep mode) 0x83 to 0xFF = Reserved - do not use. GPIO0 input functions: 0x00 to 0x7E = Reserved - do not use. 0x80 = Unused 0x81 = SDO0 disable control (HIGH — disable) 0x82 = SDO1 disable control (HIGH — disable) 0x83 = Reserved - do not modify. 0x84 = Unused 0x85 = Reserved - do not modify. 0x86 = Sleep control (HIGH — Sleep) 0x87 to 0xFF = Reserved - do not use.
11	GPIO1_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO1_ OUTPUT_ENA	8	R/W	1	GPIO1 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Output
		CFG_GPIO1_ FUNCTION	7:0	R/W	2	Function select for GPIO1 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: Unassigned. Configure to the most appropriate GPIO function for the intended application.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
12	GPIO2_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO2_ OUTPUT_ENA	8	R/W	0	GPIO2 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO2_FUNCTION	7:0	R/W	86	Function select for GPIO2 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x86 = Sleep control
13	GPIO3_CFG	RSVD	15:9	R/W	0	Reserved - do not modify.
		CFG_GPIO3_ OUTPUT_ENA	8	R/W	0	GPIO3 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO3_FUNCTION	7:0	R/W	87	Function select for GPIO3 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x82 = SDO1 disable control (HIGH disable)
Trace Equalizer Configuration						
14 to 1A	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
1B	OFFSET_ CORRECTION_ MODE	RSVD	15:2	R/W	0	Reserved - do not modify.
		CFG_OFFSET_ MANUAL_ENA	1	R/W	0	Enable offset correction: 0 = Offset correction disabled 1 = Offset correction enabled It is recommended to enable offset correction for rates HD through 12G to minimize output jitter.
		RSVD	0	R/W	0	Reserved - do not modify.
1C to 1D	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	$Reset Value_h$	Description
1E	TREQ0_ INPUT_BOOST	RSVD	15:5	R/W	0	Reserved - do not modify.
		CFG_TREQ0_BOOST	4:1	R/W	2	Trace equalizer boost setting for TEQ (Trace Equalizer): 0 = Bypass equalization stage 1 to 8 = 1 to 17dB of insertion loss at 5.94GHz (see Figure 4-1). Bypass is the minimum boost setting; boost 8 is maximum boost setting.
		CFG_TREQ0_ CD_BOOST	0	R/W	0	Selects boost level applied to DDI input signal for carrier detection function only. 0 = Sets to boost 8 (See Figure 4-1) 1 = Use CFG_TREQ0_BOOST setting
1F	TREQ0_CD_ HYSTERESIS	RSVD	15:8	R/W	0	Reserved - do not modify.
		CFG_TREQ0_CD_ ASSERT_THRESH	7:4	R/W	4	Sets assert threshold for trace equalizer carrier detect 0 to15_d, where 0 is minimum threshold and 15_d is maximum threshold (see Figure 4-2).
		CFG_TREQ0_CD_ DEASSERT_THRESH	3:0	R/W	3	Sets deassert threshold for trace equalizer carrier detect 0 to15_d, where 0 is minimum threshold and 15_d is maximum threshold (see Figure 4-2).
20 to 25	MISC_ OUTPUT_CFG	RSVD	15:0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
Output Configuration						
26 to 27	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
28	OUTPUT_PARAM_CD_SD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_SD_PREEMPH_WIDTH	12:8	R/W	3	Configure the MADI/SD rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_SD_PREEMPH_PWRDWN	6	R/W	1	Power down the MADI/SD rate pre-emphasis on cable driver output1 (SDO1). 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_SD_PREEMPH_AMPL	5:0	R/W	0	Configure the MADI/SD rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
29	OUTPUT_PARAM_CD_SD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_SD_DRIVER_SWING	13:8	R/W	17	Configure the MADI/SD rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	A0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
2A	OUTPUT_ PARAM_CD_ SD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ SD_PREEMPH_WIDTH	12:8	R/W	3	Configure the MADI/SD rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ SD_PREEMPH_ PWRDWN	6	R/W	1	Power down the MADI/SD rate pre-emphasis on cable driver output0 (SDO0). 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_ SD_PREEMPH_AMPL	5:0	R/W	0	Configure the MADI/SD rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2B	OUTPUT_ PARAM_CD_ SD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ SD_DRIVER_SWING	13:8	R/W	17	Configure the MADI/SD rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	A0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
2C	OUTPUT_ PARAM_ CD_HD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ HD_PREEMPH_WIDTH	12:8	R/W	8	Configure the HD/3G rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ HD_PREEMPH_ PWRDWN	6	R/W	0	Power down the HD/3G rate pre-emphasis on cable driver output1 (SDO1) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_ HD_PREEMPH_AMPL	5:0	R/W	5	Configure the HD/3G rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2D	OUTPUT_ PARAM_ CD_HD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ HD_DRIVER_SWING	13:8	R/W	19	Configure the HD/3G rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the cable driver amplitude. The default value produces an amplitude of $800mV_{pp}$.
		RSVD	7:0	R/W	80	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2E	OUTPUT_ PARAM_ CD_HD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ HD_PREEMPH_WIDTH	12:8	R/W	8	Configure the HD/3G rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15$_d$ Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W		Reserved - do not modify.
		CFG_OUTPUT0_CD_ HD_PREEMPH_ PWRDWN	6	R/W	0	Power down the HD/3G rate pre-emphasis on cable driver output0 (SDO0) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_ HD_PREEMPH_AMPL	5:0	R/W	5	Configure the HD/3G rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15$_d$. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.
2F	OUTPUT_ PARAM_ CD_HD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_ HD_DRIVER_SWING	13:8	R/W	19	Configure the HD/3G rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31$_d$. Adjust the cable driver amplitude. The default value produces an amplitude of 800mV$_{pp}$.
		RSVD	7:0	R/W	80	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	$Reset Value_h$	Description
30	OUTPUT_ PARAM_ CD_UHD_0	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_PREEMPH_ WIDTH	12:8	R/W	4	Configure the 6G/12G rate pre-emphasis pulse width on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape. **Note:** These settings are applied if CTRL_OUTPUT1_MANUAL_SLEW = 2.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_PREEMPH_ PWRDWN	6	R/W	0	Power down the 6G/12G rate pre-emphasis on cable driver output1 (SDO1) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled). **Note:** These settings are applied if CTRL_OUTPUT1_MANUAL_SLEW = 2.
		CFG_OUTPUT1_CD_ UHD_PREEMPH_AMPL	5:0	R/W	4	Configure the 6G/12G rate pre-emphasis amplitude on cable driver output1 (SDO1). Range: 0 to 15_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist. **Note:** These settings are applied if CTRL_OUTPUT1_MANUAL_SLEW = 2.
31	OUTPUT_ PARAM_ CD_UHD_1	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT1_CD_ UHD_DRIVER_ SWING	13:8	R/W	1B	Configure the 6G/12G rate amplitude on cable driver output1 (SDO1). amplitude. Range: 0 to 31_d. Adjust the differential cable driver amplitude. The default value produces an amplitude of 800mVpp. **Note:** These settings are applied if CTRL_OUTPUT1_MANUAL_SLEW = 2.
		RSVD	7:0	R/W	40	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
32	OUTPUT_PARAM_CD_UHD_2	RSVD	15:13	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_UHD_PREEMPH_WIDTH	12:8	R/W	4	Configure the 6G/12G rate pre-emphasis pulse width on cable driver output0 (SDO0). Range: 0 to 15$_d$. Adjust the pre-emphasis pulse width to better match the channel loss response shape. **Note:** These settings are applied if CTRL_OUTPUT0_MANUAL_SLEW = 2.
		RSVD	7	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_UHD_PREEMPH_PWRDWN	6	R/W	0	Power down the 6G/12G rate pre-emphasis on cable driver output0 (SDO0) 0 = Pre-emphasis driver powered up (pre-emphasis enabled). 1 = Pre-emphasis driver powered down (pre-emphasis disabled). **Note:** These settings are applied if CTRL_OUTPUT0_MANUAL_SLEW = 2.
		CFG_OUTPUT0_CD_UHD_PREEMPH_AMPL	5:0	R/W	4	Configure the 6G/12G rate pre-emphasis amplitude on cable driver output0 (SDO0). Range: 0 to 15$_d$. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist. **Note:** These settings are applied if CTRL_OUTPUT0_MANUAL_SLEW = 2.
33	OUTPUT_PARAM_CD_UHD_3	RSVD	15:14	R/W	0	Reserved - do not modify.
		CFG_OUTPUT0_CD_UHD_DRIVER_SWING	13:8	R/W	1B	Configure the 6G/12G rate amplitude on cable driver output0 (SDO0). amplitude. Range: 0 to 31$_d$. Adjust the cable driver amplitude. The default value produces an amplitude of 800mV$_{pp}$. **Note:** These settings are applied if CTRL_OUTPUT0_MANUAL_SLEW = 2.
		RSVD	7:0	R/W	40	Reserved - do not modify.
34 to 3B	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
3C	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
3D	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
3E	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
3F	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
40	RSVD	RSVD	15:0	R/W	340	Reserved - do not modify.
41	RSVD	RSVD	15:0	R/W	850	Reserved - do not modify.
42	RSVD	RSVD	15:0	R/W	340	Reserved - do not modify.
43	RSVD	RSVD	15:0	R/W	850	Reserved - do not modify.
44	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
45	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
46	RSVD	RSVD	15:0	R/W	342	Reserved - do not modify.
47	RSVD	RSVD	15:0	R/W	1C90	Reserved - do not modify.
Output Control						
48	OUTPUT_ SIG_SELECT	RSVD	15:4	R/W	10	Reserved - do not modify.
		CTRL_OUTPUT0_ DATA_INVERT	3	R/W	0	Controls optional signal polarity inversion on cable driver output0 (SDO0) when data is selected (CTRL_OUTPUT0_SIGNAL_SEL = 0).
		CTRL_OUTPUT1_ DATA_INVERT	2	R/W	0	Controls optional signal polarity inversion on cable driver output1 (SDO1) when data is selected (CTRL_OUTPUT1_SIGNAL_SEL = 0).
		RSVD	1	R/W	0	Reserved - do not modify.
		RSVD	0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
49	CONTROL_ OUTPUT_ MUTE	RSVD	15:6	R/W	0	Reserved - do not modify.
		RSVD	5	R/W	0	Reserved - do not modify.
		RSVD	4	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ MANUAL_MUTE	3	R/W	0	Controls mute for cable driver output1 (SDO1) when auto mute (CTRL_OUTPUT1_AUTO_MUTE = 0) is disabled. 0 = Unmute output driver 1 = Mute output driver.
		CTRL_OUTPUT1_ AUTO_MUTE	2	R/W	1	Select automatic or manual mute control for cable driver output1 (SDO1) 0 = Disable auto mute mode 1 = Enable auto mute mode If CTRL_OUTPUT1_AUTO_MUTE = 0, then CTRL_OUTPUT1_MANUAL_MUTE controls mute for SDO1.
		CTRL_OUTPUT0_ MANUAL_MUTE	1	R/W	0	Controls mute for cable driver output0 (SDO0) when auto mute (CTRL_OUTPUT0_AUTO_MUTE = 0) is disabled. 0 = Unmute output driver 1 = Mute output driver.
		CTRL_OUTPUT0_ AUTO_MUTE	0	R/W	1	Select automatic or manual mute control for cable driver output0 (SDO0) 0 = Disable auto mute mode 1 = Enable auto mute mode If CTRL_OUTPUT0_AUTO_MUTE = 0, then CTRL_OUTPUT0_MANUAL_MUTE controls mute for SDO0.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4A	CONTROL_ OUTPUT_ DISABLE	RSVD	15:4	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ MANUAL_DISABLE	3	R/W	0	Controls disable for cable driver output1 (SDO1) when auto disable (CTRL_OUTPUT1_AUTO_DISABLE = 0) is disabled. 0 = Enable output driver 1 = Disable (power down) output driver.
		CTRL_OUTPUT1_ AUTO_DISABLE	2	R/W	0	Select automatic or manual disable control for cable driver output1 (SDO1) 0 = Disable auto disable mode 1 = Enable auto disable mode If CTRL_OUTPUT1_AUTO_DISABLE = 0, then CTRL_OUTPUT1_MANUAL_DISABLE controls mute for SDO1.
		CTRL_OUTPUT0_ MANUAL_DISABLE	1	R/W	0	Controls disable for cable driver output0 (SDO0) when auto disable (CTRL_OUTPUT0_AUTO_DISABLE = 0) is disabled. 0 = Enable output driver 1 = Disable (power down) output driver.
		CTRL_OUTPUT0_ AUTO_DISABLE	0	R/W	0	Select automatic or manual disable control for cable driver output0 (SDO0) 0 = Disable auto disable mode 1 = Enable auto disable mode If CTRL_OUTPUT0_AUTO_DISABLE = 0, then CTRL_OUTPUT0_MANUAL_DISABLE controls mute for SDO0.
4B	CONTROL_ OUTPUT_ SLEW	RSVD	15:11	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_ MANUAL_SLEW	10:9	R/W	2	Manually set the slew rate and output driver rate group to be used for SDO1/$\overline{\text{SDO1}}$ when CTRL_OUTPUT1_SLEW_SEL = 0. 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		RSVD	8:3	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT0_ MANUAL_SLEW	2:1	R/W	2	Manually set the slew rate and output driver rate group to be used for SDO0/$\overline{\text{SDO0}}$ when CTRL_OUTPUT0_SLEW_SEL = 0. 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		RSVD	0	R/W	0	Reserved - do not modify.

Table 5-3: Control Register Descriptions (Continued)

$Address_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset $Value_h$	Description
4C	RSVD	RSVD	15:0	R/W	5	Reserved - do not modify.
4D	CONTROL_BALANCED_MODE	RSVD	15:2	R/W	0	Reserved - do not modify.
		CTRL_OUTPUT1_BALANCED	1	R/W	0	Enable or Disable balanced mode on cable driver output1 (SDO1) for powered ORL measurement. 0 = Disable 1 = Enable
		CTRL_OUTPUT0_BALANCED	0	R/W	0	Enable or Disable balanced mode on cable driver output (SDO0) for powered ORL measurement. 0 = Disable 1 = Enable
4E to 4F	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
50	RSVD	RSVD	15:0	R/W	3	Reserved - do not modify.
51	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
52	RSVD	RSVD	15:0	R/W	106	Reserved - do not modify.
53	RSVD	RSVD	15:0	—	—	Reserved - do not modify.
54	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
55	RSVD	RSVD	15:0	R/W	64	Reserved - do not modify.
56	RSVD	RSVD	15:0	R/W	64	Reserved - do not modify.
57	RSVD	RSVD	15:0	R/W	8000	Reserved - do not modify.
58	RSVD	RSVD	15:0	R/W	D280	Reserved - do not modify.
59	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
5A	RSVD	RSVD	15:0	R/W	7F	Reserved - do not modify.
5B	RSVD	RSVD	15:0	R/W	100	Reserved - do not modify.
5C	RSVD	RSVD	15:0	R/W	FF01	Reserved - do not modify.
5D	RSVD	RSVD	15:0	R/W	0	Reserved - do not modify.
5E to 5F	RSVD	RSVD	15:0	R/W	—	Reserved - do not modify.
Factory Settings						
60 to 7E	RSVD	RSVD	15:0	RO	—	Reserved.

Table 5-4: Status Register Descriptions

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
80	RSVD	RSVD	15:0	RO	—	Reserved.
81	VERSION_0	STAT_CONFIG_VER0	15:0	RO	—	This register contains the first part of the device configuration version. Please contact your local technical sales representative for more details.
82	VERSION_1	STAT_CONFIG_VER1	15:0	RO	—	This register contains the second part of the device configuration version. Please contact your local technical sales representative for more details.
83	VERSION_2	STAT_HW_VERSION	15:0	RO	—	This register contains the devices identification, including revision. Please contact your local technical sales representative for more details.
84	STICKY_ COUNTS_0	STAT_CNT_PRI_CD_ CHANGES	15:8	RO	—	Count of primary carrier detection status changes since last cleared. The count saturates at 255_d (0xFF). See Section 4.5.11 for procedure to clear the counts.
		RSVD	7:0	RO	—	Reserved.
85	RSVD	RSVD	15:0	RO	—	Reserved - do not modify.

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
86	CURRENT_ STATUS_0	RSVD	15	RO	—	Reserved
		STAT_CLEAR_COUNTS_ STATUS	14:13	RO	—	Clear counts status: 0 = Idle 1 = Reserved 2 = Indicates device has cleared the sticky counts 3 = Reserved. Part of a four-way handshake with CTRL_CLEAR_COUNTS. See Section 4.5.11 for more details on implementing the four way handshake for this operation.
		RSVD	12	RO	—	Reserved
		STAT_SLEEP	11	RO	—	Sleep status: 0 = Device is not in sleep 1 = Device is currently in sleep
		RSVD	10:8	RO	—	Reserved
		STAT_OUTPUT1_MODE	7:4	RO	—	Cable driver output1 (SDO1) output status: 0 = Mission Cable Driver SD/MADI slew rate 1 = Mission Cable Driver HD/3G slew rate 2 = Mission Cable Driver 6G/12G slew rate 3 = Reserved 4 = Reserved 5 = Balanced 6 = Mute 7 = Disabled
		STAT_OUTPUT0_MODE	3:0	RO	—	cable driver output0 (SDO0) output status: 0 = Mission Cable Driver SD/MADI slew rate 1 = Mission Cable Driver HD/3G slew rate 2 = Mission Cable Driver 6G/12G slew rate 3 = Reserved 4 = Reserved 5 = Balanced 6 = Mute 7 = Disabled

Table 5-4: Status Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
87	CURRENT_ STATUS_1	STAT_OUTPUT1_ DISABLE	15	RO	—	Cable driver output1 (SDO1) disable status: 0 = SDO1 is not disabled 1 = SDO1 is disabled
		STAT_OUTPUT0_ DISABLE	14	RO	—	Cable driver output0 (SDO0) disable status: 0 = SDO0 is not disabled 1 = SDO0 is disabled
		STAT_OUTPUT1_ MUTE	13	RO	—	Cable driver output1 (SDO1) mute status: 0 = SDO1 is not disabled 1 = SDO1 is disabled
		STAT_OUTPUT0_ MUTE	12	RO	—	Cable driver output0 (SDO0) mute status: 0 = SDO0 is not disabled 1 = SDO0 is disabled
		RSVD	11:9	RO	—	Reserved
		STAT_PRI_CD	8	RO	—	Primary carrier detection status. 0 = Primary carrier is not detected 1 = Primary carrier is detected
		RSVD	7	RO	—	Reserved
		STAT_OUTPUT1_ SLEW_RATE	6:5	RO	—	The current slew rate of cable driver output1 (SDO1): 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		STAT_OUTPUT0_ SLEW_RATE	4:3	RO	—	The current slew rate of cable driver output0 (SDO0): 0 = SD/MADI slew 1 = HD/3G slew 2 = 6G/12G slew
		RSVD	2:0	RO	—	Reserved
88 to BF	RSVD	RSVD	15:0	RO	—	Reserved

6. Application Information

6.1 Typical Application Circuit

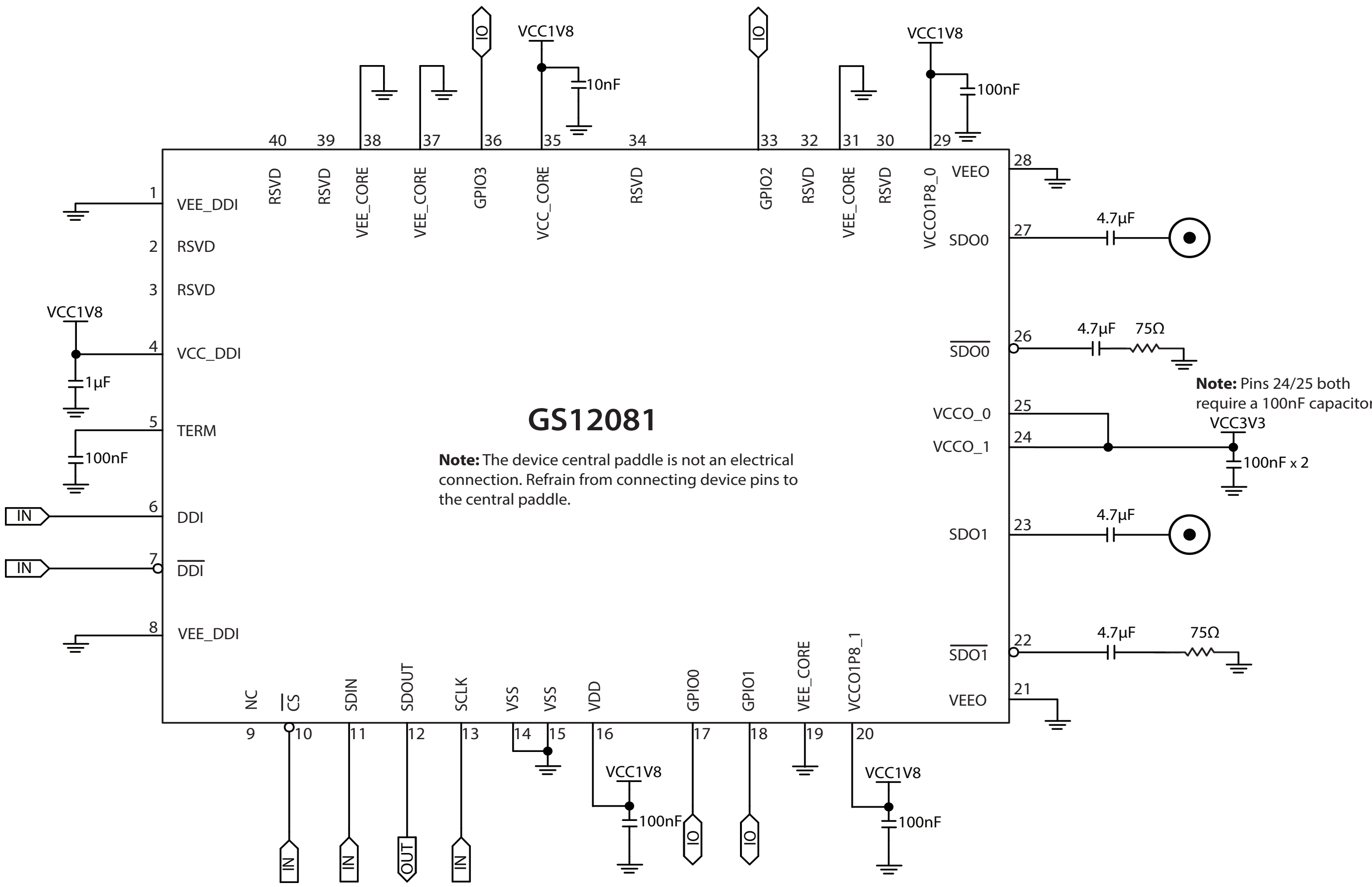


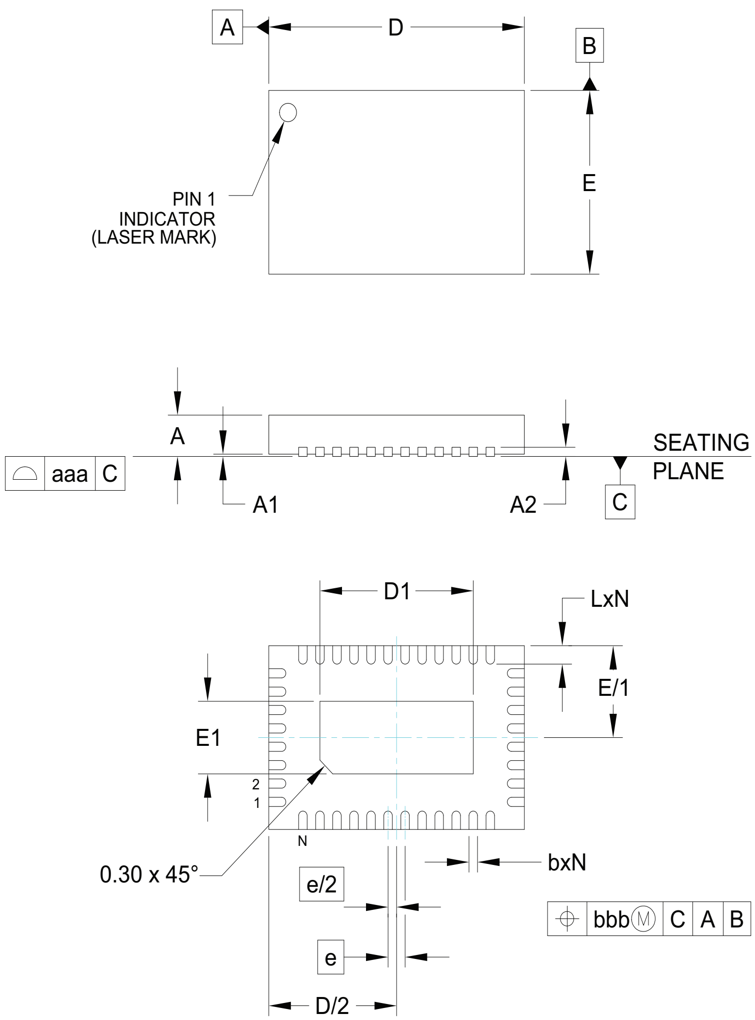
Figure 6-1: Typical Application Circuit

Note 1: 4.7µF AC-coupling capacitors are required on SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$.

Note 2: It is recommended that separate filtered supplies are used for the following three groups: (VCC_DDI, VCC_CORE), (VCCO1P8_0, VCCO1P8_1, VDD), (VCCO_0, VCCO_1). Multiple devices can share the same filtered supply plane. Contact your local technical representative for layout recommendations to achieve optimal performance.

7. Package & Ordering Information

7.1 Package Dimensions



DIM	DIMENSIONS MILLIMETERS MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.02)	
b	0.15	0.20	0.25
D	5.95	6.00	6.05
D1	3.45	3.60	3.70
E	3.95	4.00	4.05
E1	1.43	1.58	1.68
e		0.40 BSC	
L	0.30	0.40	0.50
N		40	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DIMENSION OF LEAD WIDTH APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.15 to 0.30mm FROM THE TERMINAL TIP.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

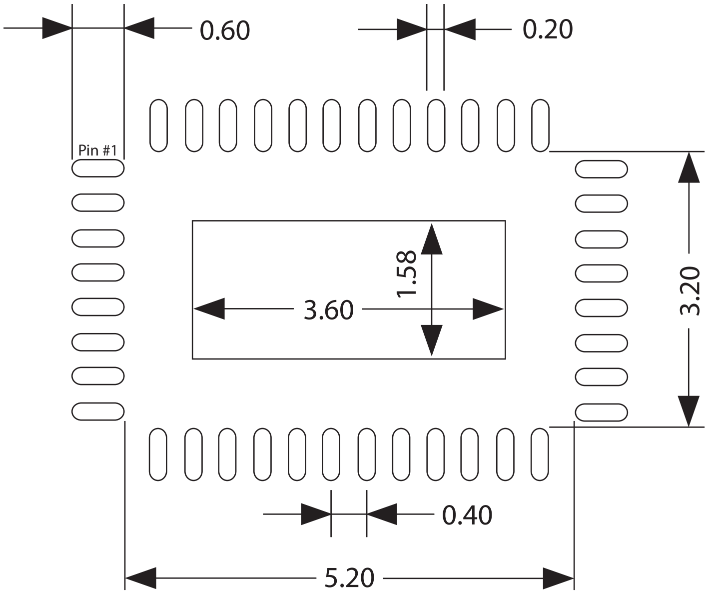


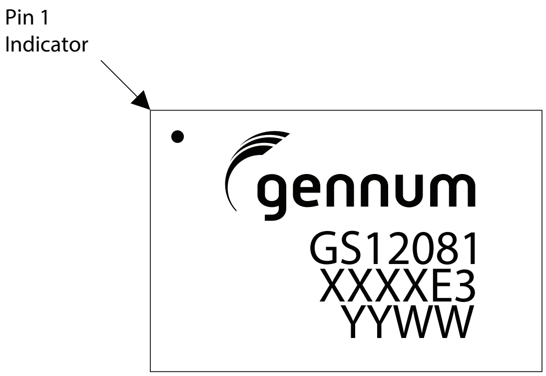
Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 4mm 40-pin QFN
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	40.0°C/W
Junction to Board Thermal Resistance, θ_{j-b}	32.0°C/W
Junction to Case Thermal Resistance, θ_{j-c}	36.0°C/W
Junction-to-Top Characterization Parameter, Psi, Ψ	<1.0°C/W
Pb-free and RoHS compliant	Yes

7.4 Marking Diagram



XXXX - Last 4 digits of Assembly lot
E3 - Pb-free & Green indicator
YYWW - Date Code

Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

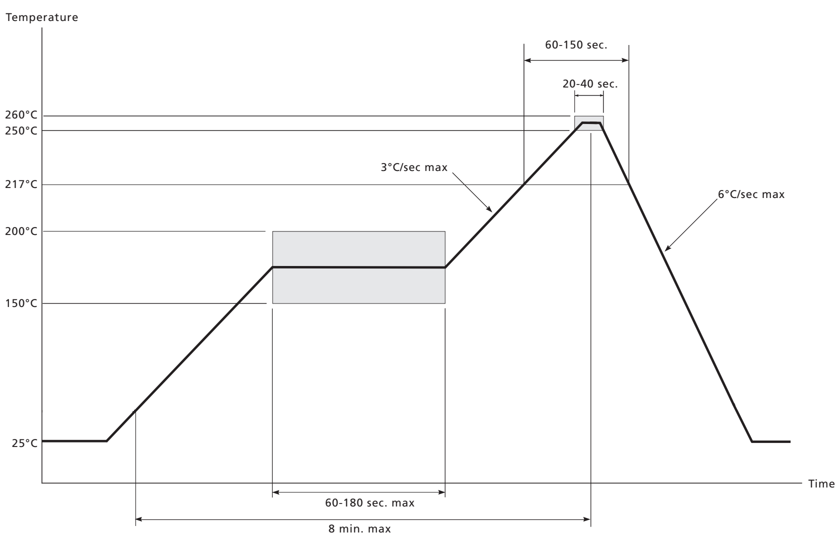


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Minimum Order Quantity	Format
GS12081-INE3	490	Tray
GS12081-INTE3	250	Tape and Reel
GS12081-INTE3Z	2500	Tape and Reel

Contact Information

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