

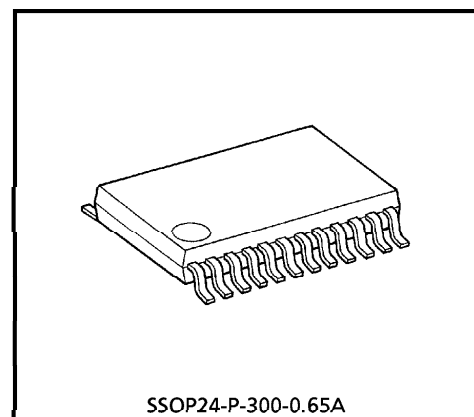
TA2120FN

LOW CONSUMPTION CURRENT STEREO HEADPHONE POWER AMPLIFIER FOR PORTABLE CD (3V USE)

The TA2120FN is a low consumption current stereo headphone power amplifier developed for portable CD players (3V). This IC has active bass boost, output limiter, input pin for beep sound.

FEATURES

- Low consumption current : $I_{CCQ} = 1.9\text{mA}$ (C-CUP) (typ.)
 $I_{CCQ} = 2.6\text{mA}$ (OCL) (typ.)
- Two kinds of gain mode available : $G_V = 16\text{dB}$ or 8.5dB
- Output power ($V_{CC} = 2.0\text{V}$, $f = 1\text{kHz}$, $\text{THD} = 10\%$, $R_L = 16\Omega$)
 $P_o = 8\text{mW}$ (typ.)
- Low noise : $V_{no} = -98\text{dBV}$ (typ.)
- Built-in the center amplifier ON/OFF function.
(Favorable for low dissipation current in the C-Couple output configuration)
- Built-in active bass boost system
- Built-in output limiter function
- Input pin for beep sound
- Excellent ripple rejection ratio
- Built-in capacitor for reducing buzz noise
- Built-in power mute
- Built-in a power on/off switch
- Operating supply voltage range ($T_a = 25^\circ\text{C}$) : $V_{CC}(\text{opr}) = 1.8 \sim 4.5\text{V}$



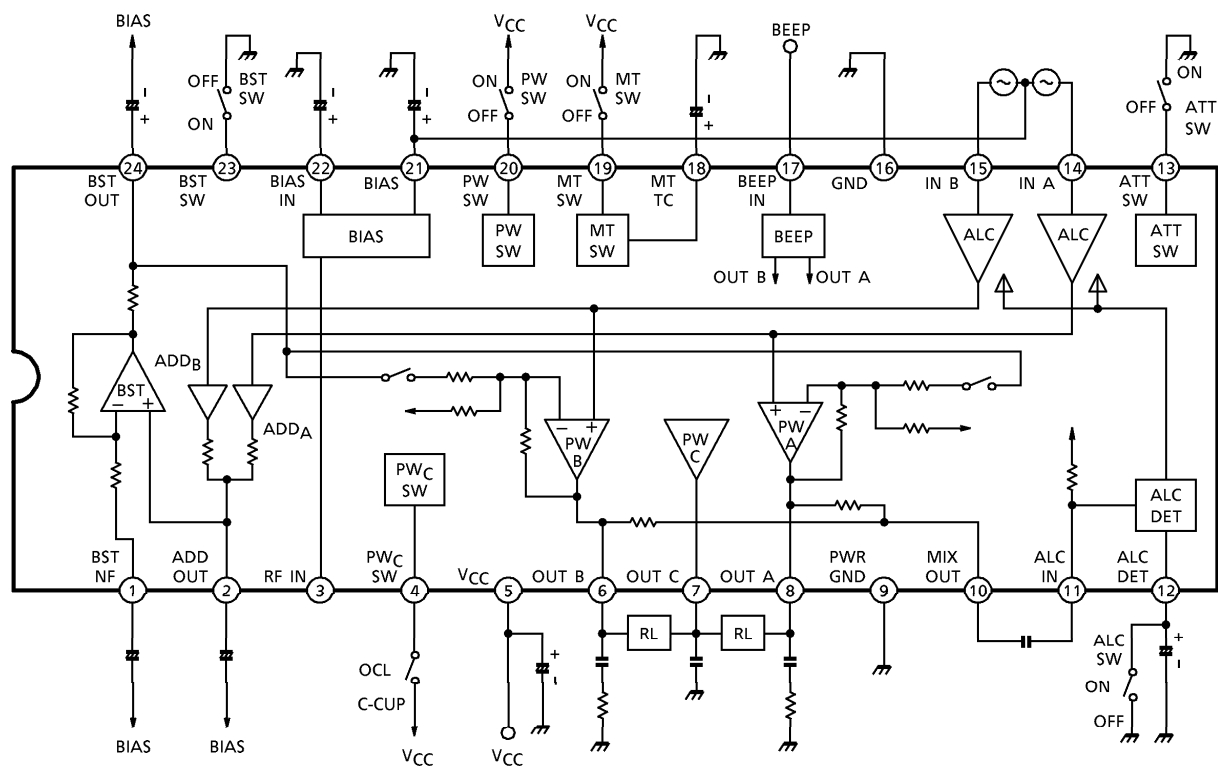
SSOP24-P-300-0.65A

Weight : 0.14g (Typ.)

980910EBA1

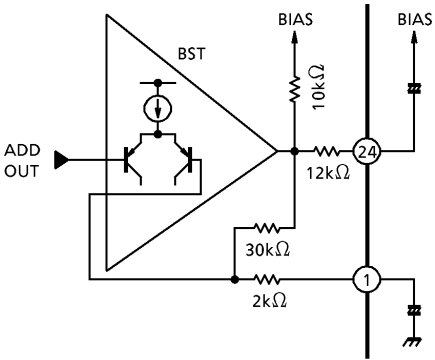
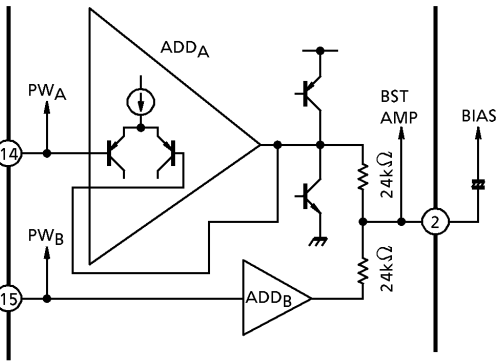
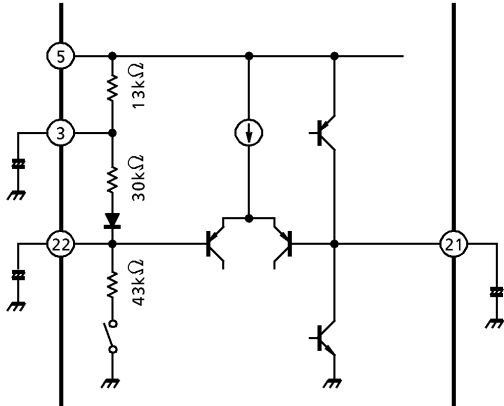
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury, or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

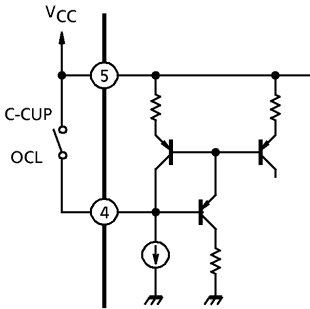
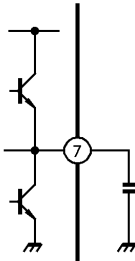
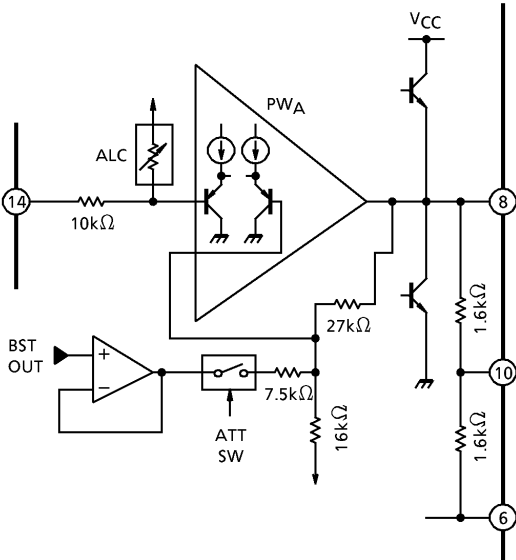
BLOCK DIAGRAM

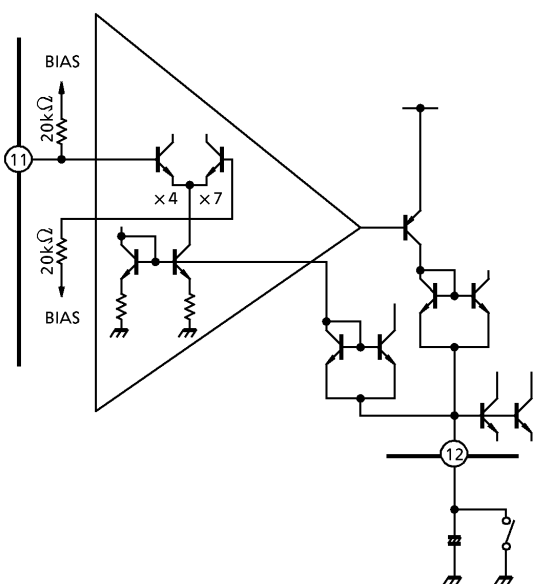
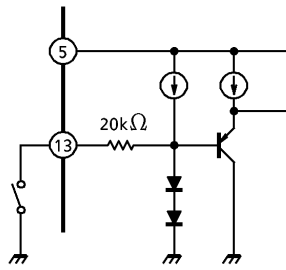
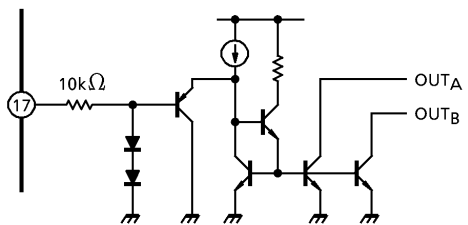


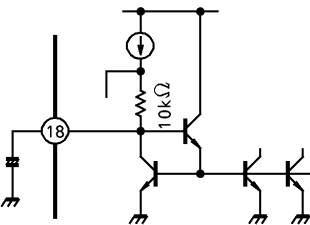
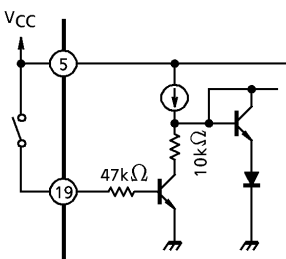
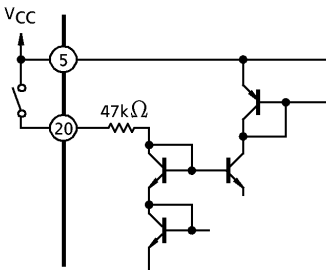
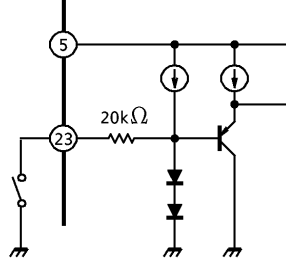
TERMINAL EXPLANATION

(Terminal voltage : Typical terminal voltage at no signal with test circuit, $V_{CC} = 2.4V$, $T_a = 25^\circ C$)

TERMINAL		FUNCTION	INTERNAL CIRCUIT	TERMINAL VOLTAGE (V)
No.	NAME			
1	BST NF	NF of BST amplifier		0.85
24	BST OUT	Output of BST amplifier (Terminal for filter)		0.85
2	ADD OUT	Output of ADD amplifier (Terminal for filter)		0.85
3	RF IN	Terminal for ripple filter circuit		1.44
21	BIAS	BIAS voltage		0.85
22	BIAS IN	Filter terminal for BIAS circuit		0.85

TERMINAL		FUNCTION	INTERNAL CIRCUIT	TERMINAL VOLTAGE (V)
No.	NAME			
4	PW _C SW	Center amplifier on / off switchover V _{CC} : Center amplifier off (C-Couple) OPEN : Center amplifier on (OCL)		—
7	OUT _C	Output of center amplifier (Common terminal for OCL output configuration)		0.85
5	V _{CC}	—	—	2.4
6	OUT _B	Output of power amplifier		0.85
8	OUT _A			0.85
14	IN _A	Input of power amplifier		0.85
15	IN _B			
10	MIX OUT	Output of power amplifier (Mixed)		0.85

TERMINAL		FUNCTION	INTERNAL CIRCUIT	TERMINAL VOLTAGE (V)
No.	NAME			
9	PWR GND	GND of power amplifier	—	0
11	ALC IN	Input terminal for ALC detector circuit		0.85
12	ALC DET	Smoothing for ALC detection, ALC on / off switchover (GND : ALC off OPEN : ALC on)		—
13	ATT SW	Power amplifier gain switchover (OPEN / V _{CC} : ATT off (G _V = 16dB) GND : ATT on (G _V = 8.5dB)		—
16	GND	GND of input stage in power amplifier	—	0
17	BEEP IN	Input terminal for Beep sound It receive beep sound from microcomputer. And power amplifier outputs this beep sound.		0

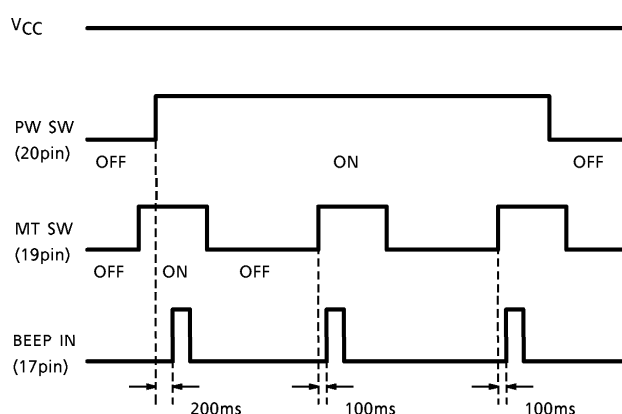
TERMINAL		FUNCTION	INTERNAL CIRCUIT	TERMINAL VOLTAGE (V)
No.	NAME			
18	MT TC	Terminal of mute smoothing Smoothing for shock noise at power muting switch over		1.4
19	MT SW	Power mute switchover (GND / OPEN : Mute off VCC : Mute on)		—
20	PW SW	Power on / off switchover (VCC : Power on GND / OPEN : Power off)		—
23	BST SW	Bst on / off switchover (BST on : OPEN / VCC BST off : GND)		—

APPLICATION NOTE

1. Beep Sound

Beep sound signals from, for example, a micro controller can be received through the beep input pin 17. At power mute mode, PW_A and PW_B are turned off. The current of the beep signal input to be via beep amplifier is amplified at the output stage of PW_A and PW_B . The output from beep amplifier becomes the constant voltage source. As a result, the beep sound is output to the headphone load.

If the input signal for beep (Pin 17) is not, this terminal should be fixed GND level.



2. Power Switch

As long as the power switch is not connect to V_{CC} , the IC does not operate.

If external noise causes malfunctions, we recommend to connect a pull-down resistor externally (Sensitivity of the power mute switch is high).

3. Center Amplifier (PW_C)

Terminal for PW_C output is common terminal for OCL output configuration.

PW_C ON/OFF mode is controlled by PW_C switch (Pin 4).

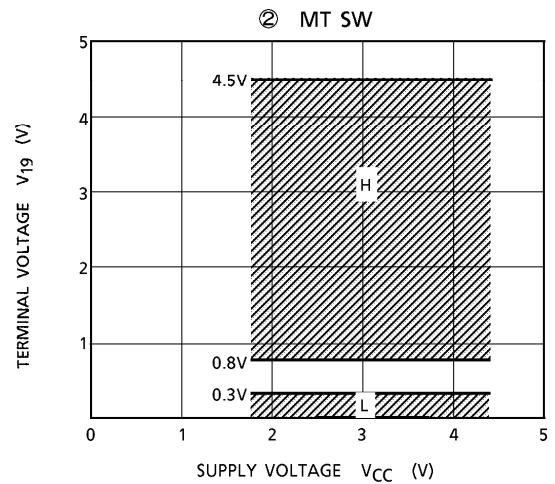
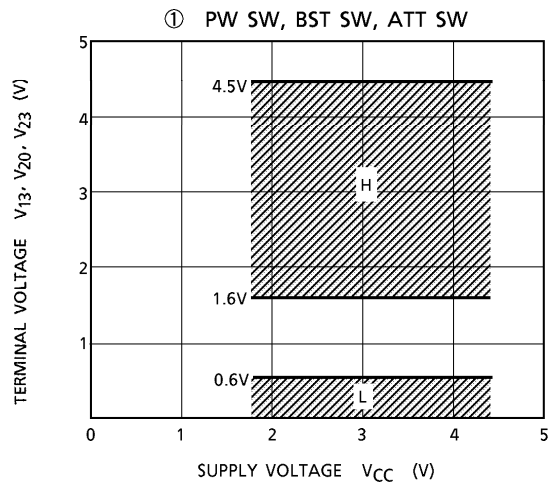
To reduce the consumption current, PW_C should be turned off by this switch.

PW_C SW	(	OPEN	: OCL
		V_{CC}	: C-Couple

4. Terminal of RF IN (3pin)

Adding Capacitor (Recommendation : $10\mu F$) to terminal of RF IN (Pin 3), the ripple rejection ratio is improved by secondly ripple filter (In the C-Couple output configuration , this capacitor should be connected.)

5. Threshold Voltage of Each Switches



	PW SW (V_{20})
'H'	OPERATING
'L' OPEN	IC OFF

	MT SW (V_{19})
'H'	MUTE ON
'L' OPEN	MUTE OFF

	ATT SW (V_{13})	BST SW (V_{23})
'H' OPEN	ATT OFF	BST ON
'L'	ATT ON	BST OFF

6. External capacitor

These capacitors which prevent oscillation of power amplifier and de-coupled at terminals of BIAS and V_{CC} need to be small temperature coefficient and excellent frequency characteristic.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	4.5	V
Output Current	I _o (peak)	100	mA
Power Dissipation	P _D (Note)	550	mW
Operating Temperature	T _{opr}	– 25~75	°C
Storage Temperature	T _{stg}	– 55~150	°C

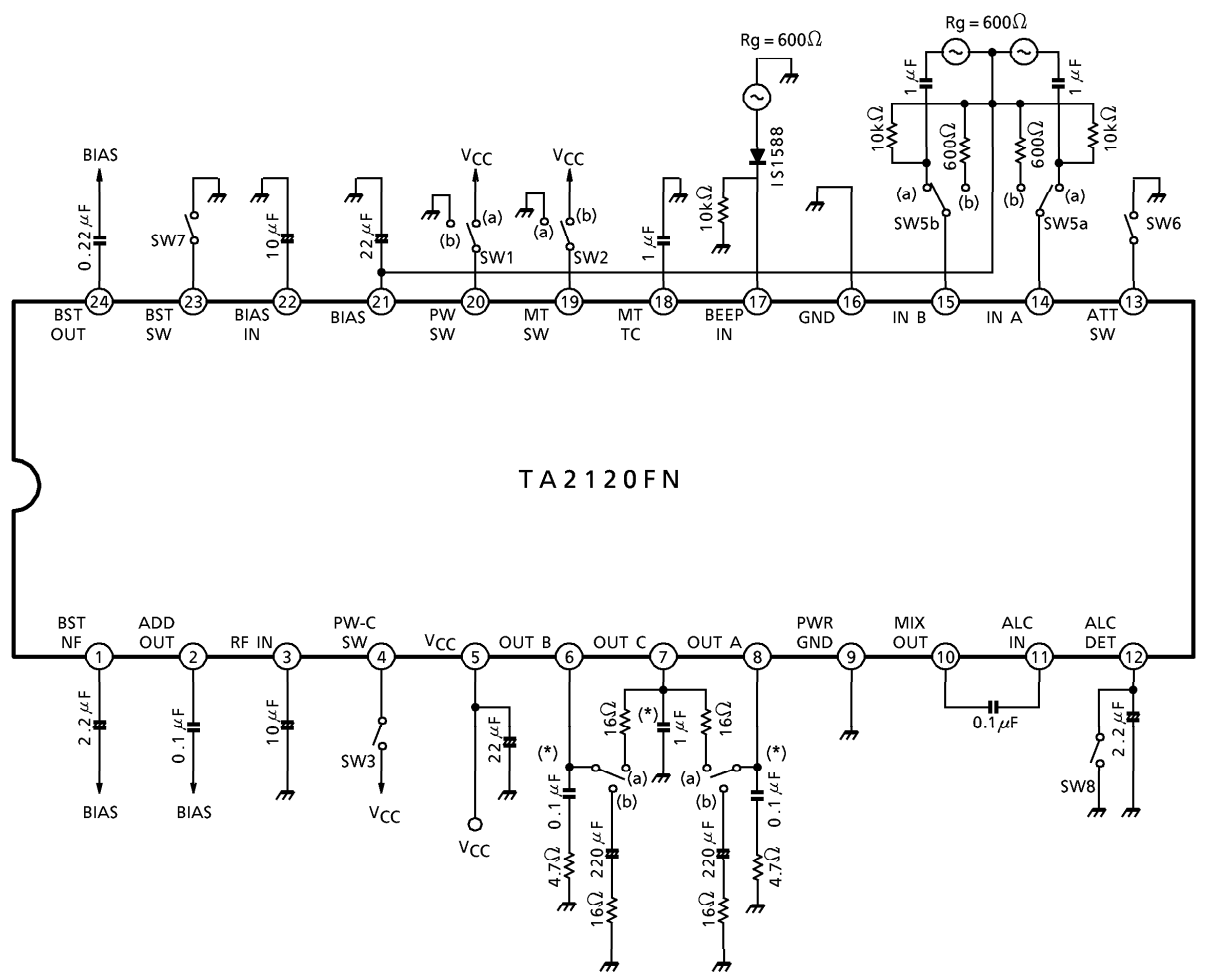
(Note) Deleted above 25°C in the proportion of 4.4mW/1°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified : V_{CC} = 2.4V, R_g = 600Ω, R_L = 16Ω, f = 1kHz, Ta = 25°C
 SW1 : a, SW2 : a, SW3 : OPEN, SW4 : a, SW5 : a, SW6 : OPEN, SW7 : ON,
 SW8 : ON

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Supply Current		I _{CC1}	—	IC OFF (C-Couple) SW1 : b, SW2 : b, SW3 : ON	—	0.1	5	μA
		I _{CC2}		IC OFF (OCL) SW1 : b, SW2 : b	—	0.1	5	μA
		I _{CC3}		MUTE ON (C-Couple) SW2 : b, SW3 : ON	—	1	2	mA
		I _{CC4}		MUTE ON (OCL) SW2 : b	—	1.7	3	mA
		I _{CC5}		No signal (C-Couple) SW3 : ON	—	1.9	3.5	mA
		I _{CC6}		No signal (OCL)	—	2.6	4.5	mA
Consumption Supply Current		I _{CC7}	—	P _O = 0.5mW + 0.5mW (C-Couple), SW3 : ON	—	6.6	—	mA
		I _{CC8}		P _O = 0.5mW + 0.5mW (OCL)	—	12.1	—	
Power Amplifier Stage	Voltage Gain (1)	G _{V1}	—	V _O = – 22dBV, SW6 : GND	5.5	8.5	10.5	dB
	Voltage Gain (2)	G _{V2}	—	V _O = – 22dBV	14	16	18	
	Output Power	P _{omax}	—	THD = 10%, V _{CC} = 2.0V	5	8	—	mW
	Total Harmonic Distortion	THD	—	V _O = – 12.2dBV	—	0.1	0.5	%
	Output Noise Voltage	V _{no}	—	R _g = 600Ω, Filter : IHF-A, SW5 : b	—	– 98	– 92	dBV
	Crosstalk	CT	—	V _O = – 12.2dBV	24	40	—	dB
	Ripple Rejection Ratio	RR	—	V _{CC} = 1.8V, fr = 100Hz, V _r = – 20dBV	69	75	—	dB
	Mute Attenuation	MUTE	—	V _O = – 12.2dBV, SW2 : b	80	90	—	dB
	Beep Voltage	VBEEP	—	V Beep IN = 0dBV, SW2 : b	– 56	– 51	– 46	dBV
Boost Gain		B _{st}	—	V _O = – 30dBV, f = 100Hz, SW7 : ON→OPEN	9	11.5	14	dB
Output Limiter Level		V _{ALC}	—	V _{in} = – 20dBV, SW8 : OPEN	– 41.5	– 39.5	– 37.5	dBV

TEST CIRCUIT



(*) MONOLITHIC CERAMIC CAPACITOR

The schematic diagram illustrates the pin connections and component values for the TA2120FN integrated circuit. The chip is shown with pins 1 through 24. Key components and connections include:

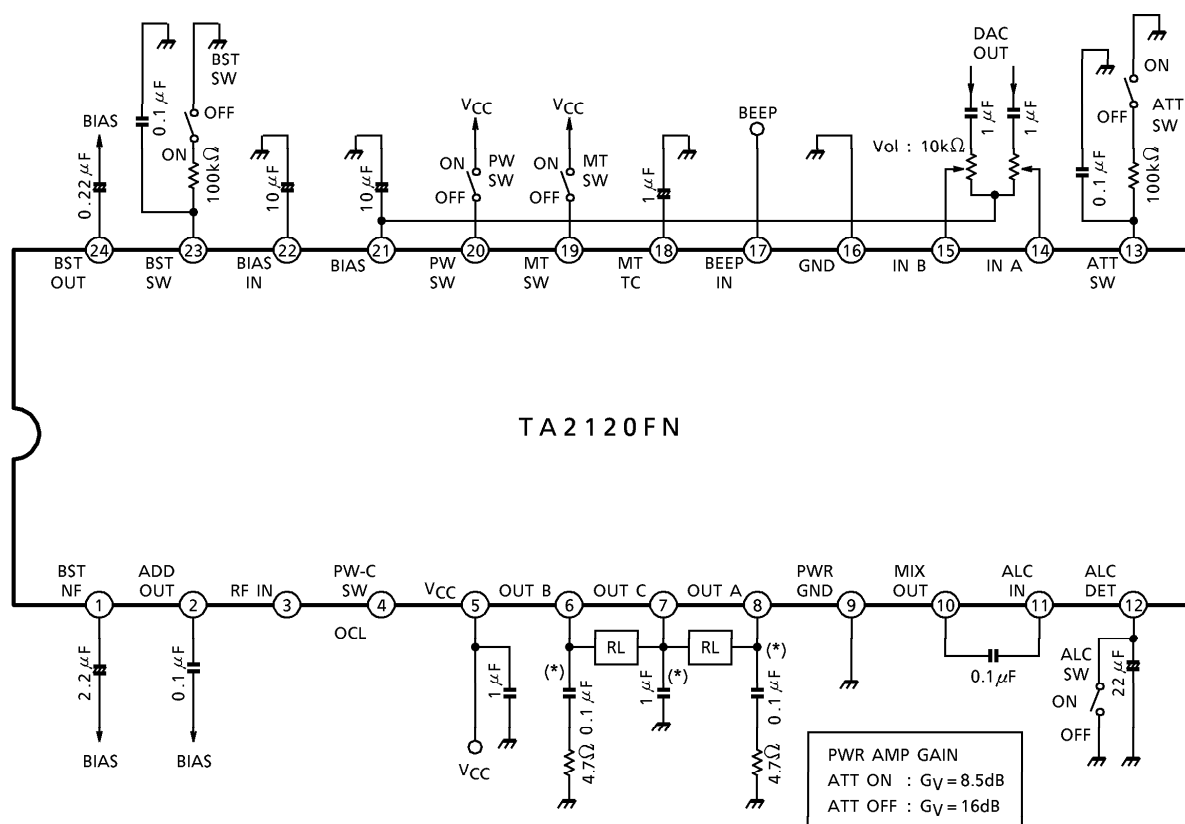
- Pin 1 (BST NF):** Connected to a 2.2 μF capacitor to BIAS.
- Pin 2 (ADD OUT):** Connected to a 0.1 μF capacitor to BIAS.
- Pin 3 (RF IN):** Connected to a 10 μF capacitor to ground.
- Pin 4 (PW-C SW):** Connected to C-CUP.
- Pin 5 (VCC):** Connected to a 1 μF capacitor to VCC.
- Pin 6 (OUT B):** Connected to a 220 μF capacitor to ground and a load resistor (RL) to VCC.
- Pin 7 (OUT C):** Connected to a 4.7 Ω resistor to ground and a 0.1 μF capacitor to VCC.
- Pin 8 (OUT A):** Connected to a 4.7 Ω resistor to ground, a 220 μF capacitor to ground, and a load resistor (RL) to VCC.
- Pin 9 (PWR GND):** Connected to ground.
- Pin 10 (MIX OUT):** Connected to ground.
- Pin 11 (ALC IN):** Connected to a capacitor to ALC SW.
- Pin 12 (ALC DET):** Connected to a 22 μF capacitor to ground and ALC SW.
- Pin 13 (ATT SW):** Connected to a 100 Ω resistor to ground and a 0.1 μF capacitor to VCC.
- Pin 14 (IN A):** Connected to a 1 μF capacitor to ground and a 10 $\text{k}\Omega$ resistor to VCC.
- Pin 15 (IN B):** Connected to a 1 μF capacitor to ground and a 10 $\text{k}\Omega$ resistor to VCC.
- Pin 16 (GND):** Connected to ground.
- Pin 17 (BEEP IN):** Connected to a 1 μF capacitor to ground.
- Pin 18 (MT TC):** Connected to a 1 μF capacitor to ground.
- Pin 19 (MT SW):** Connected to a switch to VCC.
- Pin 20 (PW SW):** Connected to a switch to VCC.
- Pin 21 (BIAS):** Connected to a 10 μF capacitor to ground.
- Pin 22 (BIAS IN):** Connected to a 10 μF capacitor to ground.
- Pin 23 (BST SW):** Connected to a 100 $\text{k}\Omega$ resistor to ground and a switch to VCC.
- Pin 24 (BST OUT):** Connected to a 0.22 μF capacitor to BIAS.

Power Amplifier Gain Table:

ATT	Gain (G_V)
ON	8.5 dB
OFF	16 dB

1998-09-25 11/16

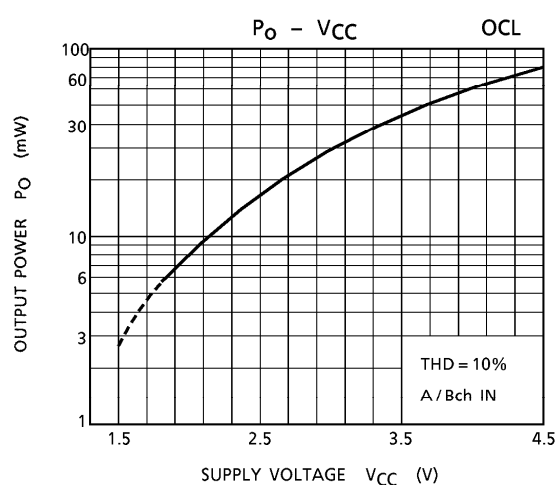
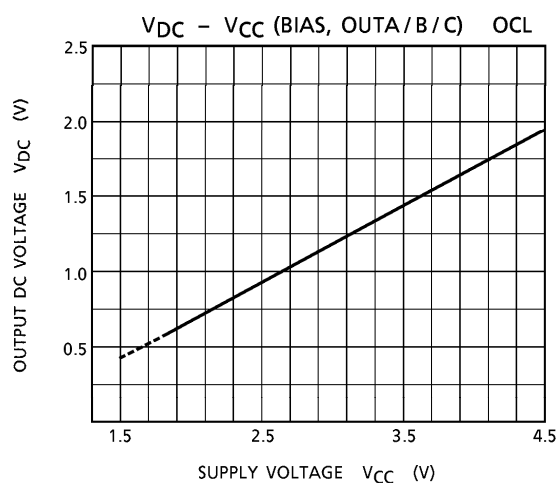
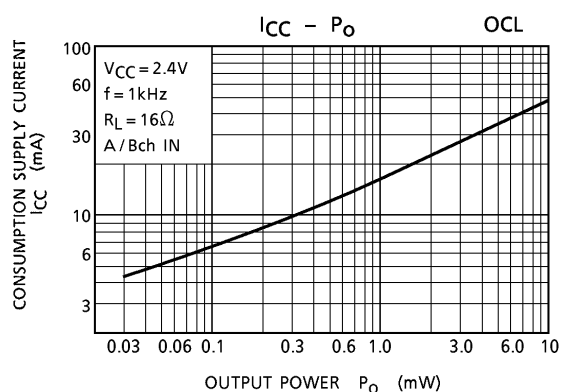
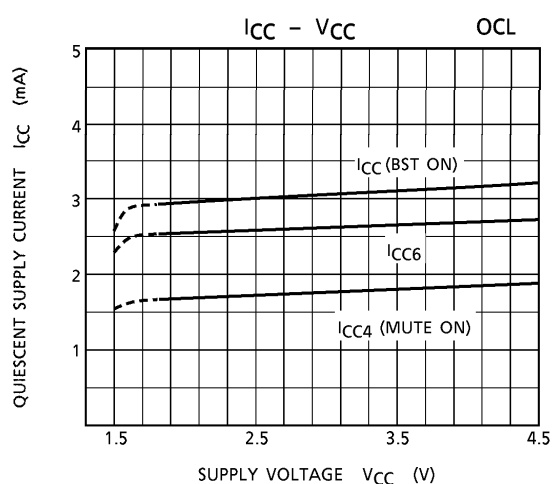
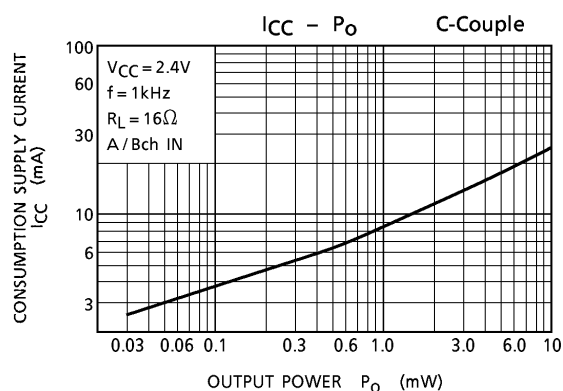
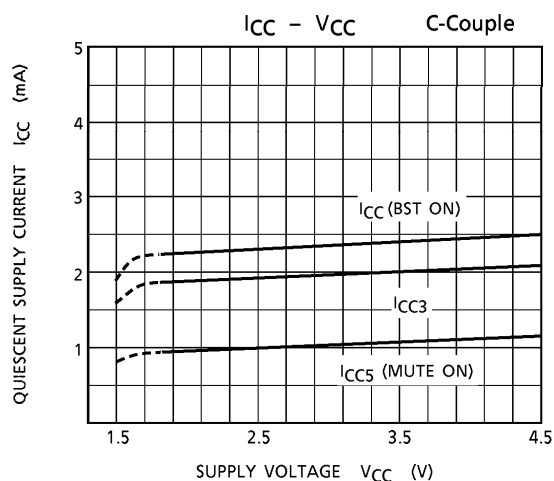
APPLICATION CIRCUIT 2 (OCL MODE)

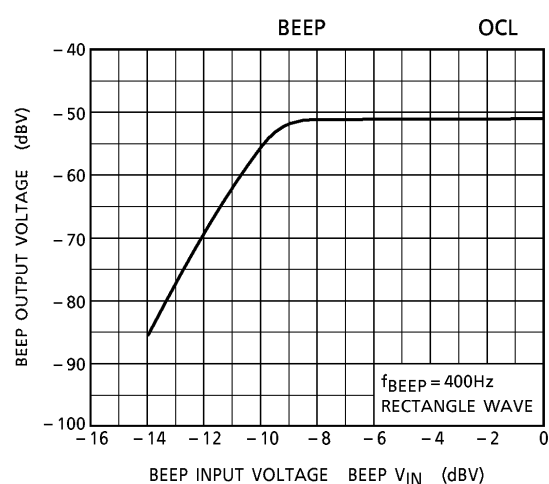
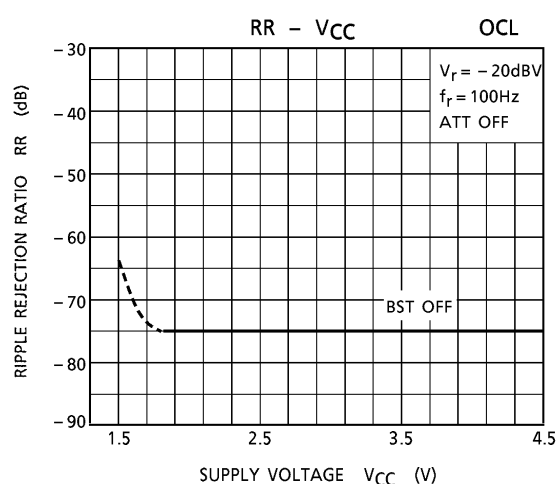
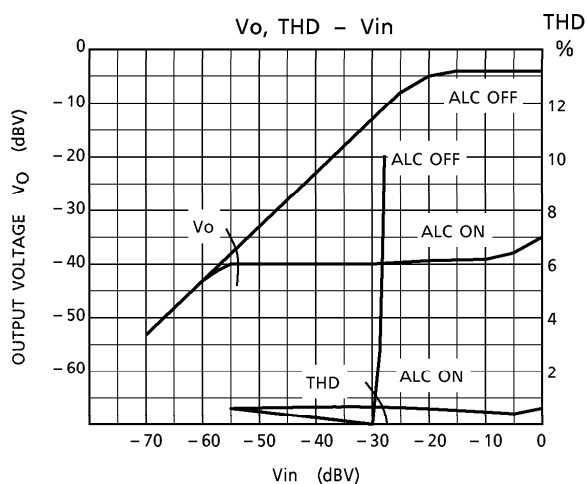
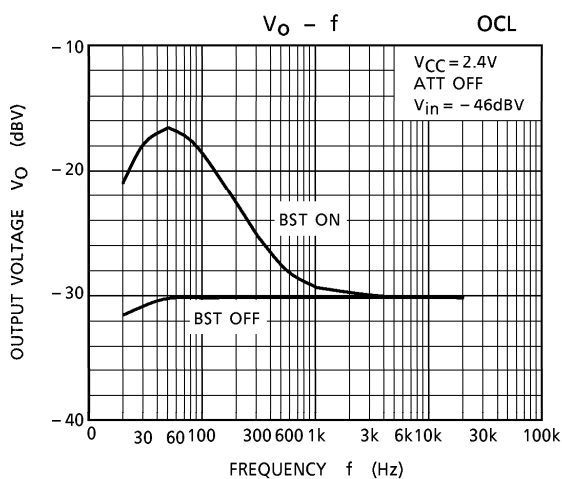
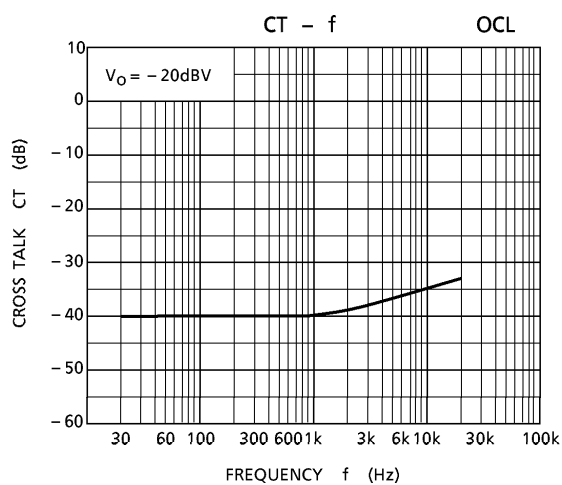
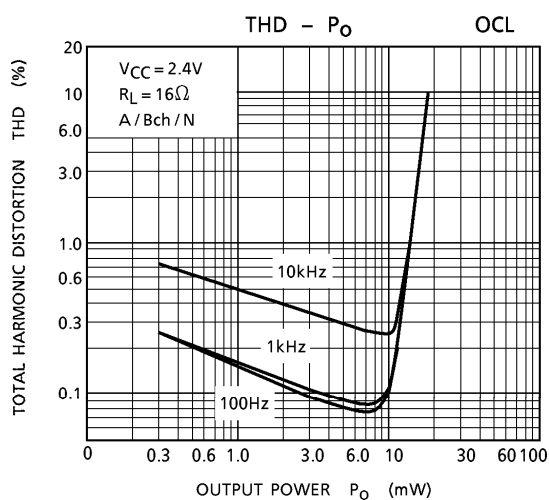


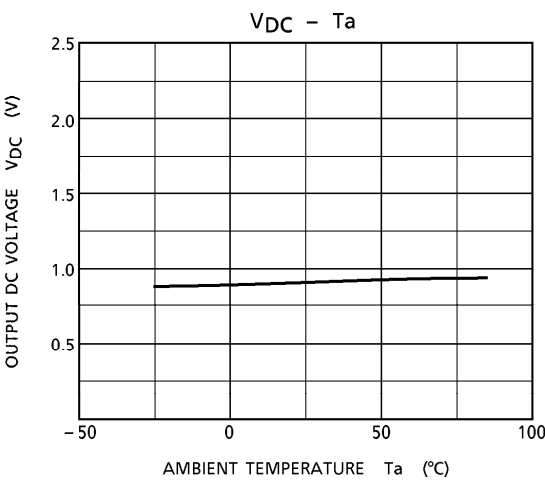
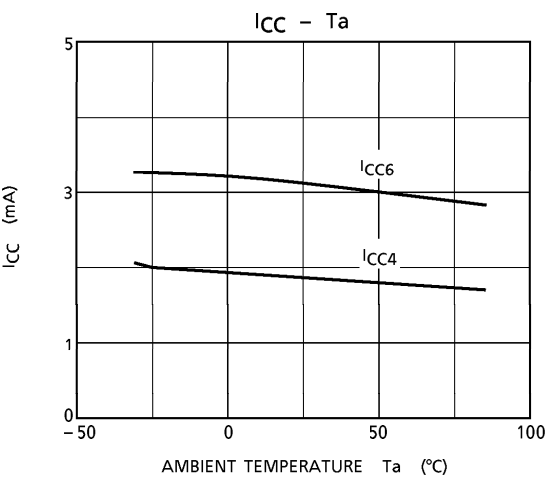
(*) MONOLITHIC CERAMIC CAPACITOR

CHARACTERISTICS

(Unless otherwise specified : $V_{CC} = 2.4V$, $R_L = 16\Omega$, $R_g = 600\Omega$, $f = 1kHz$, $T_a = 25^\circ C$, OCL, ATT OFF)



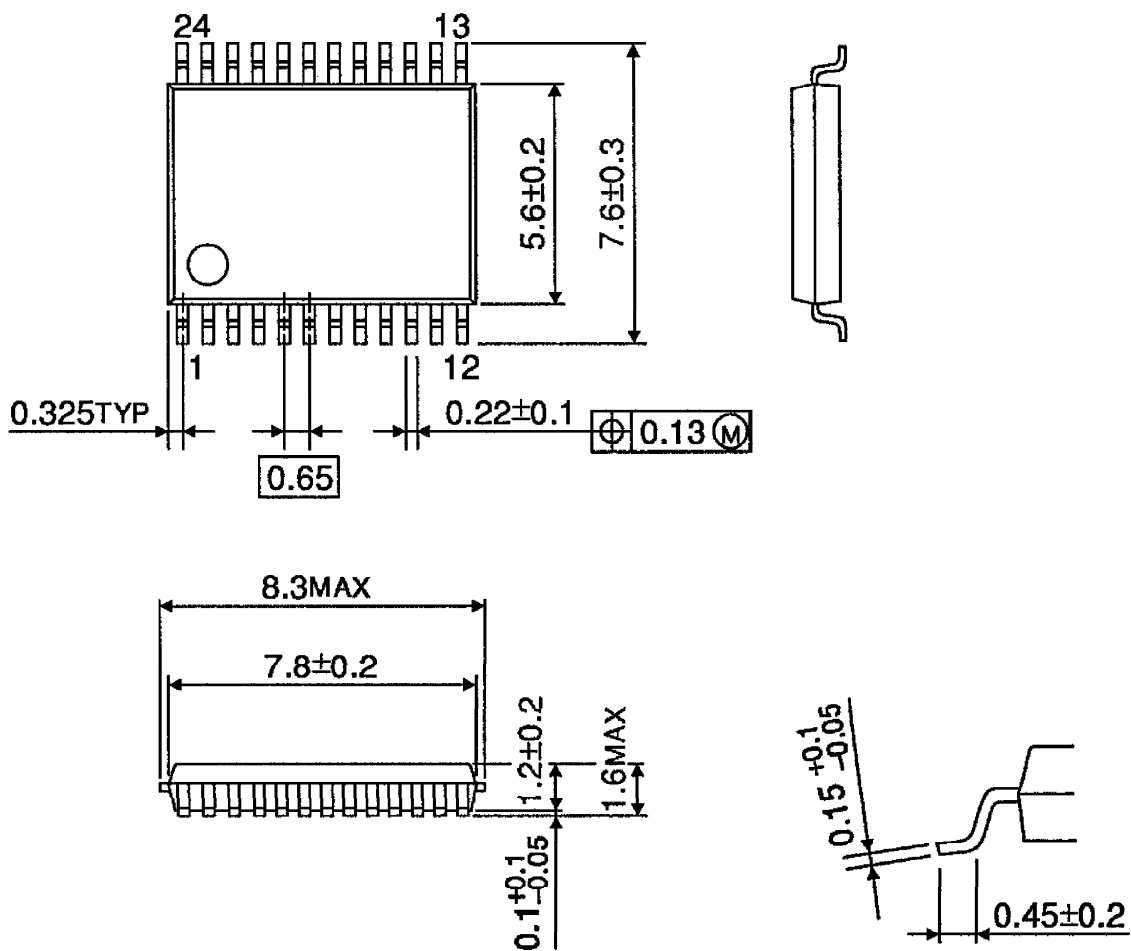




OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)