# 74LVT16244B; 74LVTH16244B

## 3.3 V 16-bit buffer/driver; 3-state

Rev. 11 — 1 March 2012 Product data sheet

## 1. General description

The 74LVT16244B; 74LVTH16244B is a high-performance BiCMOS product designed for $V_{CC}$ operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

## 2. Features and benefits

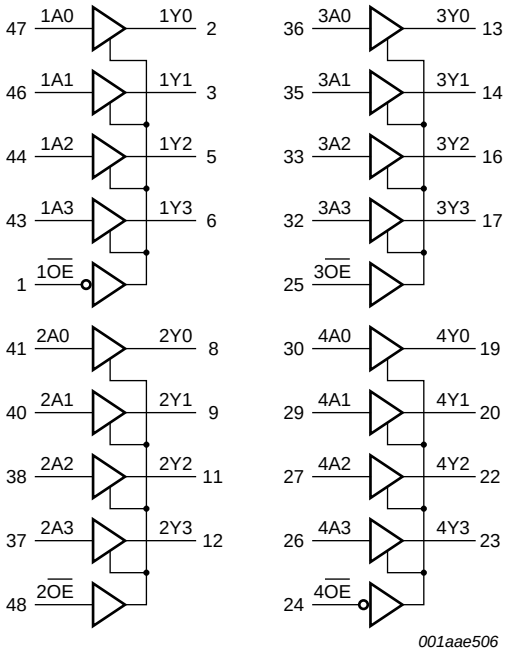
- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and −32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
  - JESD78B Class II exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

## 3. Ordering information

**Table 1. Ordering information**

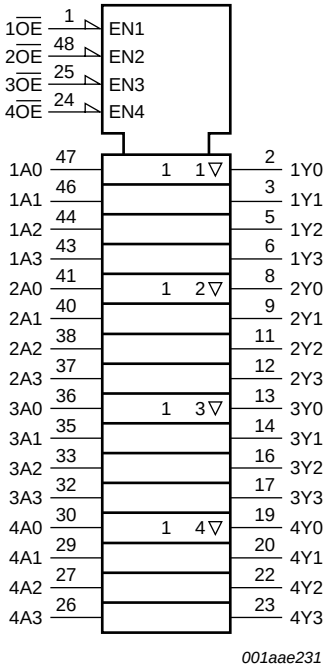
| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVT16244BDL | −40 °C to +85 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74LVTH16244BDL | | | | |
| 74LVT16244BDGG | −40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVTH16244BDGG | | | | |
| 74LVT16244BEV | −40 °C to +85 °C | VFBGA56 | plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm | SOT702-1 |
| 74LVT16244BBX | −40 °C to +125 °C | HXQFN60 | plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 × 6 × 0.5 mm | SOT1134-2 |
| 74LVTH16244BBX | | | | |

## 4. Functional diagram




Pin numbers are shown for SSOP48 and TSSOP48 packages only.

**Fig 1. Logic symbol**




Pin numbers are shown for SSOP48 and TSSOP48 packages only.

**Fig 2. IEC logic symbol**

# 5. Pinning information

## 5.1 Pinning

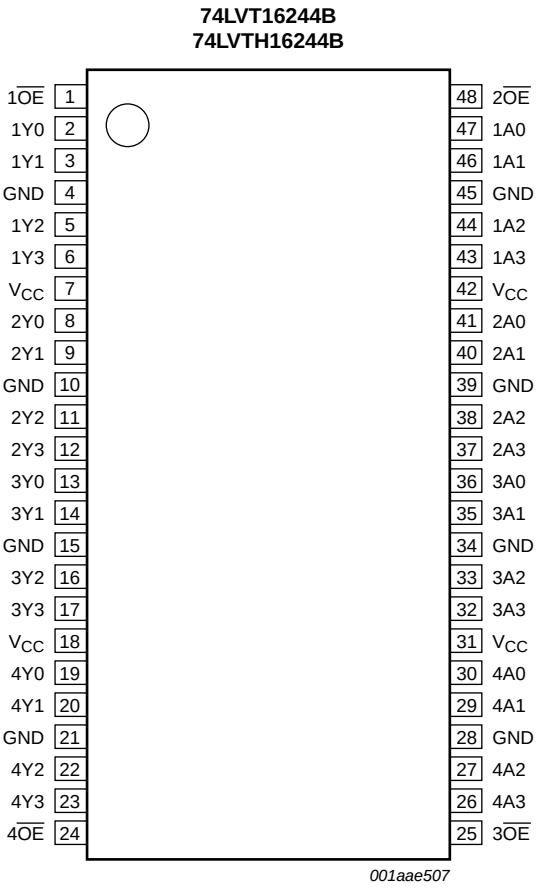



**Fig 3. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)**

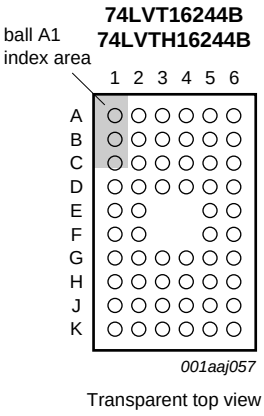
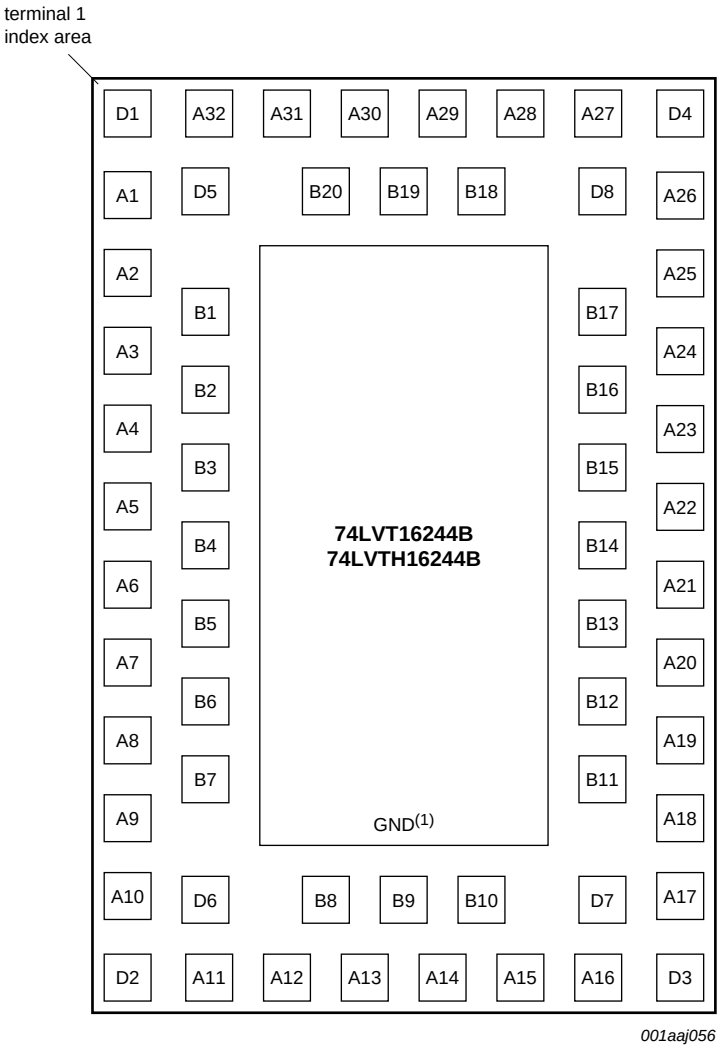



**Fig 4. Pin configuration SOT702-1 (VFBGA56)**




Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

**Fig 5. Pin configuration SOT1134-2 (HXQFN60)**

### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | | | Description |
|---|---|---|---|---|
| | SOT370-1 and SOT362-1 | SOT702-1 | SOT1134-2 | |
| 1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$ | 1, 48, 25, 24 | A1, A6, K6, K1 | A30, A29, A14, A13 | output enable input (active LOW) |
| 1Y0 to 1Y3 | 2, 3, 5, 6 | B2, B1, C2, C1 | B20, A31, D5, D1 | data output |
| 2Y0 to 2Y3 | 8, 9, 11, 12 | D2, D1, E2, E1 | A2, B2, B3, A5 | data output |
| 3Y0 to 3Y3 | 13, 14, 16, 17 | F1, F2, G1, G2 | A6, B5, B6, A9 | data output |
| 4Y0 to 4Y3 | 19, 20, 22, 23 | H1, H2, J1, J2 | D2, D6, A12, B8 | data output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | B3, B4, D3, D4, G3, G4, J3, J4 | A32, A3, A8, A11, A16, A19, A24, A27 | ground (0 V) |
| $V_{CC}$ | 7, 18, 31, 42 | C3, C4, H3, H4 | A1, A10, A17, A26 | supply voltage |
| 1A0 to 1A3 | 47, 46, 44, 43 | B5, B6, C5, C6 | B18, A28, D8, D4 | data input |
| 2A0 to 2A3 | 41, 40, 38, 37 | D5, D6, E5, E6 | A25, B16, B15, A22 | data input |
| 3A0 to 3A3 | 36, 35, 33, 32 | F6, F5, G6, G5 | A21, B13, B12, A18 | data input |
| 4A0 to 4A3 | 30, 29, 27, 26 | H6, H5, J6, J5 | D3, D7, A15, B10 | data input |
| n.c. | - | A2, A3, A4, A5, K2, K3, K4, K5 | A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19 | not connected |

## 6. Functional description

**Table 3. Function table[1]**

| Control | Input | Output |
|---|---|---|
| **n$\overline{OE}$** | **nAn** | **nYn** |
| L | L | L |
| L | H | H |
| H | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +4.6 | V |
| $V_I$ | input voltage | | [1] | –0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | –50 | - | mA |

**Table 4. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_O$ | output current | output in LOW-state | | - | 128 | mA |
| | | output in HIGH-state | | −64 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_j$ | junction temperature | | [2] | - | 150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +85 °C; | | | | |
| | | (T)SSOP48 package | [3] | - | 500 | mW |
| | | VFBGA56 package | [4] | - | 1000 | mW |
| | | HXQFN60 package | [4] | - | 1000 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] Above 60 °C the value of $P_{tot}$ derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of $P_{tot}$ derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.7 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.8 | V |
| $I_{OH}$ | HIGH-level output current | | −32 | - | - | mA |
| $I_{OL}$ | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; $f_i \geq 1$ kHz | - | - | 64 | mA |
| $T_{amb}$ | ambient temperature | in free-air | −40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C** [1] | | | | | | | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.7 V; $I_{IK}$ = –18 mA | | –1.2 | –0.85 | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –100 µA; $V_{CC}$ = 2.7 V to 3.6 V | | $V_{CC}$ – 0.2 | $V_{CC}$ | - | V |
| | | $I_{OH}$ = –8 mA; $V_{CC}$ = 2.7 V | | 2.4 | 2.5 | - | V |
| | | $I_{OH}$ = –32 mA; $V_{CC}$ = 3.0 V | | 2.0 | 2.3 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.7 V | | | | | |
| | | $I_{OL}$ = 100 µA | | - | 0.07 | 0.2 | V |
| | | $I_{OL}$ = 24 mA | | - | 0.3 | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | | | | | |
| | | $I_{OL}$ = 16 mA | | - | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 32 mA | | - | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 64 mA | | - | 0.4 | 0.55 | V |
| $I_I$ | input leakage current | all input pins; $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | | - | 0.1 | 10 | µA |
| | | control pins; $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | | - | 0.1 | ±1.0 | µA |
| | | data pins; $V_{CC}$ = 3.6 V | [2] | | | | |
| | | $V_I$ = $V_{CC}$ | | - | 0.1 | 1 | µA |
| | | $V_I$ = 0 V | | –5 | –0.1 | - | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | | - | 0.1 | ±100 | µA |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 3 V; $V_I$ = 0.8 V | [3] | 75 | 135 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 3 V; $V_I$ = 2.0 V | | - | –135 | –75 | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | nAn input; $V_{CC}$ = 0 V to 3.6 V; $V_I$ = 3.6 V | | 500 | - | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | nAn input; $V_{CC}$ = 0 V to 3.6 V; $V_I$ = 3.6 V | | - | - | –500 | µA |
| $I_{LO}$ | output leakage current | output in HIGH-state when $V_O$ > $V_{CC}$; $V_O$ = 5.5 V; $V_{CC}$ = 3.0 V | | - | 50 | 125 | µA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2$ V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; $\overline{nOE}$ = don't care | [4] | - | 1 | ±100 | µA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | output HIGH: $V_O$ = 3.0 V | | - | 0.5 | 5 | µA |
| | | output LOW: $V_O$ = 0.5 V | | –5 | +0.5 | - | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | | |
| | | output HIGH | | - | 0.07 | 0.12 | mA |
| | | output LOW | | - | 4.0 | 6.0 | mA |
| | | outputs disabled | [5] | - | 0.07 | 0.12 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3.0 V to 3.6 V; one input at $V_{CC}$ – 0.6 V other inputs at $V_{CC}$ or GND | [6] | - | 0.1 | 0.2 | mA |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_I$ | input capacitance | $V_I$ = 0 V or 3.0 V | - | 3 | - | pF |
| $C_O$ | output capacitance | outputs disabled; $V_O$ = 0 V or 3.0 V | - | 9 | - | pF |

[1] Typical values are measured at $V_{CC}$ = 3.3 V and at $T_{amb}$ = 25 °C.

[2] Unused pins at $V_{CC}$ or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC}$ = 1.2 V to $V_{CC}$ = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.

[5] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

## 10. Dynamic characteristics

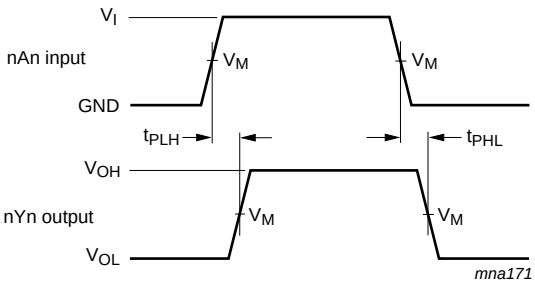
**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C[1]** | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nAn to nYn; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.5 | 1.8 | 3.2 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nAn to nYn; see Figure 6 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.5 | 1.7 | 3.2 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $n\overline{OE}$ to nYn; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 5.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.3 | 4.0 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | $n\overline{OE}$ to nYn; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 5.3 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.1 | 4.0 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $n\overline{OE}$ to nYn; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 5.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.2 | 4.5 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | $n\overline{OE}$ to nYn; see Figure 7 | | | | |
| | | $V_{CC}$ = 2.7 V | - | - | 4.4 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.9 | 4.0 | ns |

[1] Typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

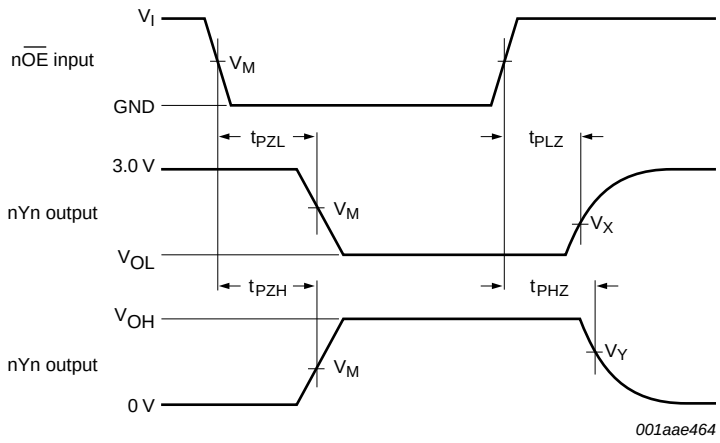
## 11. Waveforms




Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nAn) to output (nYn)**



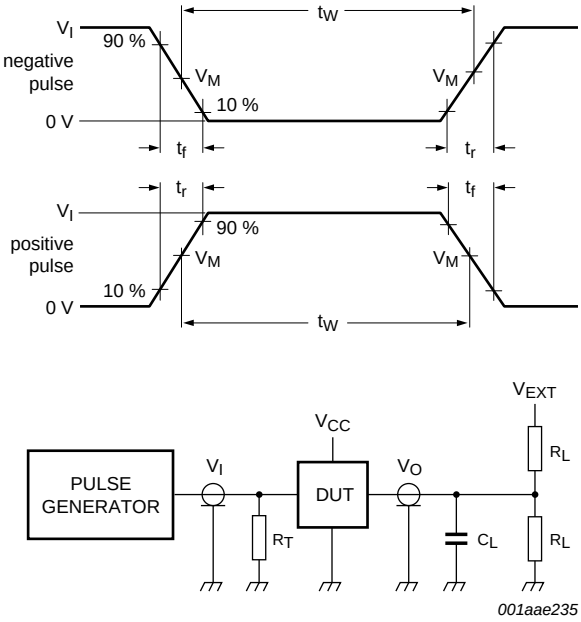

Measurements points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 7. 3-state output enable and disable times**

**Table 8. Measurement points**

| Input | Output | | |
|---|---|---|---|
| $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

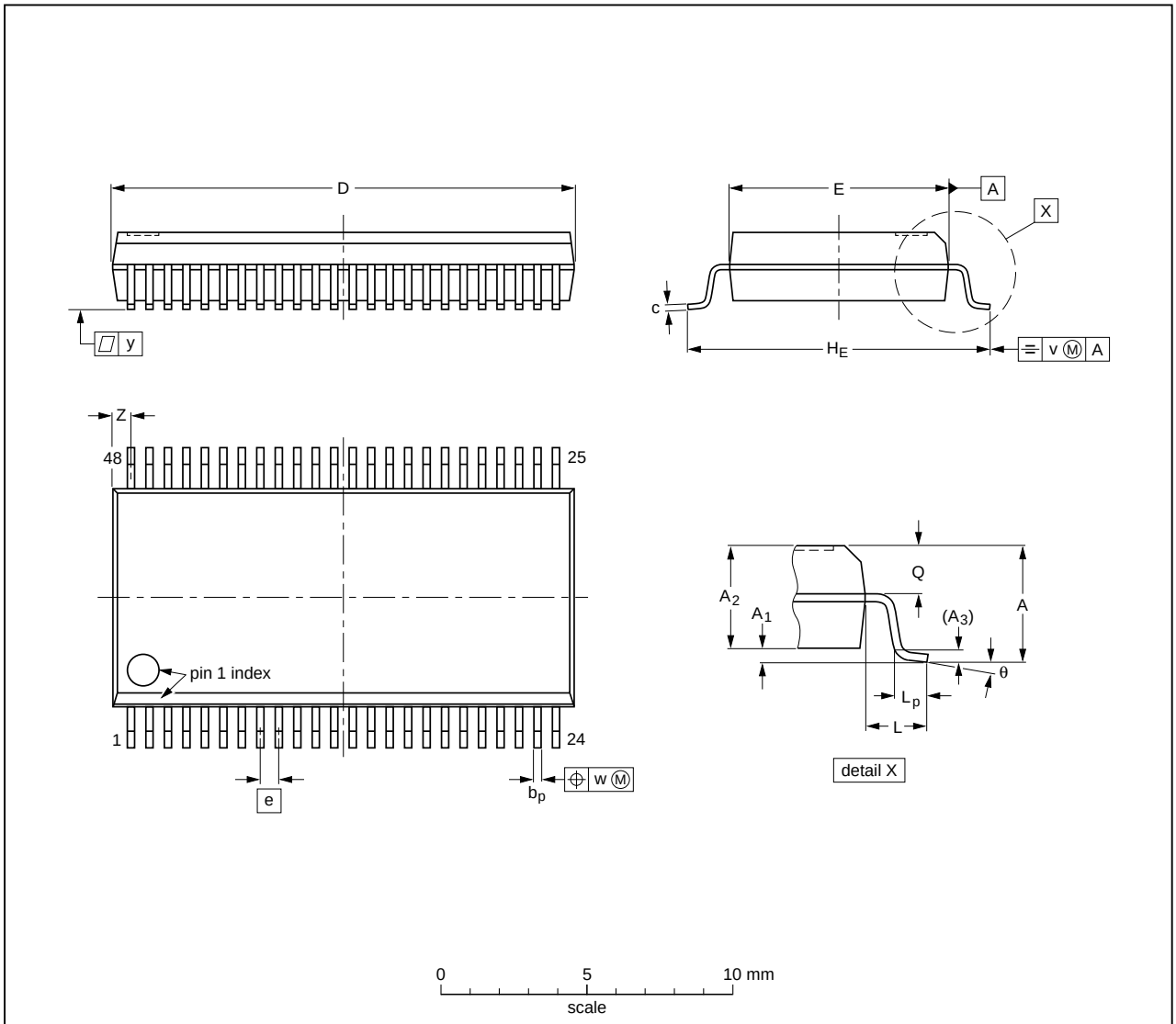
**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

## 12. Package outline

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm** **SOT370-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

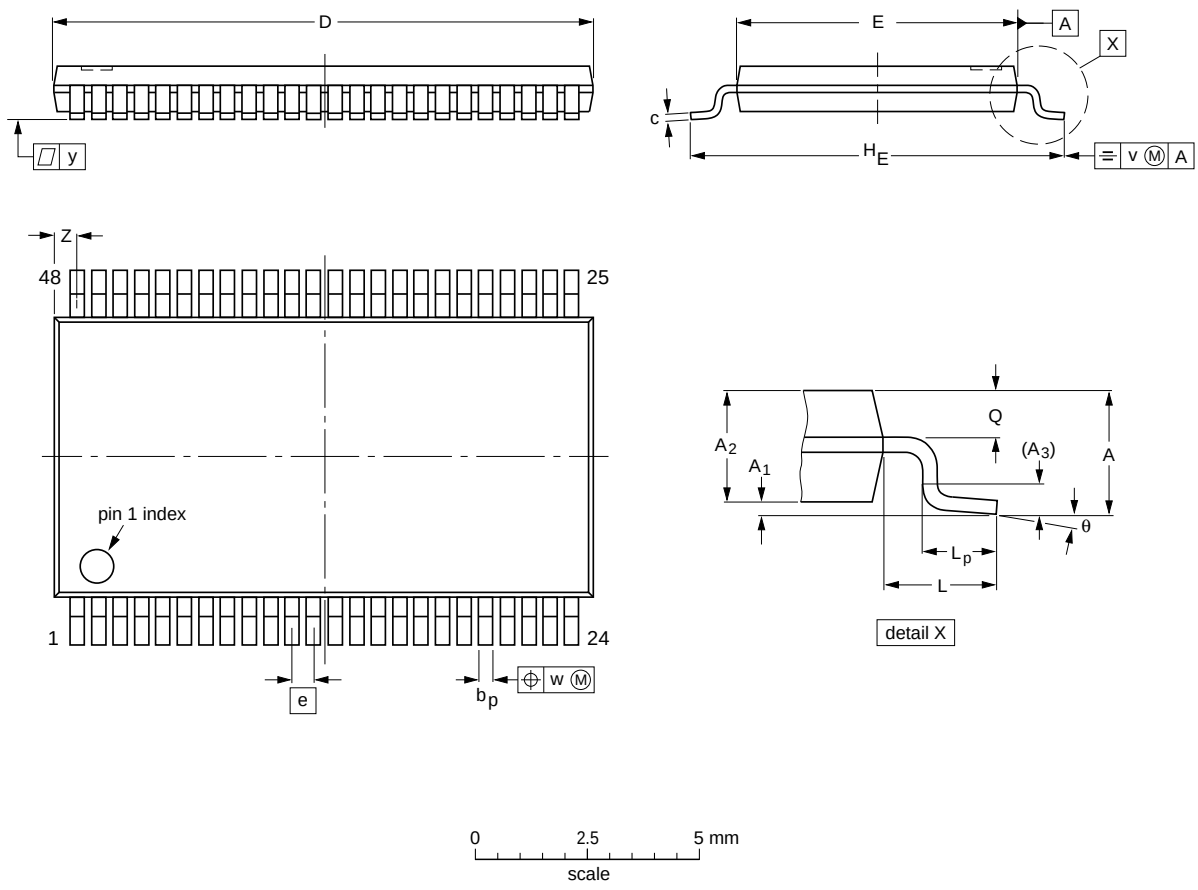
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT370-1 | | MO-118 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT370-1 (SSOP48)**

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | **0.2**<br>**0.1** | 12.6<br>12.4 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

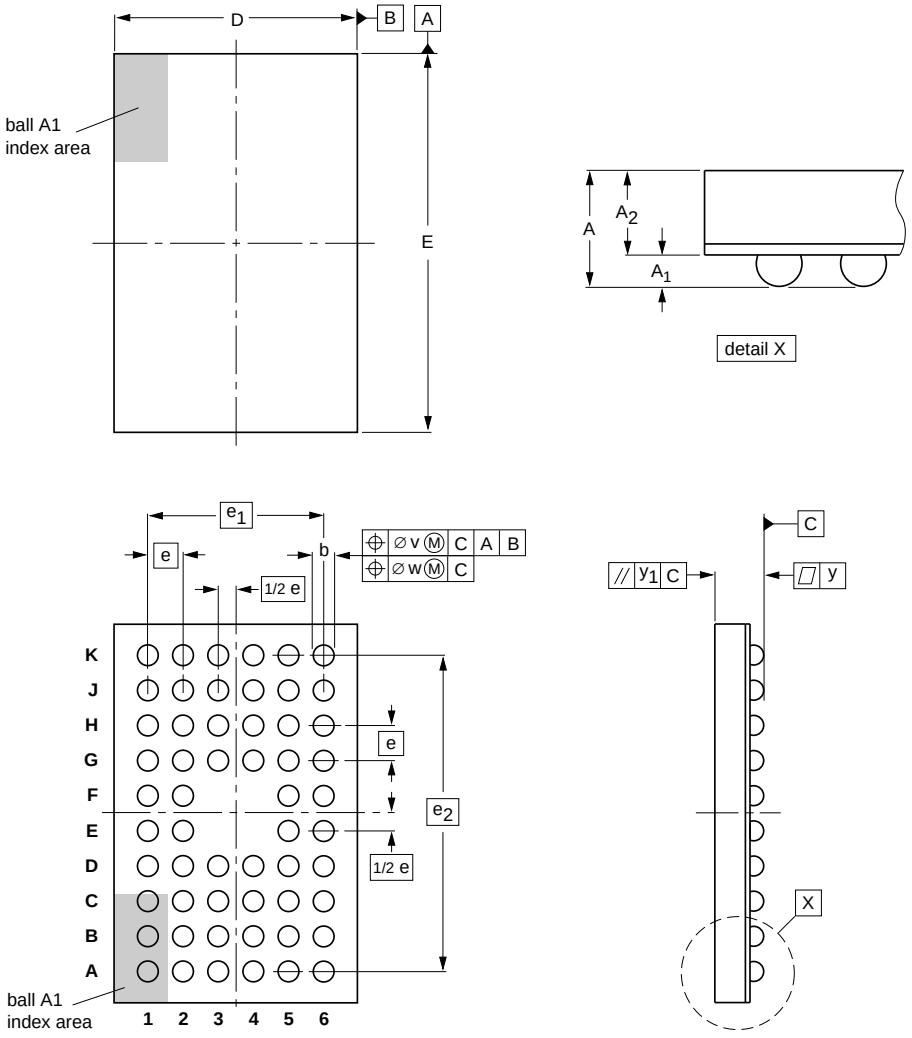
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

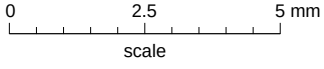
**Fig 10. Package outline SOT362-1 (TSSOP48)**

**VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm** **SOT702-1**




**DIMENSIONS (mm are the original dimensions)**

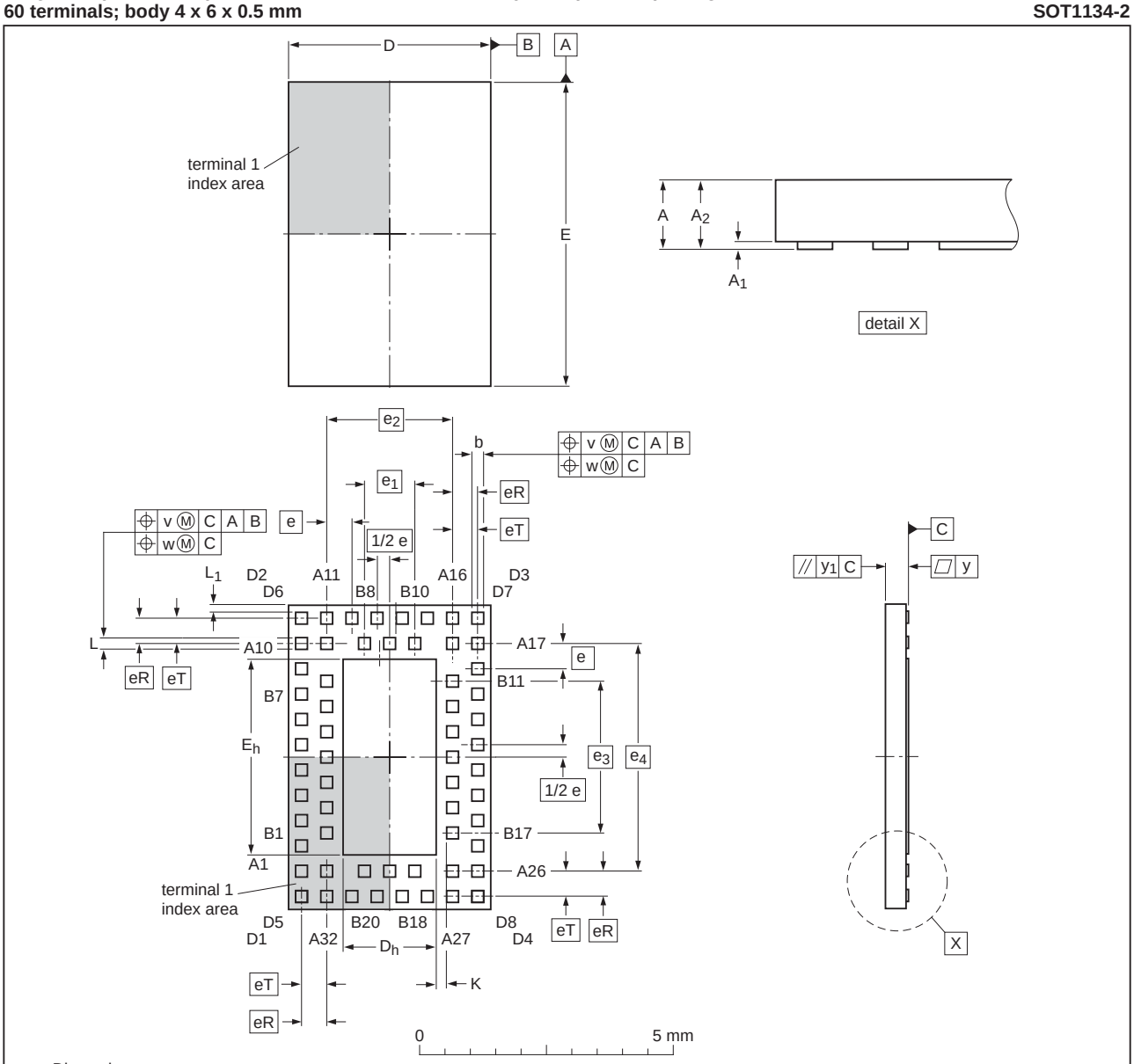
| UNIT | A max. | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.3<br>0.2 | 0.7<br>0.6 | 0.45<br>0.35 | 4.6<br>4.4 | 7.1<br>6.9 | 0.65 | 3.25 | 5.85 | 0.15 | 0.08 | 0.08 | 0.1 |




| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT702-1 | | MO-225 | | | | ~~02-08-08~~<br>03-07-01 |

**Fig 11. Package outline SOT702-1 (VFBGA56)**

**HXQFN60: plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 x 6 x 0.5 mm** **SOT1134-2**




Dimensions

| Unit | | A | $A_1$ | $A_2$ | b | D | $D_h$ | E | $E_h$ | e | $e_1$ | $e_2$ | $e_3$ | $e_4$ | eR | eT | K | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.50 | 0.08 | 0.42 | 0.28 | 4.1 | 1.95 | 6.1 | 3.95 | | | | | | | | 0.25 | 0.28 | 0.195 | | | | |
| | nom | | 0.05 | 0.40 | 0.23 | 4.0 | 1.85 | 6.0 | 3.85 | 0.5 | 1.0 | 2.5 | 3.0 | 4.5 | 0.5 | 0.49 | 0.20 | 0.23 | 0.145 | 0.1 | 0.05 | 0.08 | 0.1 |
| | min | | 0.02 | 0.38 | 0.18 | 3.9 | 1.75 | 5.9 | 3.75 | | | | | | | | 0.15 | 0.18 | 0.095 | | | | |

*sot1134-2_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1134-2 | - - - | - - - | - - - | | | 11-08-15 |

**Fig 12. Package outline SOT1134-2 (HXQFN60)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVT_LVTH16244B v.11 | 20120301 | Product data sheet | - | 74LVT_LVTH16244B v.10 |
| Modifications: | • For type number 74LVT16244BBX and 74LVTH16244BBX the sot code has changed to SOT1134-2. | | | |
| 74LVT_LVTH16244B v.10 | 20111122 | Product data sheet | - | 74LVT_LVTH16244B v.9 |
| Modifications: | • Legal pages updated. | | | |
| 74LVT_LVTH16244B v.9 | 20110620 | Product data sheet | - | 74LVT_LVTH16244B v.8 |
| 74LVT_LVTH16244B v.8 | 20100322 | Product data sheet | - | 74LVT_LVTH16244B v.7 |
| 74LVT_LVTH16244B v.7 | 20090326 | Product data sheet | - | 74LVT_LVTH16244B v.6 |
| 74LVT_LVTH16244B v.6 | 20081113 | Product data sheet | - | 74LVT_LVTH16244B v.5 |
| 74LVT_LVTH16244B v.5 | 20060321 | Product data sheet | - | 74LVT16244B v.4 |
| 74LVT16244B v.4 | 20021031 | Product specification | - | 74LVT16244B v.3 |
| 74LVT16244B v.3 | 19981007 | Product specification | - | 74LVT16244B v.2 |
| 74LVT16244B v.2 | 19980219 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 17. Contents





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