

DATA SHEET

74LVC07A

Hex buffer with open-drain outputs

Product specification
Supersedes data of 2003 Feb 25

2003 Nov 11

Hex buffer with open-drain outputs

74LVC07A

FEATURES

- 5 V tolerant inputs and outputs (open drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.65 to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74LVC07A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 to 5 V environment.

The 74LVC07A provides six non-inverting buffers.

The outputs of the 74LVC07A are open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PLZ}/t_{PZL}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	2.2	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$; notes 1 and 2	6.0	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_i = \text{GND to } V_{CC}$

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	L
H	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

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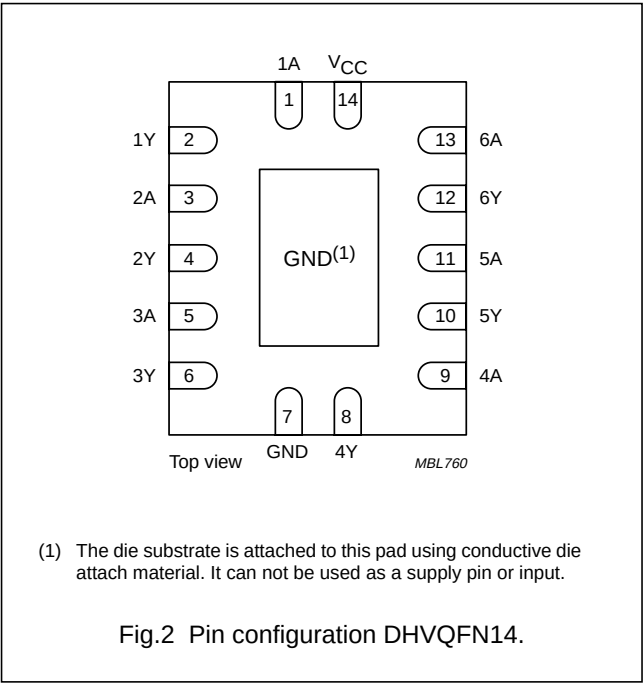
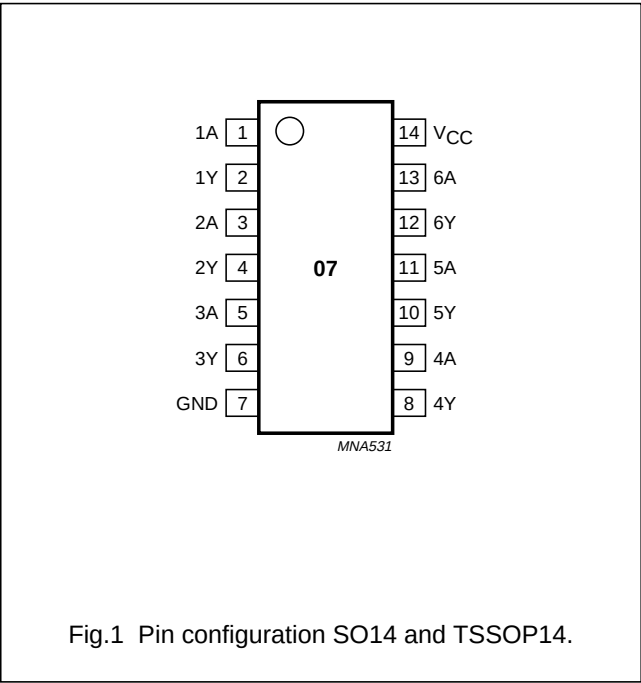
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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC07AD	−40 to +125 °C	14	SO14	plastic	SOT108-1
74LVC07APW	−40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC07ABQ	−40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V _{CC}	supply voltage



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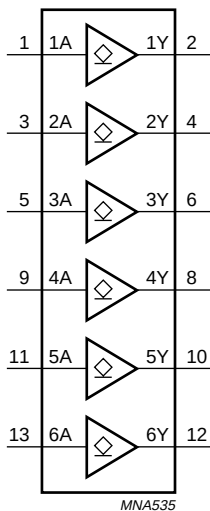


Fig.3 Logic symbol.

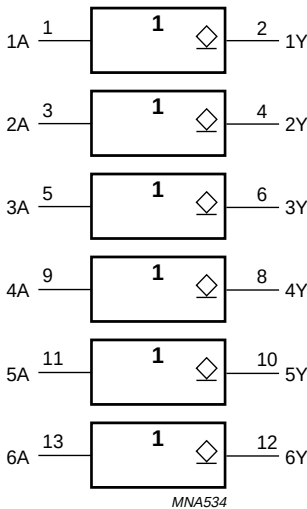


Fig.4 IEC logic symbol.

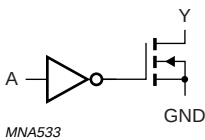


Fig.5 Logic diagram (one gate).

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	5.5	V
		high-impedance mode	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall ratios	$V_{CC} = 1.65$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	—	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output clamping diode current	$V_O < 0$	—	-50	mA
V_O	output voltage	active mode; note 1	-0.5	+6.5	V
		high-impedance mode; note 1	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ to V_{CC}	—	50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		—	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	—	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.
 For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		1.65 to 1.95	V _{CC}	−	−	V
			2.3 to 2.7	1.7	−	−	V
			2.7 to 3.6	2.0	−	−	V
			4.5 to 5.5	0.7 × V _{CC}	−	−	V
V _{IL}	LOW-level input voltage		1.65 to 1.95	−	−	GND	V
			2.3 to 2.7	−	−	0.7	V
			2.7 to 3.6	−	−	0.8	V
			4.5 to 5.5	−	−	0.30 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA I _O = 4 mA I _O = 8 mA I _O = 12 mA I _O = 24 mA I _O = 32 mA	1.65 to 5.5	−	−	0.20	V
			1.65	−	−	0.45	V
			2.3	−	−	0.3	V
			2.7	−	−	0.4	V
			3.0	−	−	0.55	V
			4.5	−	−	0.55	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	1.65 to 5.5	−	±0.1	±5	μA
I _{OZ}	output leakage current	V _I = V _{IH} ; V _O = 5.5 V or GND	1.65 to 5.5	−	0.1	±10	μA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V	0.0	−	±0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	−	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} − 0.6 V; I _O = 0	2.3 to 5.5	−	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.65 to 1.95	V _{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V _{CC}	–	–	V
V _{IL}	LOW-level input voltage		1.65 to 1.95	–	–	GND	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.30 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA I _O = 4 mA I _O = 8 mA I _O = 12 mA I _O = 24 mA I _O = 32 mA	1.65 to 5.5	–	–	0.20	V
			1.65	–	–	0.45	V
			2.3	–	–	0.3	V
			2.7	–	–	0.4	V
			3.0	–	–	0.55	V
			4.5	–	–	0.55	V
			I _{LI}	input leakage current	V _I = 5.5 V or GND	1.65 to 5.5	–
I _{OZ}	output leakage current	V _I = V _{IH} ; V _O = 5.5 V or GND	1.65 to 5.5	–	–	±10	μA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V	0.0	–	–	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 0.6 V; I _O = 0	2.3 to 5.5	–	–	500	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2$ ns for $V_{CC} \leq 2.7$ V and $t_r = t_f \leq 2.5$ ns for $V_{CC} \geq 2.7$ V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = −40 to +85 °C; note 1							
t _{PLZ} /t _{PZL}	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	–	2.5	–	ns
			2.3 to 2.7	0.5	1.6	2.8	ns
			2.7	0.5	2.4	3.3	ns
			3.0 to 3.6	0.5	2.2	3.6	ns
			4.5 to 5.5	0.5	1.6	2.6	ns
T _{amb} = −40 to +125 °C							
t _{PLZ} /t _{PZL}	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	–	–	–	ns
			2.3 to 2.7	0.5	–	3.5	ns
			2.7	0.5	–	4.5	ns
			3.0 to 3.6	0.5	–	4.5	ns
			4.5 to 5.5	0.5	–	3.5	ns

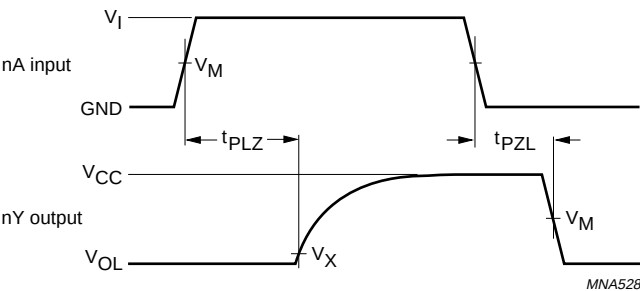
Note

1. All typical values are measured at $T_{amb} = 25$ °C and at $V_{CC} = 1.8, 2.5, 2.7, 3.3$ and 5.0 V, respectively.

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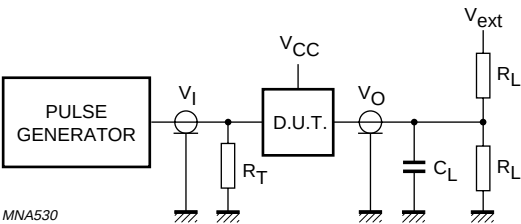
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AC WAVEFORMS



V_{CC}	V_M	V_X
$<2.7\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$
$\geq 2.7\text{ to }3.6\text{ V}$	1.5 V	$V_{OL} + 0.3\text{ V}$
$\geq 4.5\text{ to }5.5\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$

Fig.6 The input nA to output nY propagation delays.



V_{CC}	V_{ext}	V_I	C_L	R_L
$1.65\text{ to }1.95\text{ V}$	$2 \times V_{CC}$	V_{CC}	30 pF	$1\text{ k}\Omega$
$2.3\text{ to }2.7\text{ V}$	$2 \times V_{CC}$	V_{CC}	30 pF	$500\text{ }\Omega$
2.7 V	6 V	2.7 V	50 pF	$500\text{ }\Omega$
$3.0\text{ to }3.6\text{ V}$	6 V	2.7 V	50 pF	$500\text{ }\Omega$
$4.5\text{ to }5.5\text{ V}$	$2 \times V_{CC}$	V_{CC}	50 pF	$500\text{ }\Omega$

Definitions for test circuits:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

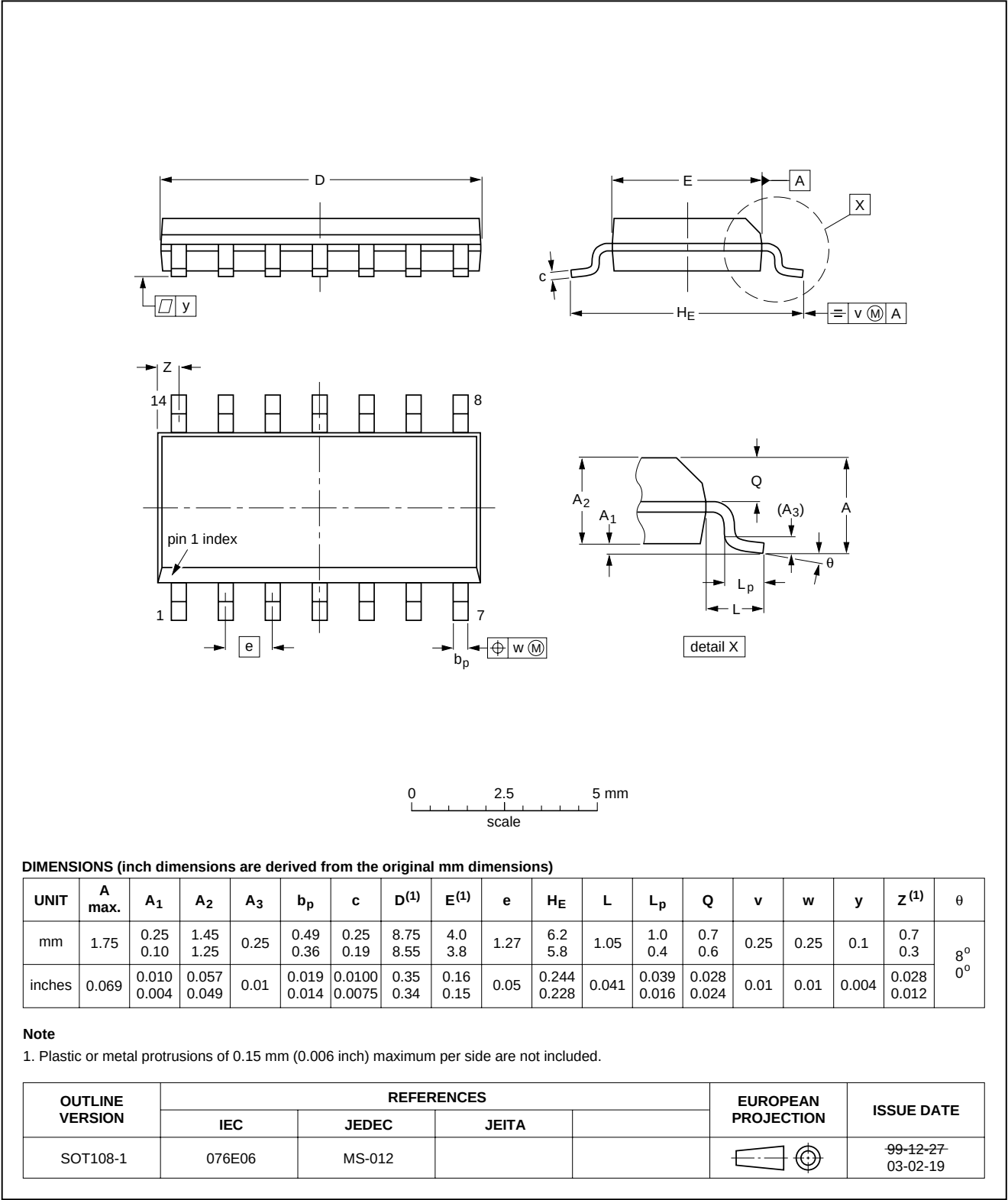
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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

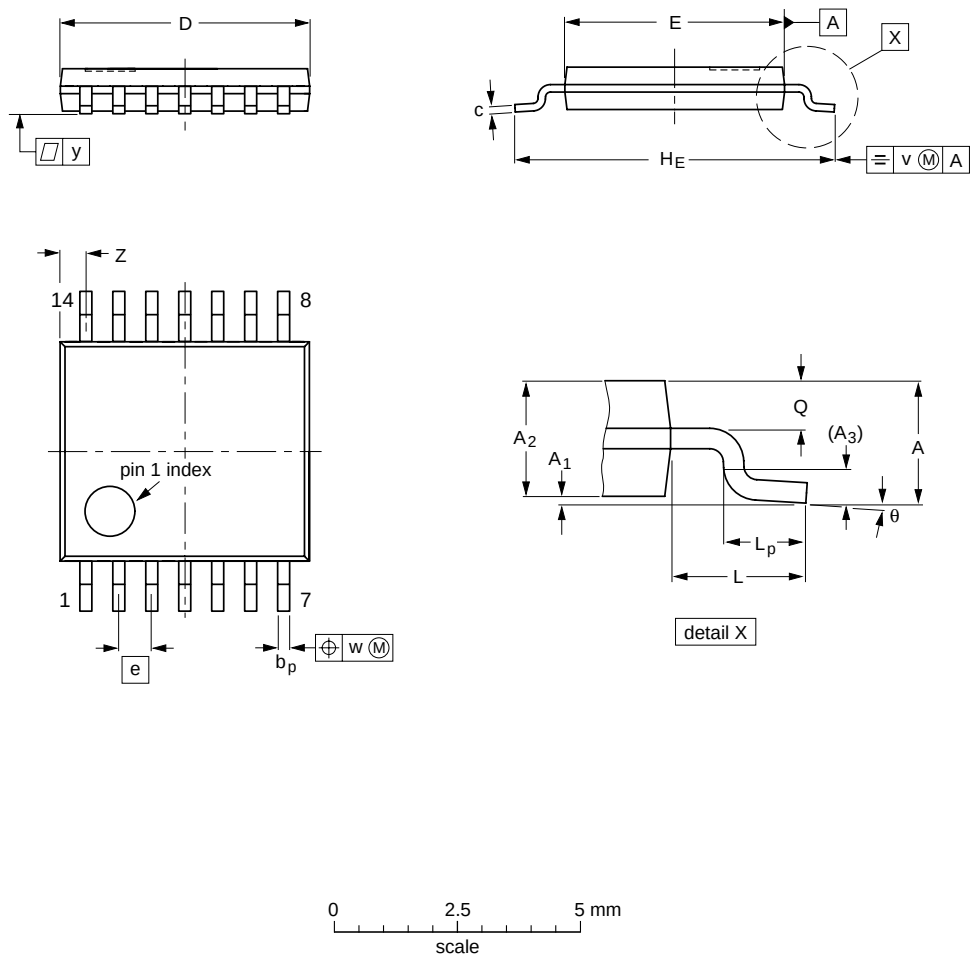


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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

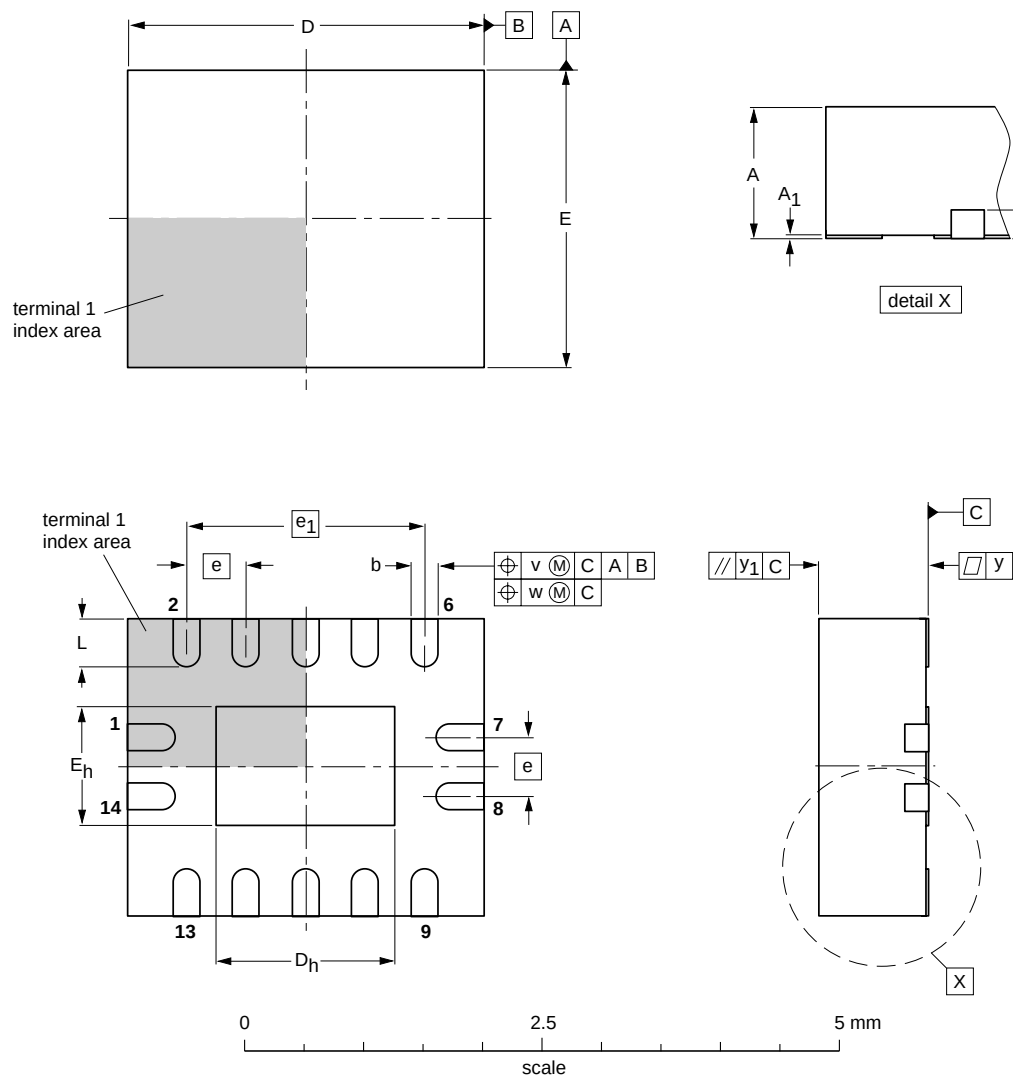
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

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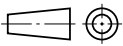
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

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LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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