

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC164AP, TC74HC164AF

8-Bit Shift Register (S-IN, P-OUT)

The TC74HC164A is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

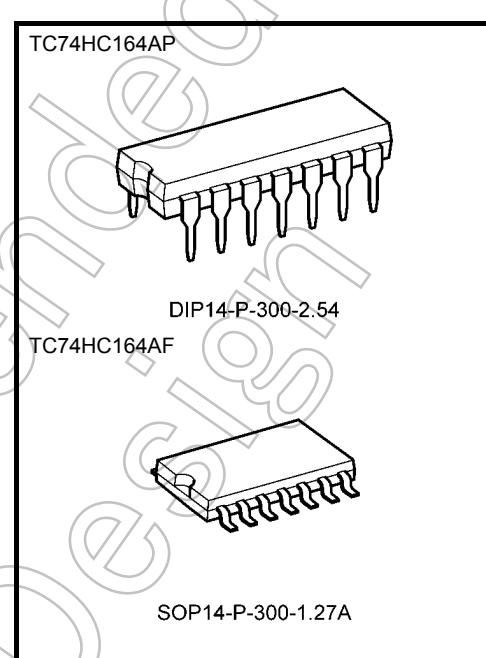
It consists of a serial-in, parallel-out 8-bit shift register with a CK input and an overriding $\overline{\text{CLR}}$ input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

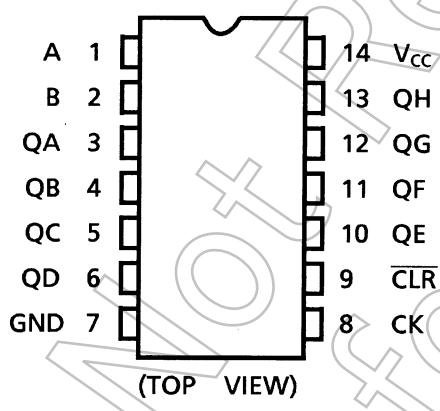
Features

- High speed: $f_{\text{max}} = 58 \text{ MHz}$ (typ.) at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (min)
- Outputs drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$ (min)
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS164



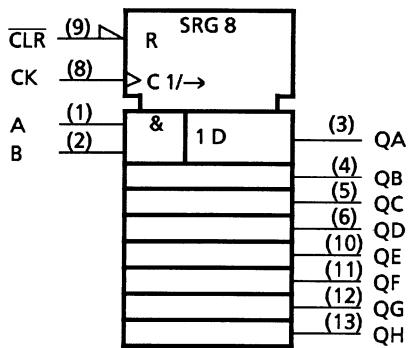
Weight
 DIP14-P-300-2.54 : 0.96 g (typ.)
 SOP14-P-300-1.27A : 0.18 g (typ.)

Pin Assignment



Start of commercial production
 1986-11

IEC Logic Symbol



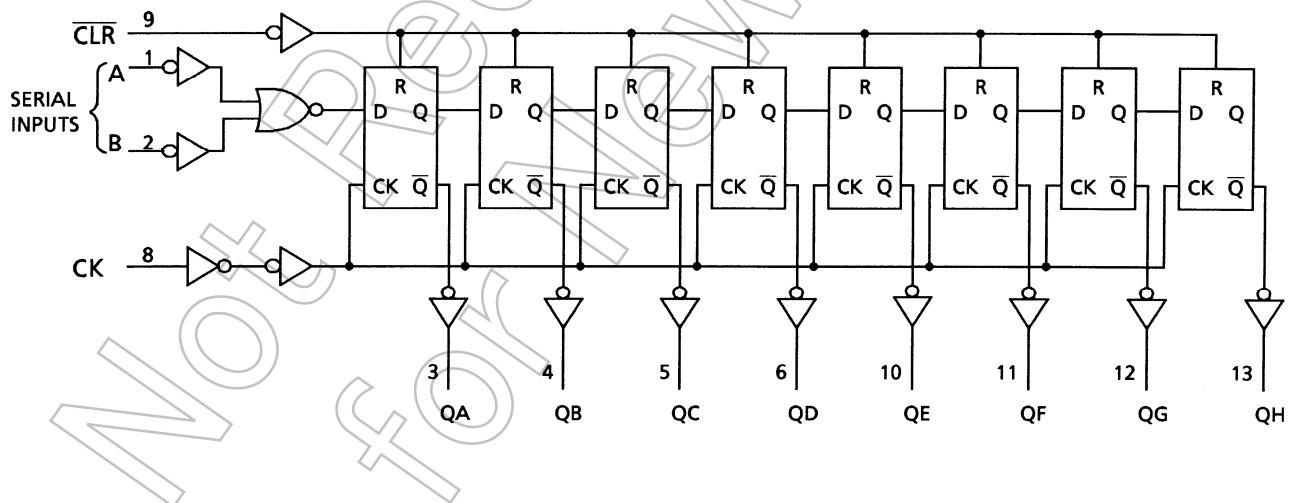
Truth Table

Inputs			Outputs				
\overline{CLR}	CK	Serial IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H	↓	X	X	No Change			
H	↑	L	X	L	QA_n	...	QG_n
H	↑	X	L	L	QA_n	...	QG_n
H	↑	H	H	H	QA_n	...	QG_n

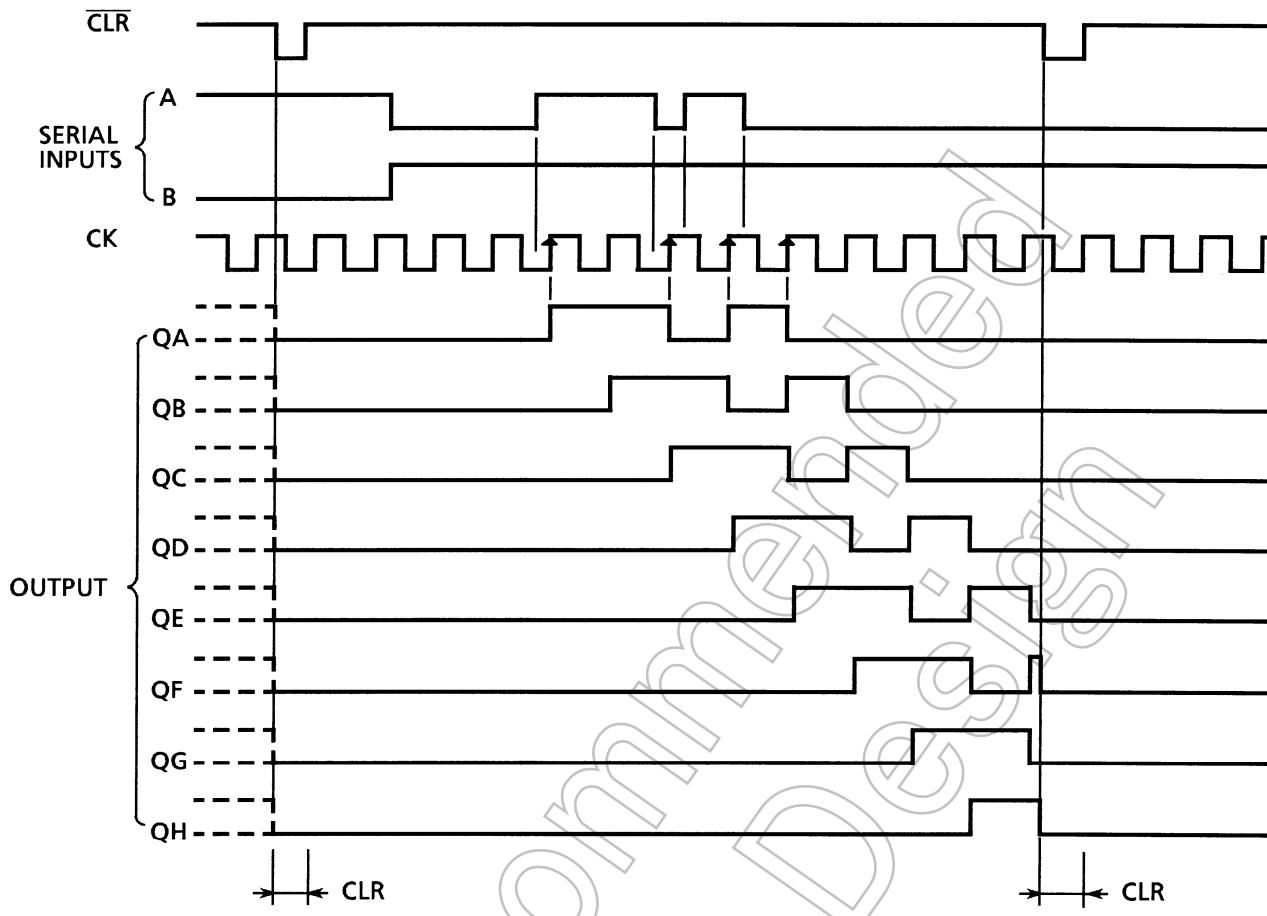
X: Don't care

 $QA_n \sim QG_n$: The level of $QA \sim QG$, respectively, before the most recent positive edge of clock.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10 \text{ mW}/^\circ\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = +40 to 85°C		Unit	
			V_{CC} (V)	Min	Typ.	Max	Min		
High-level input voltage	V_{IH}	—	2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu A$	2.0	1.9	2.0	—	1.9	V
			$I_{OH} = -4 mA$	4.5	4.4	4.5	—	4.4	
			$I_{OH} = -5.2 mA$	6.0	5.9	6.0	—	5.9	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu A$	2.0	—	0.0	0.1	—	V
			$I_{OL} = 4 mA$	4.5	—	0.0	0.1	—	
			$I_{OL} = 5.2 mA$	6.0	—	0.0	0.1	—	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ.	Limit	
Minimum pulse width (CK)	t_W (L) t_W (H)	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum pulse width (\overline{CLR})	t_W (L)	—	2.0	—	80	ns
			4.5	—	16	
			6.0	—	14	
Minimum set-up time (A, B)	t_s	—	2.0	—	50	ns
			4.5	—	10	
			6.0	—	9	
Minimum hold time (A, B)	t_h	—	2.0	—	5	ns
			4.5	—	5	
			6.0	—	5	
Minimum removal time (\overline{CLR})	t_{rem}	—	2.0	—	5	ns
			4.5	—	5	
			6.0	—	5	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	—	31	
			6.0	—	36	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (CK-Qn)	t_{pLH} t_{pHL}	—	—	15	27	ns
Propagation delay time (\overline{CLR} -Qn)	t_{pHL}	—	—	16	30	ns
Maximum clock frequency	f _{max}	—	33	58	—	MHz

AC Characteristics ($C_L = 50 \text{ pF}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	25	75	—	95
			4.5	—	7	15	—	19
			6.0	—	6	13	—	16
Propagation delay time (CK-Qn)	t_{pLH} t_{pHL}	—	2.0	—	57	160	—	200
			4.5	—	19	32	—	40
			6.0	—	16	27	—	34
Propagation delay time (\overline{CLR} -Qn)	t_{pHL}	—	2.0	—	60	175	—	220
			4.5	—	20	35	—	44
			6.0	—	17	30	—	37
Maximum clock frequency	f_{max}	—	2.0	6	18	—	5	—
			4.5	31	53	—	25	—
			6.0	36	62	—	29	—
Input capacitance	C _{IN}	—	—	—	5	10	—	10
Power dissipation capacitance	C _{PD} (Note)	—	—	—	107	—	—	—

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

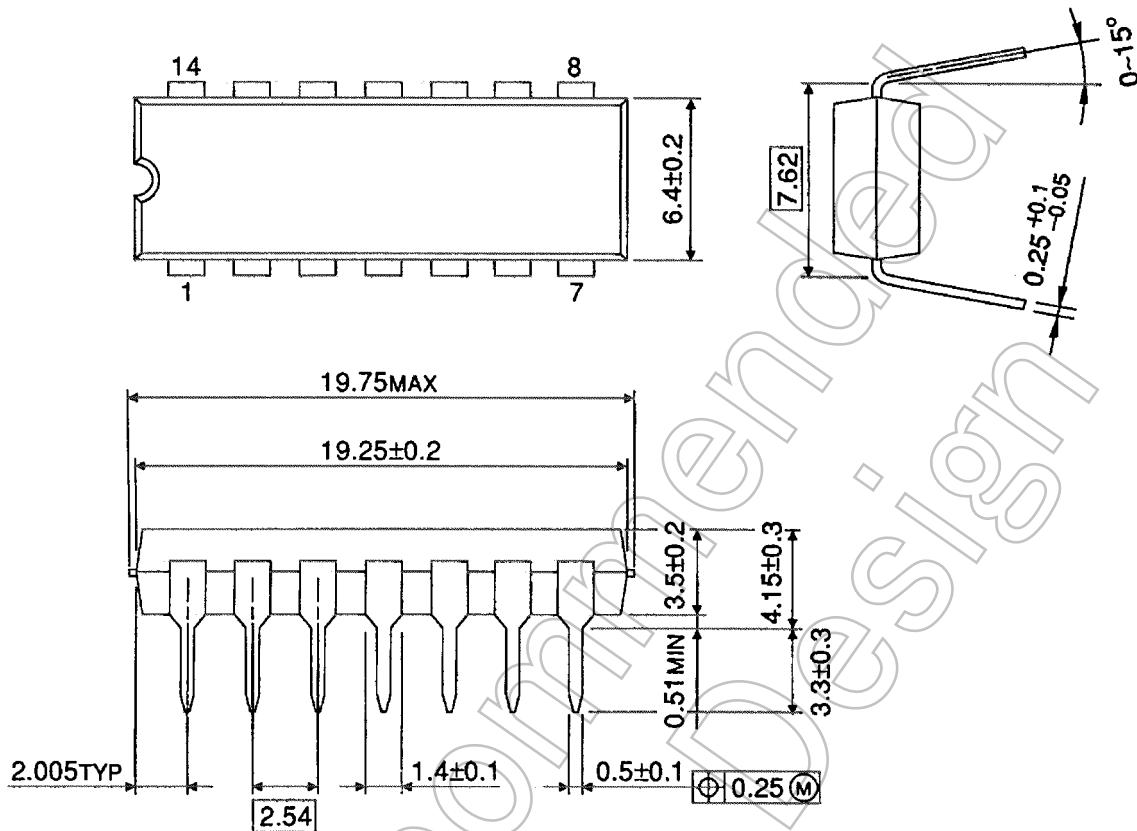
Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm

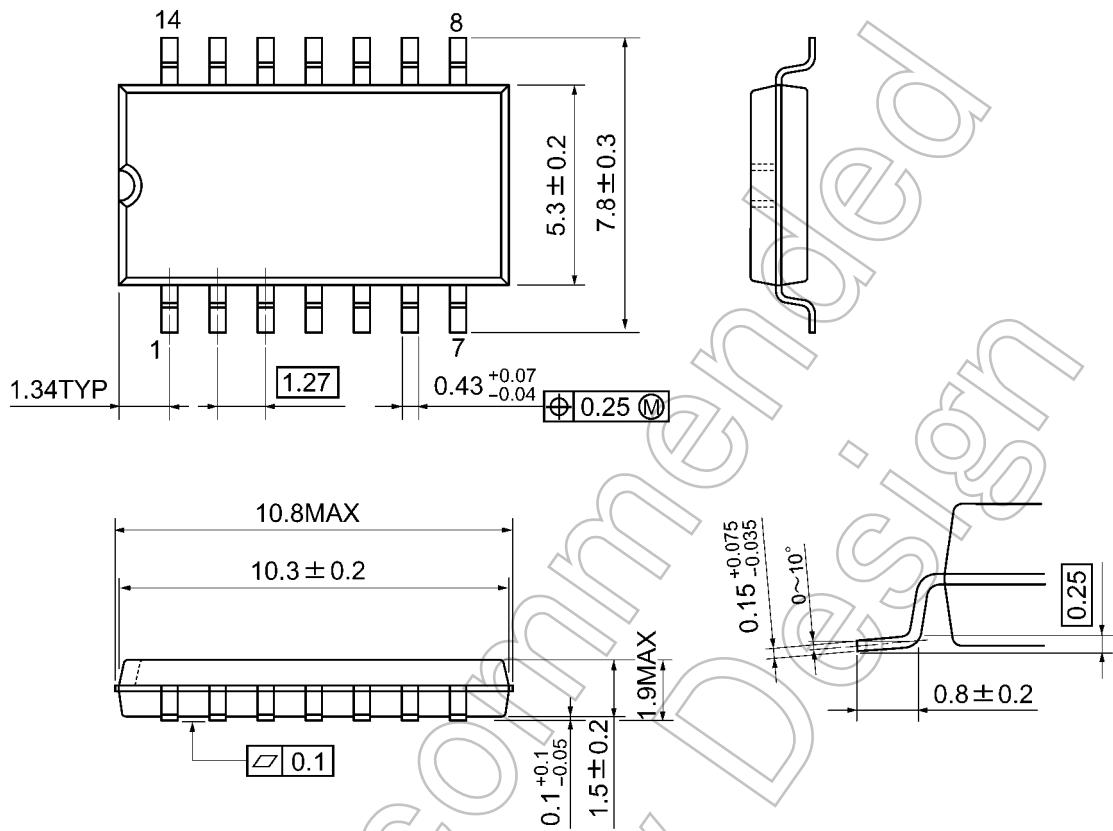


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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