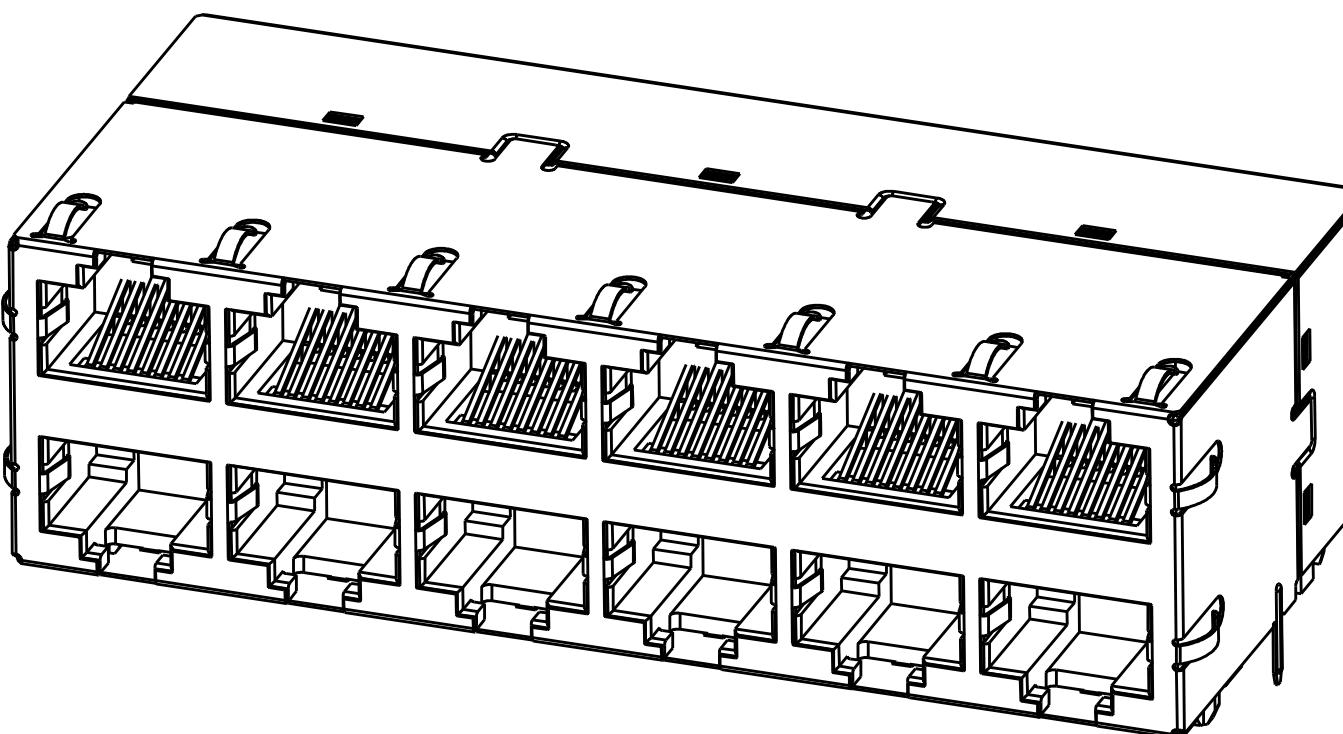


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PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:  
5736910 5939955 6425781 6428361 6554638 6840817 7123117  
7429195 7717749 7808751 6217391 6149050 7924130

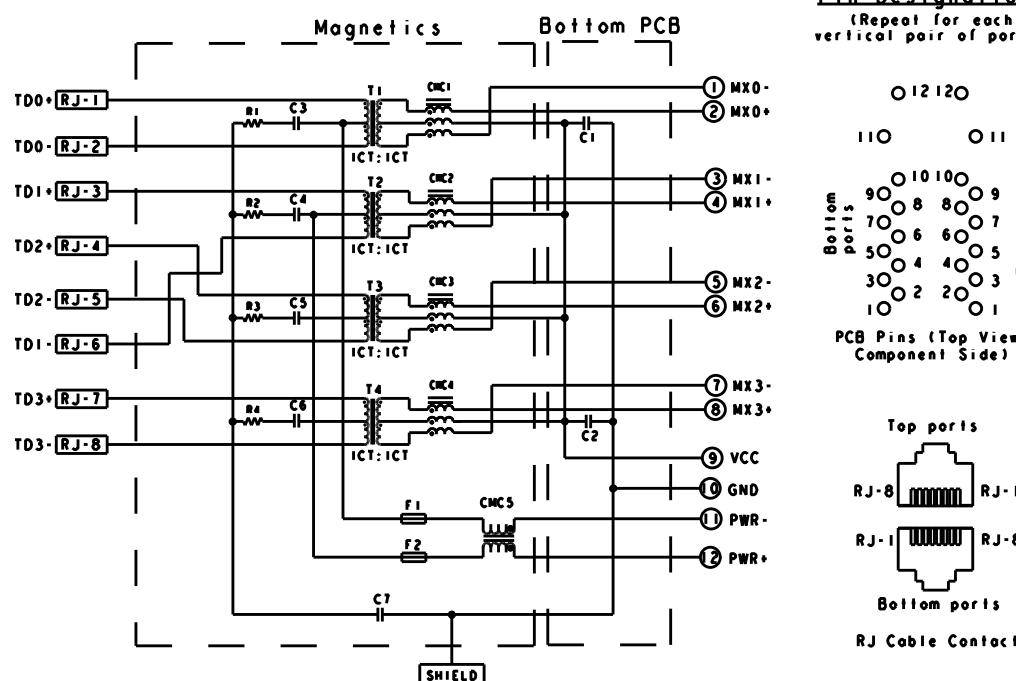
REVISIONS		DATE	REV
P	LTR	DESCRIPTION	DATE DWN APVD

D D EC-1411035 COMPANY LOGO CHANGE 26JAN2015 CZ TY



### S9HG63 GIGABIT PoE PLUS CIRCUIT

Top and Bottom Ports



C1-C2=10nF, 50V, X7R, CAPACITORS  
C3-C6=22nF, 100V, CAPACITORS  
C7=1000PF, 3KV, CAPACITOR  
R1-R4=750hms, 1/16W, RESISTORS  
F1-F2=63V, 1.5A, FUSES

**1. MATERIALS:**  
PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0  
SHIELD: BRASS, PREPLATED WITH 0.76μm MIN SEMI-BRIGHT NICKEL.  
POST DIPPED WITH 2.54μm MIN SAC SOLDER ON SOLDER TAILS.  
CONTACTS: PHOSPHOR BRONZE, 1.27μm MIN OVERALL NICKEL  
UNDERPLATE WITH SELECT 1.27μm MIN GOLD AT MATING INTERFACE  
AND 2.54μm MIN MATTE TIN ON SOLDER TAILS.  
ALL PC BOARDS: HIGH TEMPERATURE PCB, TG>170°C

**△ MAGNETICS**  
APPLICATION: 10/100/1000 BASE-T, PoE PLUS  
IMPEDANCE: 100 OHMS  
TURNS RATIO (CHIP:CABLE): 1:1 ALL FOUR PAIRS  
OPEN CIRCUIT INDUCTANCE (OCL): ALL CHANNELS 350uH MIN @100kHz,  
0.1VRMS WITH 8mA DC BIAS FROM 0°C TO 70°C, 200uH MIN @100kHz,  
0.1VRMS WITH 19mA DC BIAS FROM 0°C TO 70°C, ACROSS RJ1-RJ2 & RJ3-RJ6  
ALL FOUR PAIRS BI-DIRECTIONAL  
POE CURRENT: 600mA DC MAX  
PERFORMANCE @ 25°C:  
INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz  
RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 40MHz  
12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz  
CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz  
33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz  
COMMON MODE REJECTION RATIO (CMRR): 30dB MIN FROM 0.5MHz TO 100MHz  
ISOLATION VOLTAGE: 2250VDC(MAX) FOR 60 SECONDS WITH A RISE TIME OF  
500V/SEC AND WITH ALL PORTS CONNECTED.

**△ PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN ARE LOCATED IN APPROXIMATE AREA SHOWN. DATE CODE "YY" IS YEAR, "WW" IS WORK WEEK, "D" IS DAY OF WEEK, WITH SUNDAY=1**

**△ TRP LOGO AND AGENCY APPROVAL LOGO ARE LOCATED IN APPROXIMATE AREA SHOWN.**

**5. OPERATING TEMP: FROM 0°C TO +70°C.**

**6. RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.**

**△ INDICATED MAGNETIC CONNECTIONS ARE SYMMETRICAL AND SUPPORT AUTO-MDI/MDIX.**

**△ DATUM AND BASIC DIMENSION ESTABLISHED BY CUSTOMER.**

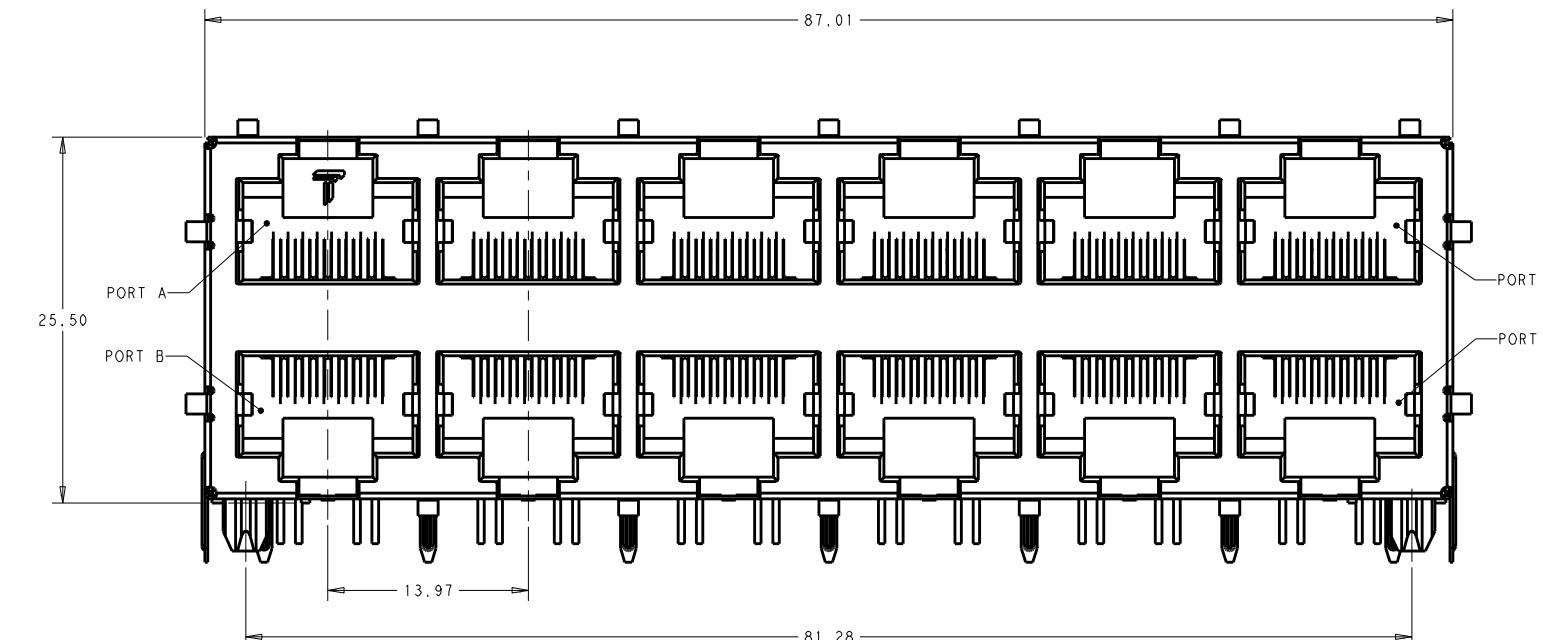
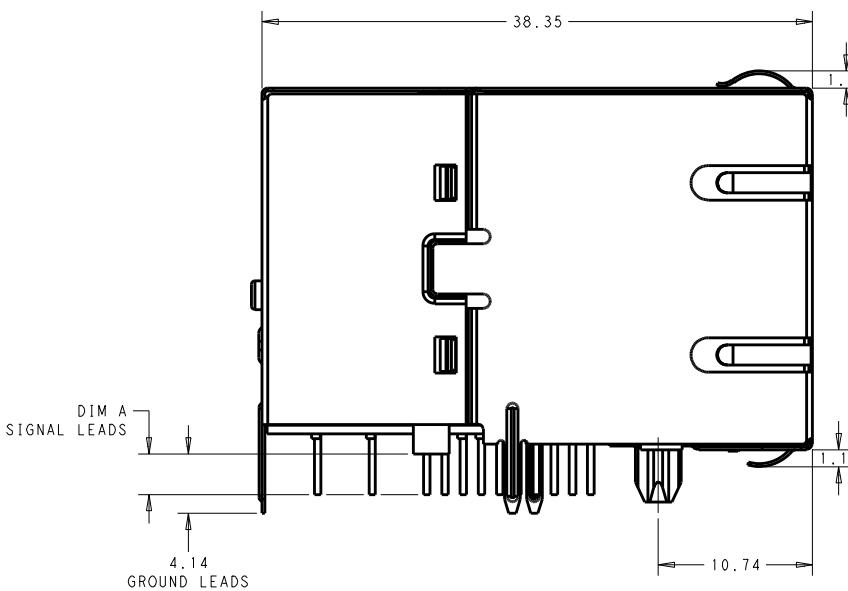
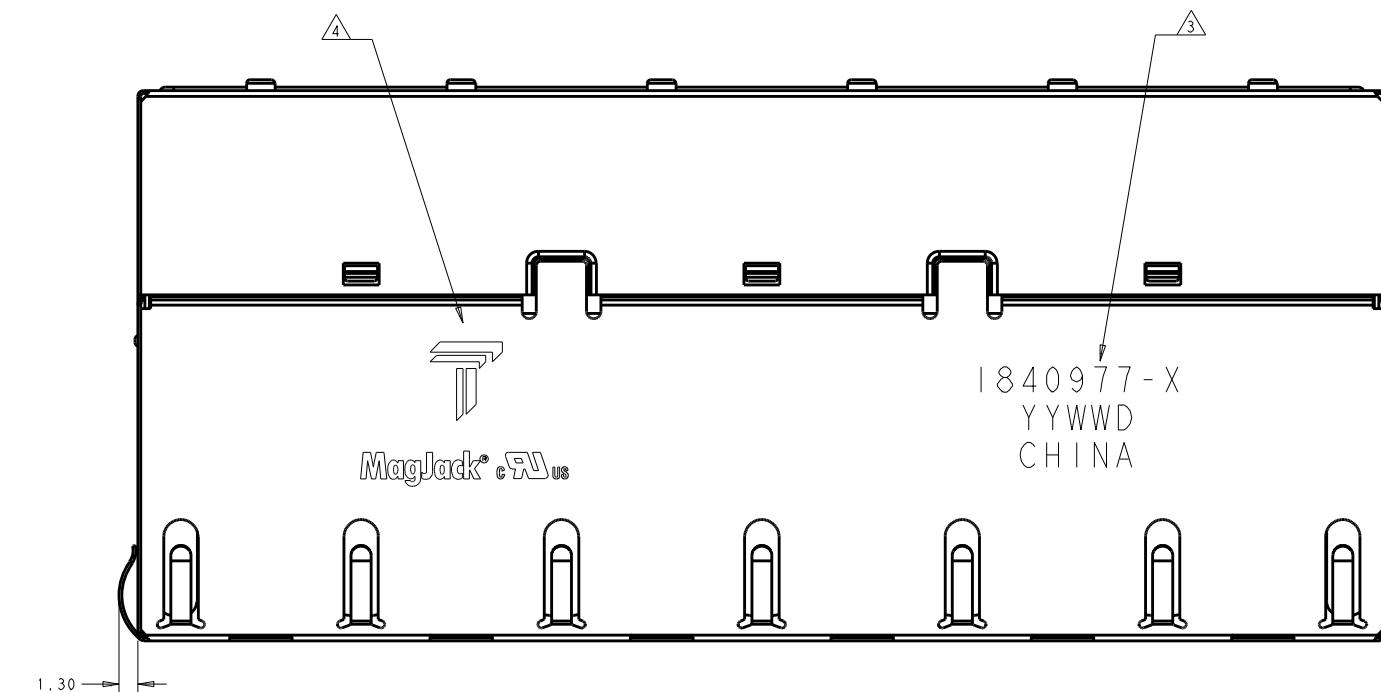
**△ BASIC DIMENSION ESTABLISHED BY CUSTOMER, BUT MAY NOT BE GREATER THAN 5.08mm.**

**10. THE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS, PEAK TEMPERATURE 260°C MAX, 10 SECONDS MAX.**

THIS DRAWING IS A CONTROLLED DOCUMENT.	DW	TONY YUAN	11JUN2010	2.29	1840977-2
DIMENSIONS:	1. TOLERANCES UNLESS OTHERWISE SPECIFIED:	2. PLC	3. PLC	4. PLC	5. APVD
mm		±0.1	±0.25	±0.25	APVD
					LEI THI THU
					11JUN2010
					MODEL NAME
					MAG JACK
					STACK PoE+
					DESC 2X6 S9HG63 GIGABIT PoE+ W/O LED
PRODUCT SPEC	APPLICATION SPEC	SIZE	CAGE CODE	DRAWING NO	RESTRICTED TO
108-104004	-	A1	C-1840977	-	
		CUSTOMER DRAWING	SCALE	NTS	SHEET 1 OF 3 REV D

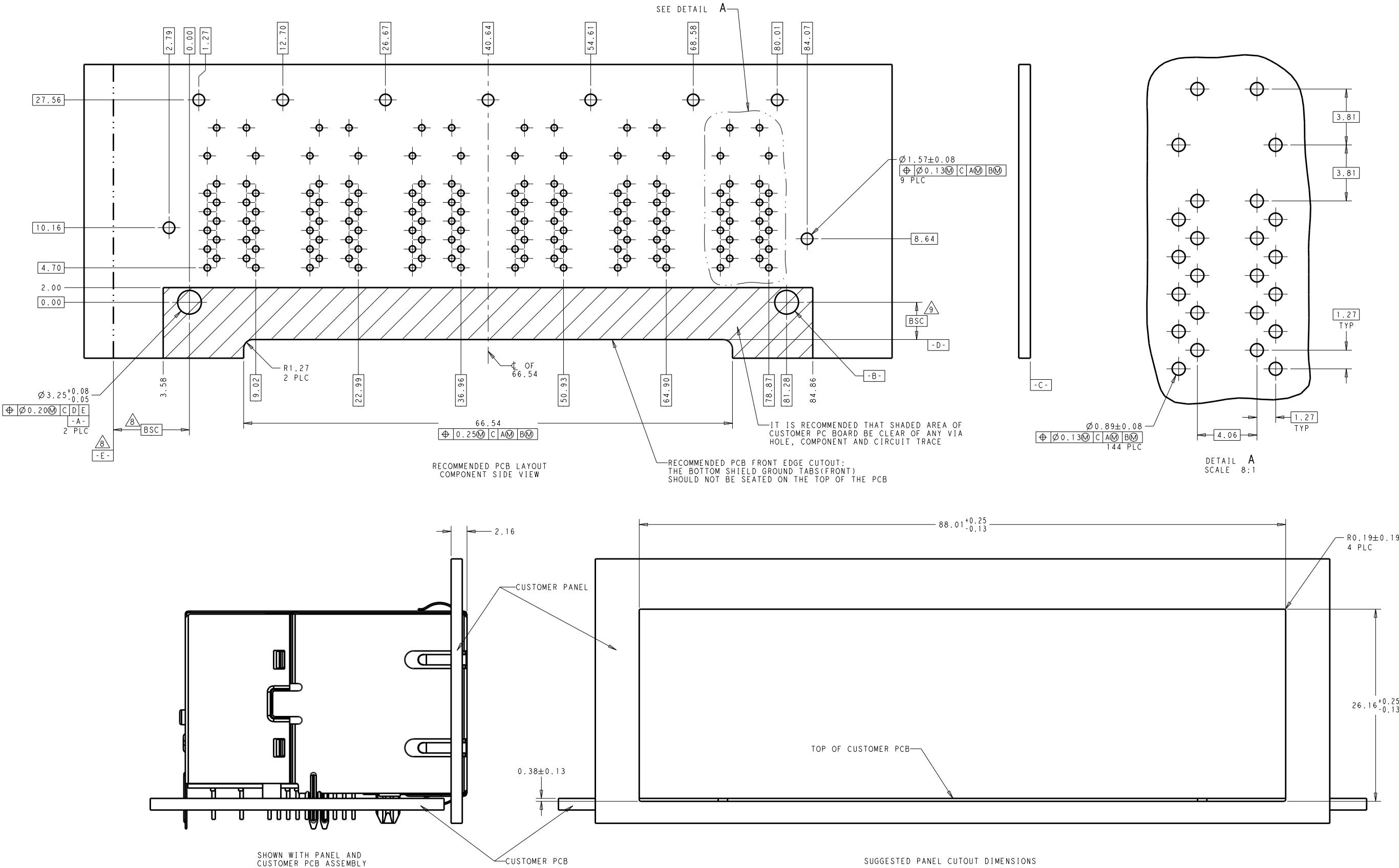
**trp** CONNECTOR  
a bel group

DONGGUAN CHINA



THIS DRAWING IS A CONTROLLED DOCUMENT		DN: TOMMY REN 11JUN2010	DN: CHEN YUAN 11JUN2010	trp CONNECTOR	DONGGUAN CHINA
DIMENSIONS:		TOLERANCES UNLESS OTHERWISE SPECIFIED:			
mm		1 PLC ±0.05			
		2 PLC ±0.25			
		3 PLC ±0.25			
		4 PLC ±0.05			
		ANGLES ±0.5°			
PRODUCT SPEC		APPLICATION SPEC			
108-104004		-			
CUSTOMER DRAWING		SIZE: A1	CAGE CODE: DRAWING NO: C=1840977	RESTRICTED TO: -	SCALE: NTS SHEET 2 OF 3 REV: D

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DIMENSIONS: TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD: 11JUN2010	REFLTH: THU		
mm		MODEL NAME: MAGJACK STACK PoE+		DESC: 2X6 S9HG63 GIGABIT PoE+ W/O LED	
		SIZE: A1		CAGE CODE: C=1840977	RESTRICTED TO: -
PRODUCT SPEC: 108-104004		APPLICATION SPEC: -		SCALE: NTS SHEET 3 OF 3 REV: D	
CUSTOMER DRAWING					