Micropower Voltage Reference with Comparator

ISL21440

The ISL21440 is a micropower, FGA™ reference and comparator on a single chip. Drawing less than 1.8µA supply current over the full operating temperature range, the ISL21440 operates from a single 2V to 11V supply and can also be used with split bipolar supplies.

The ISL21440's on-board reference provides a 1.182V ±0.5% output. It features programmable hysteresis and TTL/CMOS compatible outputs that sink and source current. Low Bias currents permit high value divider resistors for typical circuit current drains of <2.5µA.

The low supply current makes the ISL21440 ideal for battery powered devices in battery level or low voltage monitors circuits.

The ISL21440 is a pin-compatible, performance upgrade of both the LTC1440, LTC1540, MAX921 and MAX931.

Features

- 1.8µA Supply Current Over Full Temperature Range
- Wide Supply Range . . . . . 2V to 11V
- Precision 1.182V ±0.5% Voltage Reference
- Comparator with User Programmable Hysteresis
- Temperature Range . . . . . -40°C to +125°C
- 8 Ld MSOP and 8 Ld TDFN Packages
- Pin Compatible Upgrade to MAX921 and LTC1440

Applications

- Low Battery Detector
- Low Voltage Reset
- Overvoltage Monitor
- Window Comparator

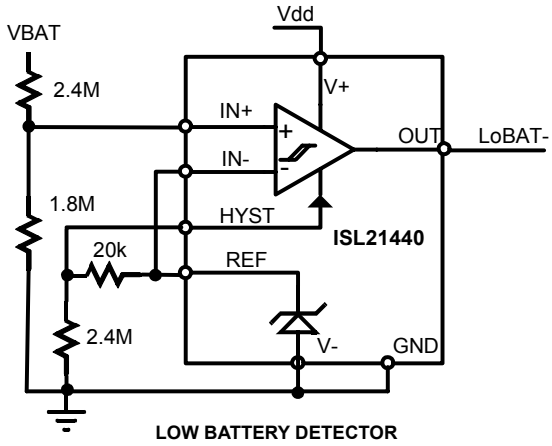


FIGURE 1. TYPICAL APPLICATION

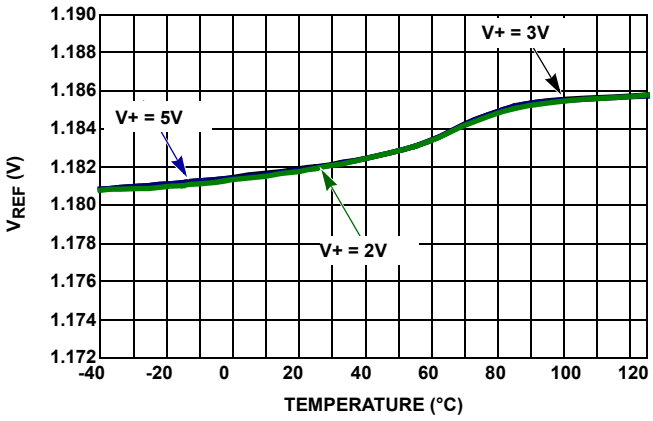
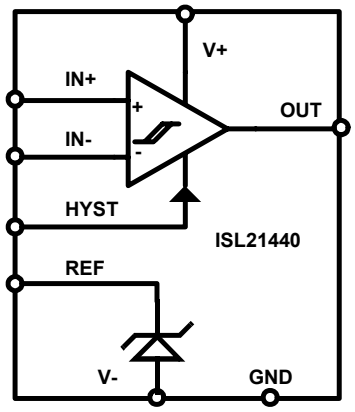


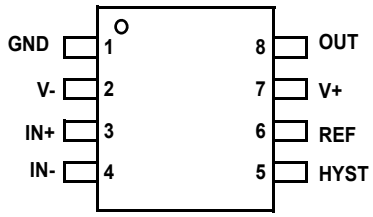
FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

Block Diagram



Pin Configuration

ISL21440
(8 LD MSOP, 8 LD TDFN)
TOP VIEW



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	GND	Ground pin. Sets the Comparator output low level.
2	V-	Negative Supply Input for Voltage Reference and Comparator.
3	IN+	Comparator non-inverting input pin. Range: V- to V+ -1.5V.
4	IN-	Comparator inverting input pin. Range: V- to V+ -1.5V
5	HYST	Comparator Hysteresis input. Accepts a voltage divided from the Reference output. Range is VREF - 50mV to VREF. Connect directly to VREF for zero hysteresis.
6	REF	Reference output. Source 2mA and Sink 10µA.
7	V+	Positive Supply Input for Comparator and Reference. Range is 2.0V to 11.0V
8	OUT	Comparator output, CMOS push-pull. Output swing referenced to V+ and GND.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL21440IUZ	1440Z	2 to 11	-40 to +125	8 Ld MSOP	M8.118
ISL21440IRTZ	1440	2 to 11	-40 to +125	8 Ld TDFN	L8.3x3G

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL21440. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

Supply Voltage Range, V+ to GND . . . . . -0.5V to +12V
IN+, IN- with Respect to V- . . . . . -0.3V to (V+) +0.3V
GND with Respect to V- . . . . . 6.0V to -0.3V
V+ with Respect to V- . . . . . 12V to -0.3V
REF, HYST with Respect to V- . . . . . -0.3V to 1.5V
Out with Respect to GND . . . . . (V+) +0.3V to -0.3V
Voltage on All Other Pins . . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
  Human Body Model 4000V
  Machine Model 350V
  Charged Device Model 2000V
Latch Up (Tested Per JESD-78B; Class 1, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP Package (Notes 5, 7)	154	55
8 Ld TDFN Package (Notes 5, 6)	68	8

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile (Note 8) . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
Supply Voltage . . . . . 2.7V to 5.5V

Environmental Operating Conditions

X-Ray Exposure (Note 4) 10mRem

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Measured with no filtering, distance of 10" from source, intensity set to 55kV and 70mA current, 30s duration. Other exposure levels should be analyzed for Output Voltage drift effects. See "Applications Information" on page 11.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.
8. Post-reflow drift for the ISL21440 device voltage reference output will range from 100mV to 1.0mV based on experimental results with devices on FR4 double sided boards. The design engineer must take this into account when considering the reference voltage after assembly.

Analog Specifications

V+= +5.0V. V- = GND = 0V unless otherwise specified, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNITS
POWER SUPPLY							
V_+	Supply Voltage Range	V- = GND		**2.0**		**11.0**	V
I_{CC}	Supply Current	IN+ = IN- +80mV, HYST = REF			0.46	0.75	µA
						0.85	µA
COMPARATOR							
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V	MSOP Package			±3	mV
						±3.25	mV
			TDFN Package			±3.6	mV
						±3.75	mV
I_{IN}	Input Leakage Current (IN+, IN-, HYST)	V_{IN+} = V_{IN-} = 2.5V	MSOP Package		0.1	1.4	nA
			TDFN Package		0.1	1.5	nA
						3	nA
V_{CM}	Common-Mode Input Range			**V-**		**(V+) - 1.5**	V
CMRR	Common-Mode Rejection Ratio	V- to (V+ - 1.5V)	MSOP Package		1.2	3	mV/V
						3.5	mV/V
			TDFN Package		1.2	4.5	mV/V
						5	mV/V

Analog Specifications

V+= +5.0V. V- = GND = 0V unless otherwise specified, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNITS
PSRR	Power Supply Rejection Ratio	V+ = 2V to 11V	MSOP Package		0.25	1.1	mV/V
						1.2	mV/V
			TDFN Package		0.25	1.5	mV/V
						1.6	mV/V
V_{HYST}	Hysteresis Input Voltage			REF - 50mV		REF	V
t_{PHL}	Propagation Delay - High to Low Transition	C_L = 100pF	Overdrive = 10mV		100		µs
			Overdrive = 100mV		50		µs
t_{PLH}	Propagation Delay - Low to High Transition	C_L = 100pF	Overdrive = 10mV		200		µs
			Overdrive = 100mV		100		µs
V_{OH}	Output High Voltage	I_O = -10mA		**(V+) - 0.4**			V
V_{OL}	Output Low Voltage	I_O = 3mA				**GND + 0.4**	V
REFERENCE							
V_{REF}	Reference Voltage	No Load		**1.176**		**1.188**	V
ΔV_{REF}	Output Load Regulation	$0 \le I_{SOURCE} \le 2mA$			-0.5	-2.0	mV
						-2.5	mV
		$0 \le I_{SINK} \le 10µA$			0.1	2.0	mV
						2.5	mV

Analog Specifications

V+= +3.0V. V- = GND = 0V unless otherwise specified, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNITS
V+ = 3.0V, V- = GND = 0V							
I_{CC}	Supply Current	IN+ = IN- +80mV, HYST = REF			0.40	0.7	µA
						0.8	µA
COMPARATOR							
V_{OS}	Input offset Voltage	V_{CM} = 1.5V	MSOP Package		±2.3	±3.4	mV
						±3.5	mV
			TDFN Package		±2.3	±4.2	mV
						±4.3	mV
I_{IN}	Input Leakage Current (IN+, IN-, HYST)	$V_{IN+} = V_{IN-}$ = 1.5V			0.1	1.1	nA
						3	nA
V_{CM}	Common-Mode Input Range			**V-**		**(V+) - 1.5**	V
CMRR	Common-Mode Rejection Ratio	V- to (V+ - 1.5V)	MSOP Package		1.2	5	mV/V
						5.5	mV/V
			TDFN Package		1.2	7.5	mV/V
						8	mV/V

Analog Specifications V+= +3.0V. V- = GND = 0V unless otherwise specified, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNITS
PSRR	Power Supply Rejection Ratio	V+ = 2V to 11V	MSOP Package		0.25	1.1	mV/V
						1.2	mV/V
			TDFN Package		0.25	1.5	mV/V
						1.6	mV/V
V_{HYST}	Hysteresis Input Voltage			REF - 50mV		REF	V
t_{PHL}	Propagation Delay - High to Low Transition	C_L = 100pF	Overdrive = 10mV		100		µs
			Overdrive = 100mV		50		µs
t_{PLH}	Propagation Delay - Low to High Transition	C_L = 100pF	Overdrive = 10mV		200		µs
			Overdrive = 100mV		100		µs
V_{OH}	Output High Voltage	I_O = -6mA		**(V+) - 0.4**			V
V_{OL}	Output Low Voltage	I_O = 1.8mA				**GND + 0.4**	V
REFERENCE							
V_{REF}	Reference Voltage	No Load		**1.176**		**1.188**	V
ΔV_{REF}	Output Load Regulation	$0 \le I_{SOURCE} \le 2mA$			-0.5	-2.0	mV
						-2.5	mV
		$0 \le I_{SINK} \le 10µA$			0.1	2.0	mV
						-2.5	mV

NOTES:

9. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -40°C to +125°C = +165°C.
10. Parts are 100% tested at +25°C and +85°C. The -40°C and +125°C temperature limits are established by characterization and are not production tested.

Typical Performance Curves

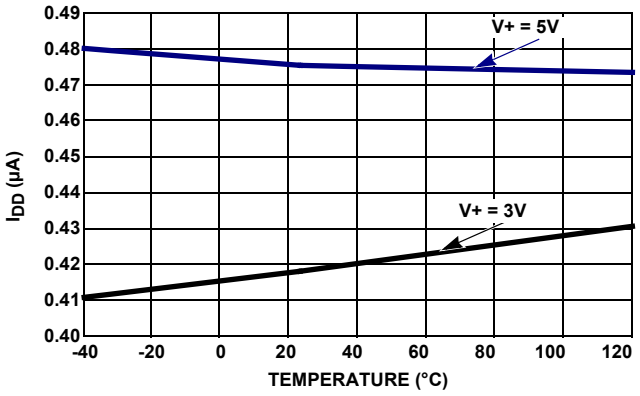


FIGURE 3. I_{DD} vs TEMPERATURE

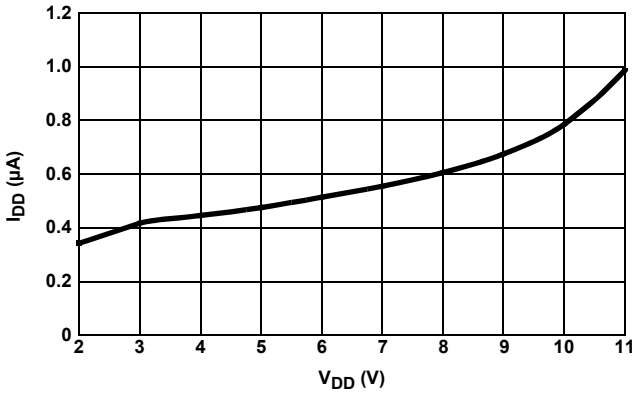


FIGURE 4. I_{DD} vs V_{DD}

Typical Performance Curves (Continued)

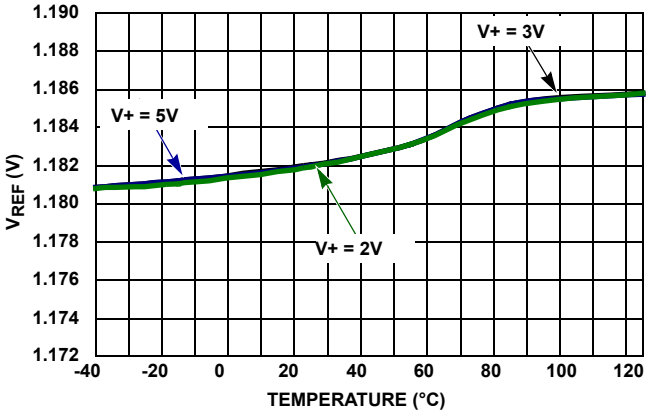


FIGURE 5. V_{REF} vs TEMPERATURE

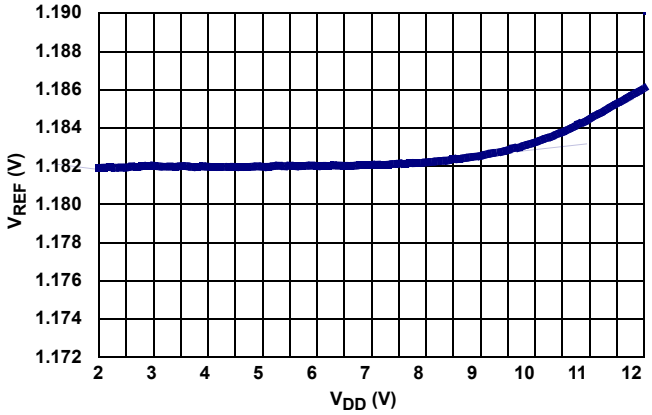


FIGURE 6. V_{REF} vs SUPPLY VOLTAGE

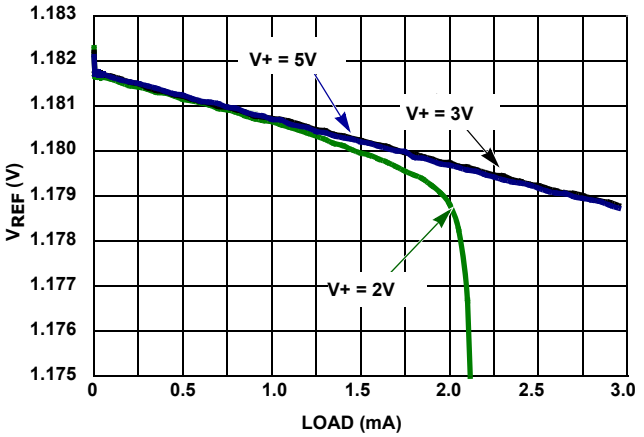


FIGURE 7. V_{REF} vs LOAD (SOURCE)

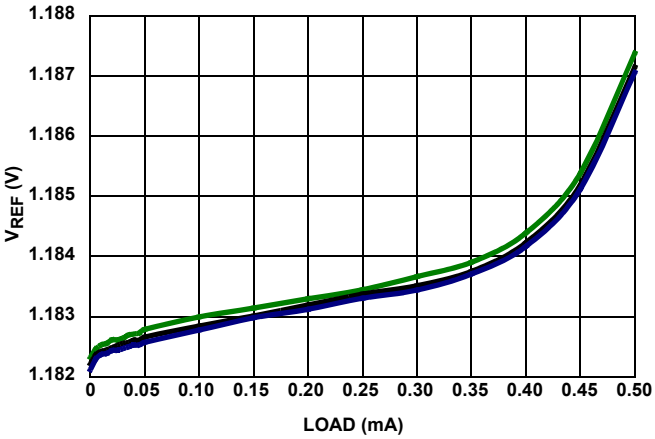


FIGURE 8. V_{REF} vs LOAD (SINK)

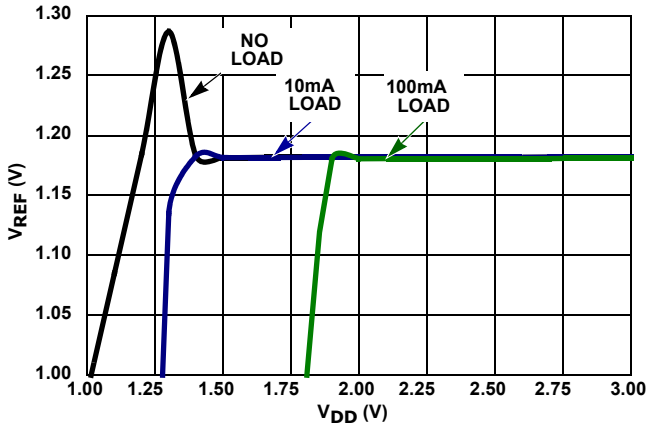


FIGURE 9. DROPOUT - V_{REF} OUTPUT

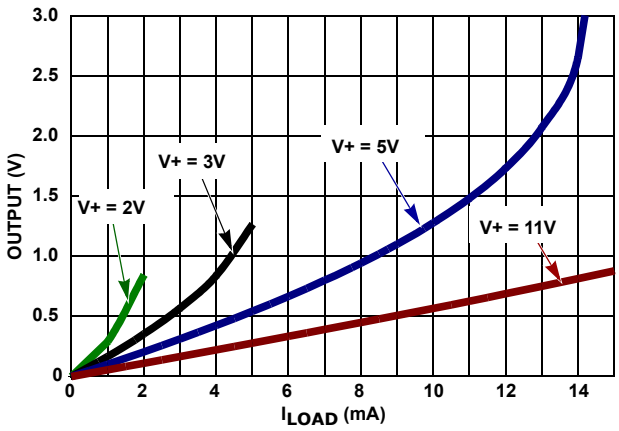


FIGURE 10. COMPARATOR OUTPUT LOW VOLTAGE vs LOAD

Typical Performance Curves (Continued)

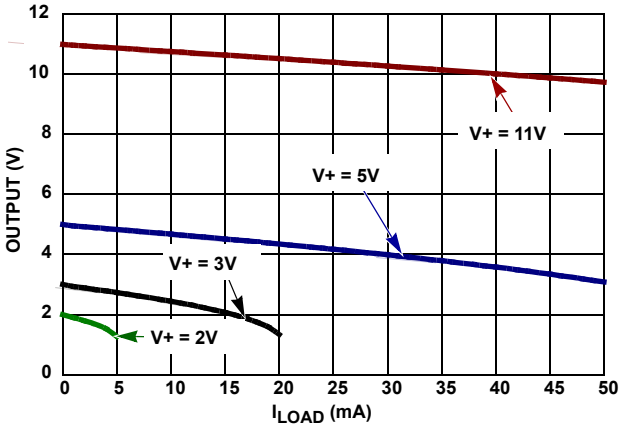


FIGURE 11. COMPARATOR OUTPUT HIGH VOLTAGE vs LOAD

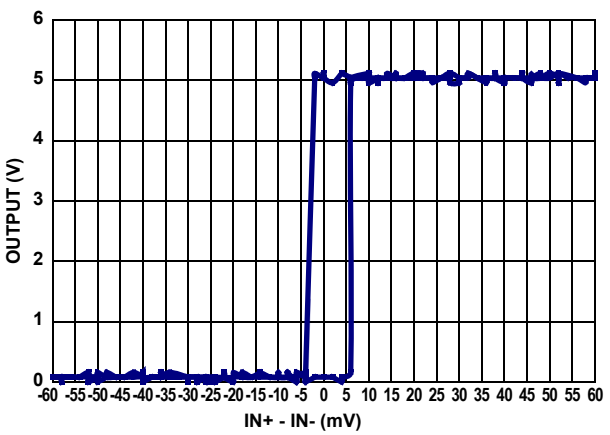


FIGURE 12. HYSTERESIS - 0mV (V+ = 5V)

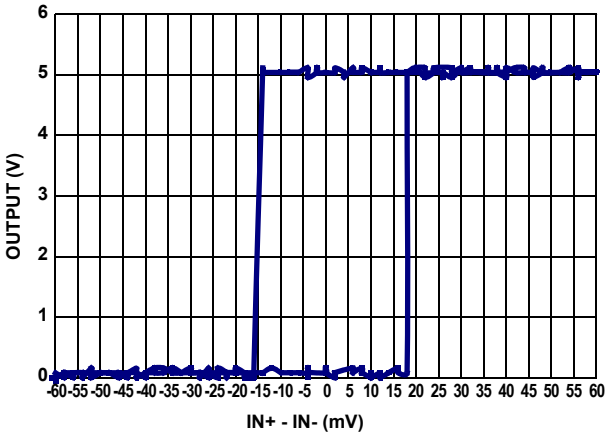


FIGURE 13. HYSTERESIS - 12.5mV (V+ = 5V)

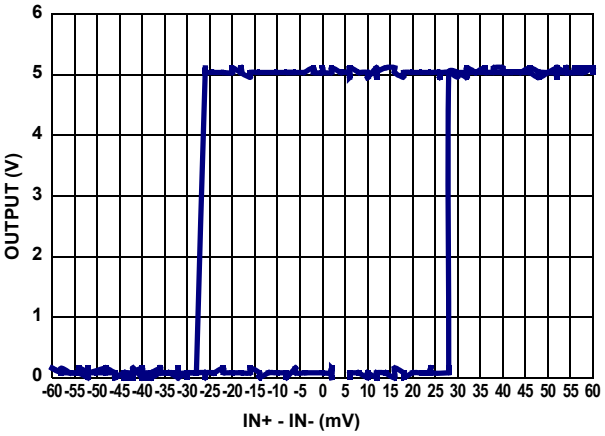


FIGURE 14. HYSTERESIS - 25mV (V+ = 5V)

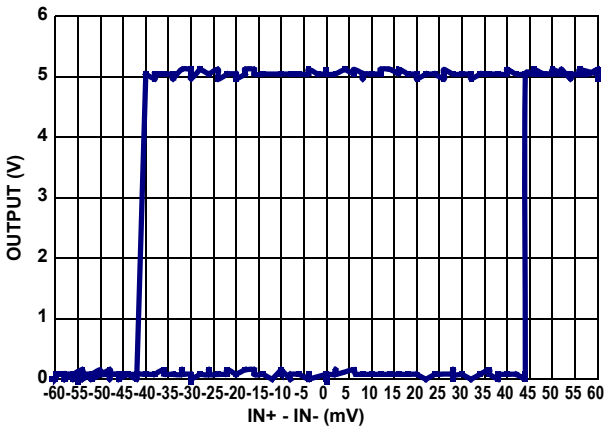


FIGURE 15. HYSTERESIS - 37.5mV (V+ = 5V)

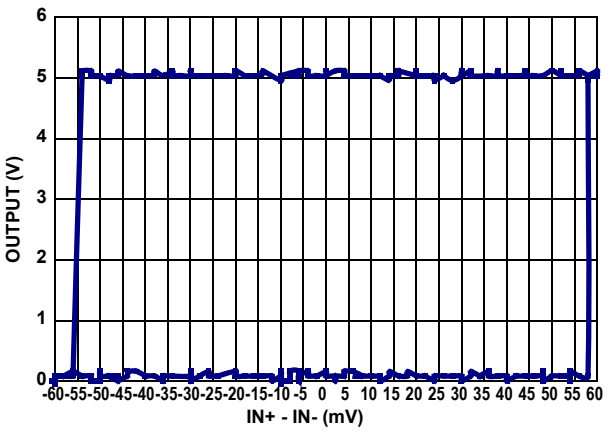


FIGURE 16. HYSTERESIS - 50mV (V+ = 5V)

Typical Performance Curves (Continued)

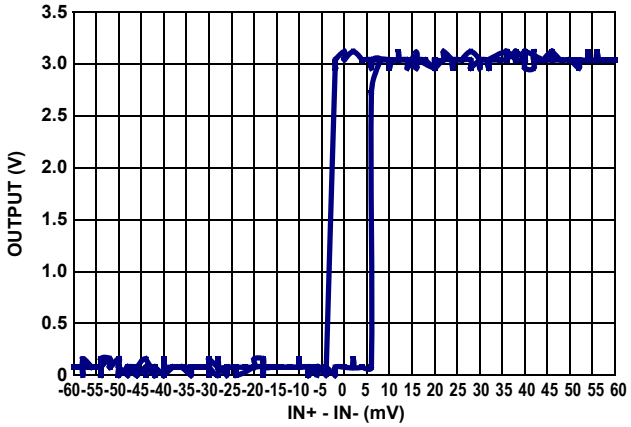


FIGURE 17. HYSTERESIS - 0mV (V+ = 3V)

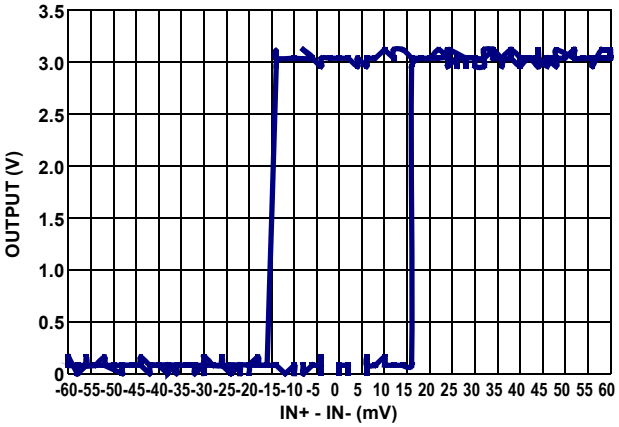


FIGURE 18. HYSTERESIS - 12.5mV (V+ = 3V)

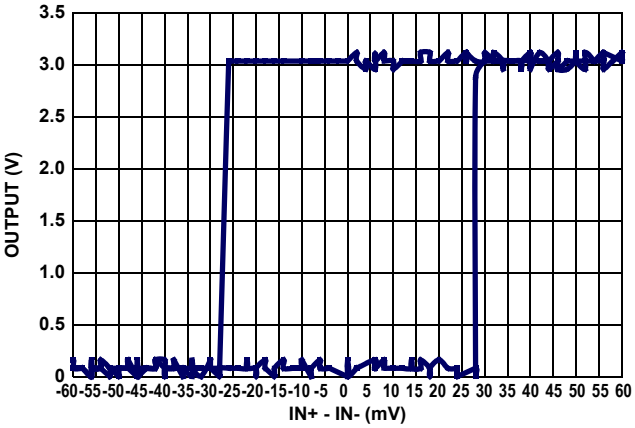


FIGURE 19. HYSTERESIS - 25mV (V+ = 3V)

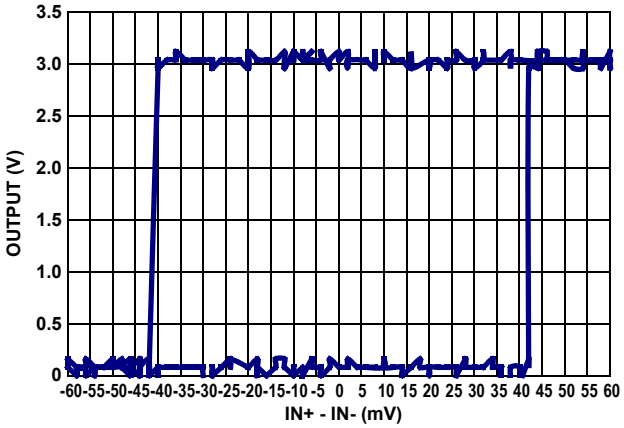


FIGURE 20. HYSTERESIS - 37.5mV (V+ = 3V)

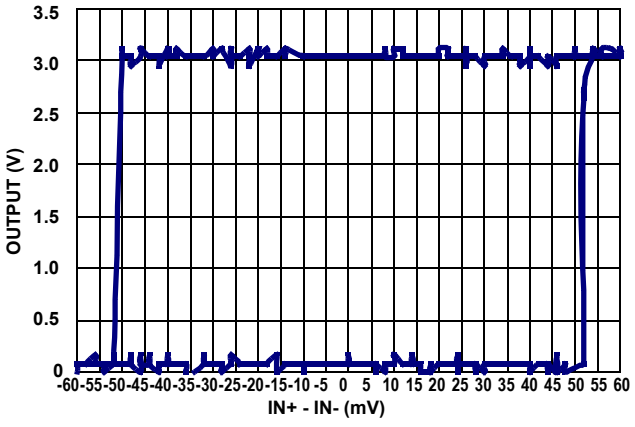


FIGURE 21. HYSTERESIS - 50mV (V+ = 3V)

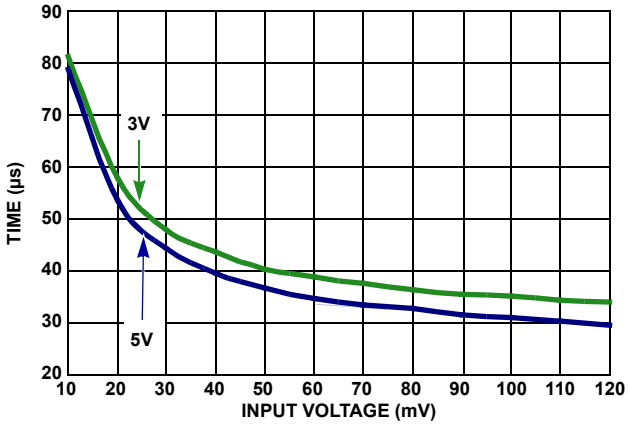


FIGURE 22. OUTPUT RESPONSE TIME vs INPUT OVERDRIVE (t_{PHL})

Typical Performance Curves (Continued)

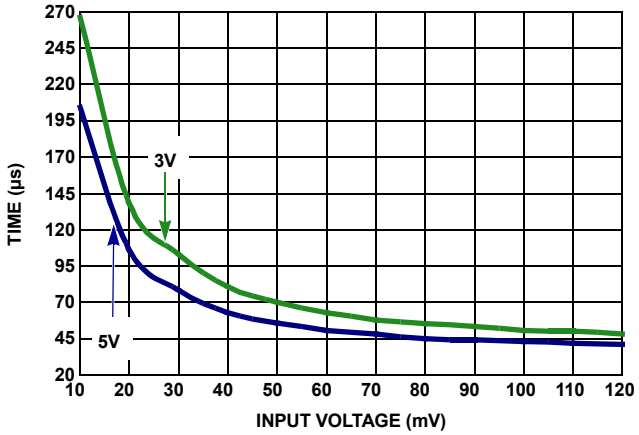


FIGURE 23. OUTPUT RESPONSE TIME vs INPUT OVERDRIVE (t_{PLH})

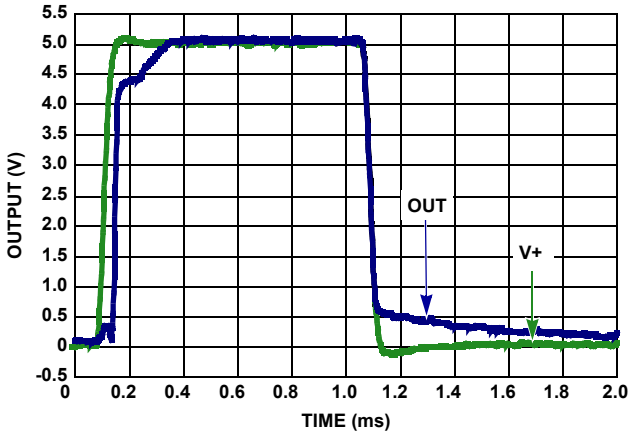


FIGURE 24. POWER-UP/DOWN OUTPUT RESPONSE (V+ = 5V, IN+ = V+, IN- = V_{REF})

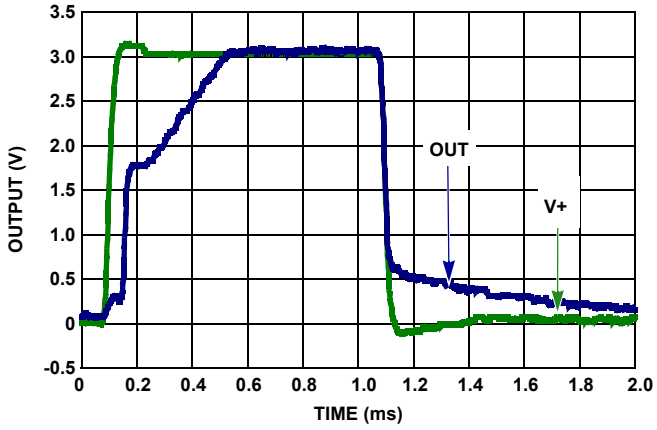


FIGURE 25. POWER-UP/DOWN OUTPUT RESPONSE (V+ = 3V, IN+ = V+, IN- = V_{REF})

Functional Description

Device Power

The ISL21440 device has a single positive supply pin, V+, and two other supply pins, V- and GND. Normally for single supply applications the V- pin is tied to system ground as well as the GND pin. The separate ground pin allows the comparator to be powered by split supplies from ±1.0V to ±5.5V. Note that the minimum supply voltage will be 0.8V above the comparator maximum input level for accurate operation.

Comparator Section

The comparator inputs can swing from the negative supply (GND pin) to within 0.8V of the positive supply (V+). Alternatively, with the comparator input set at the 1.182V reference level, the minimum input voltage for accurate operation is 2.0V. If the inputs are expected to see voltage levels above V+ or below ground, they should be clamped with low leakage Schottky diodes.

The CMOS output swings essentially from the GND potential to V+ potential, depending on load current. If loads in excess of 1mA are expected, then a 0.1µF decoupling capacitor at the V+ pin should be added.

Voltage Reference Section

The voltage reference is a micropower FGA reference and is set to 1.182V ±0.5% at the factory. The reference output can source up to 2mA but the sink capability is very limited at only 10µA, maximum. Small value capacitors, up to 10nF, can be used on the reference output to lower noise if desired.

Applications Information

Handling and Board Mounting

FGA references provide excellent initial accuracy and low temperature drift at the expense of very little power drain. There are some precautions to take to insure this accuracy is not compromised. Excessive heat during solder reflow can cause excessive initial accuracy drift, so the recommended +260°C max temperature profile should not be exceeded. Expect up to 1mV drift from the solder reflow process.

FGA references are susceptible to excessive X-radiation like that used in PC board manufacturing. Initial accuracy can change

10mV or more under extreme radiation. If an assembled board needs to be X-rayed, care should be taken to shield the FGA reference device.

Hysteresis

The Hysteresis function allows for changing the value of the reference switchover point depending on the previous state of the comparator. This works to remove the effects of noise or glitches in the voltage detection input and provide more reliable output transitions.

Hysteresis is added to the ISL21440 by connecting one resistor between the REF and HYST pins (R_{REF}), and another resistor(R_{HYST}) between the HYST pin and ground. The hysteresis voltage (V_H) is designed to be twice the voltage difference between the HYST pin and REF pin ($V_H = 2 * (V_{REF} - V_{HYST})$). Since the reference voltage is 1.182V (V_{REF}), Equations 1 and 2 for these two resistors are shown as follows:

$$R_{REF} = V_H/(2*I_{REF}) = (V_{REF} - V_{HYST})/I_{REF} \quad \text{(EQ. 1)}$$

$$R_{HYST} = (1.182 - V_H/2)/I_{REF} = V_{HYST}/I_{REF} \quad \text{(EQ. 2)}$$

I_{REF} is chosen to be less than the maximum output of the reference, usually 5µA is a safe value but for lowest power, 0.1µA can be used.

If the hysteresis is not used, the HYST pin should be tied to the REF pin.

Board Assembly Considerations

FGA references provide high accuracy and low temperature drift but some PC board assembly precautions are necessary. Normal Output voltage shifts of 100µV to 1mV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

Post-assembly X-ray inspection may also lead to permanent changes in device output voltage and should be minimized or avoided. If X-ray inspection is required, it is advisable to monitor the reference output voltage to verify excessive shift has not occurred. If large amounts of shift are observed, it is best to add an X-ray shield consisting of thin zinc (300µm) sheeting to allow clear imaging, yet block x-ray energy that affects the FGA reference.

Special Applications Considerations

In addition to post-assembly examination, there are also other X-ray sources that may affect the FGA reference long term accuracy. Airport screening machines contain X-rays and will have a cumulative effect on the voltage reference output accuracy. Carry-on luggage screening uses low level X-rays and is not a major source of output voltage shift, although if a product is expected to pass through that type of screening over 100x it may need to consider shielding with copper or aluminum. Checked luggage X-rays are higher intensity and can cause output voltage shift in much fewer passes, so devices expected to go through those machines should definitely consider shielding. Note that just two layers of 1/2 ounce copper planes will reduce the received dose by over 90%. The lead frame for the device which is on the bottom also provides similar shielding.

If a device is expected to pass through luggage X-ray machines numerous times, it is advised to mount a 2-layer (minimum) PC board over the top of the package, which along with a ground plane underneath will effectively shield it from 50 to 100 passes through the machine. Since these machines vary in X-ray dose delivered, it is difficult to produce an accurate maximum pass recommendation.

Typical Applications

Low Battery Detector

Figure 26 shows a typical implementation for the ISL21440, a low battery detector. The values for R_{REF} and R_{HYST} provide 20mV of hysteresis and 0.5µA I_{REF}. The input trip point for V_{detect} is the same as the reference voltage, 1.182V, and a resistor divider at the input sets the Lo_{BAT} trip point at 2.7V. The total current draw for the circuit is going to be 1.1µA for V_{DD} and 0.6µA for V_{BAT}.

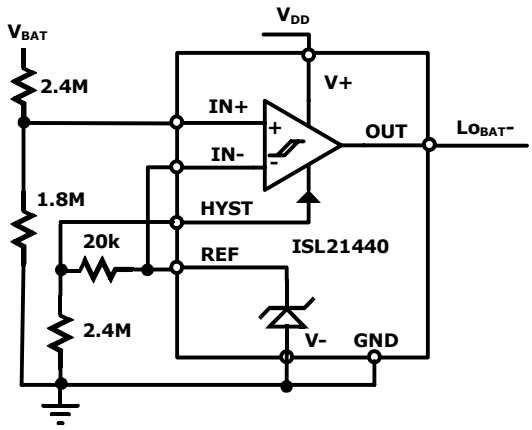


FIGURE 26. LOW BATTERY DETECTOR WITH HYSTERESIS

Window Comparator

The ISL21440 can be combined with a micropower comparator to produce a window comparator circuit. The circuit in Figure 27 uses a 3 resistor divider to produce high and low trip points, and the ISL28197 (800nA supply current) comparator is added to give the second output. The two outputs can be used separately for over or undervoltage indication, or a gate can be added as shown to report either in-window or out-of window condition.

The resistors are shown as Equations 3, 4 and 5 as follows.

Set:

$$R_3 = 1M(1\%) \quad \text{(EQ. 3)}$$

$$R_2 = R_3[V_H/V_L - 1] \quad \text{(EQ. 4)}$$

$$R_1 = R_3([V_H/V_{REF} - 1] - R_2) \quad \text{(EQ. 5)}$$

Example: For $V_H = 3.8V$, $V_L = 2.7V$ (3.3V ± 0.5V)

$R_2 = 402k$, $R_1 = 1.82M$ (can be 1%)

The resulting circuit draws about 3µA and works down to V_{DD} = 2.2V.

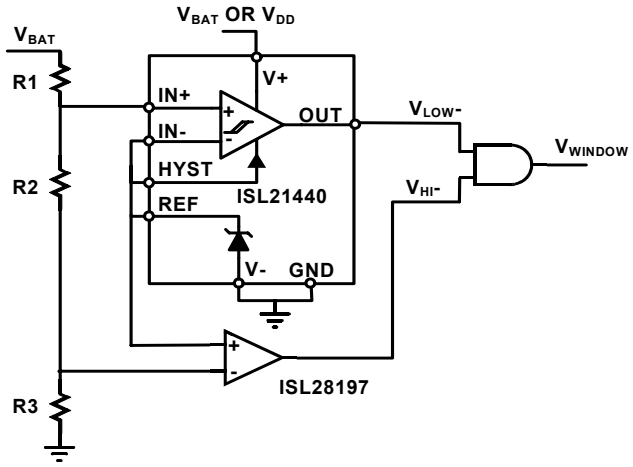


FIGURE 27. WINDOW COMPARATOR CIRCUIT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
1/24/11	FN6532.2	On page 3: Updated Tape & Reel note in “Ordering Information” to add new standard "Add “-T*” suffix for tape and reel." The "*" covers all possible tape and reel options On page 6: Separated “Analog Specifications” tables into 2 tables. Put specs from "V+ = 3.0V, V- = GND = 0V" to end of table into separate table and added following common conditions: "V+= +3.0V. V- = GND = 0V unless otherwise specified, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**" On page 6: Changed conditions for “V_{OH}” from Io = -7mA to Io = -6mA Changed conditions for “V_{OL}” from Io = 3mA to Io = 1.8mA
3/31/10		In “Window Comparator” on page 12, changed "with a micropower to.." to: "with a micropower comparator to.." Page 14, replaced POD M8.118 with newest revision. Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing
3/2/10	FN6532.1	Updated datasheet with the TDFN spec. Spec added on pages 5-6 are: VOS, IIN, CMRR and PSRR. Each spec has an added row for the TDFN package and the original limit for the MSOP package.
12/7/09	FN6532.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL21440

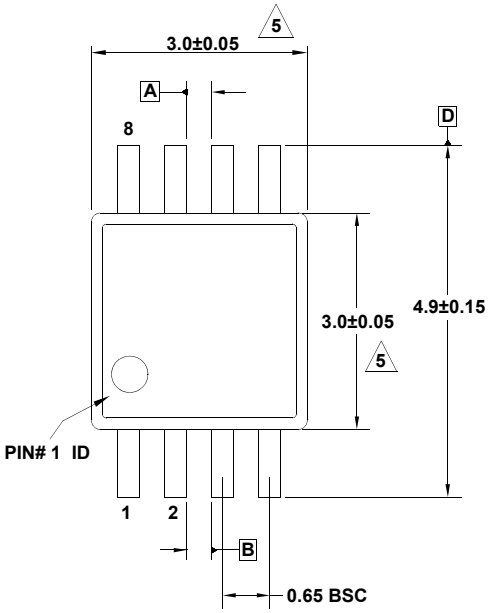
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

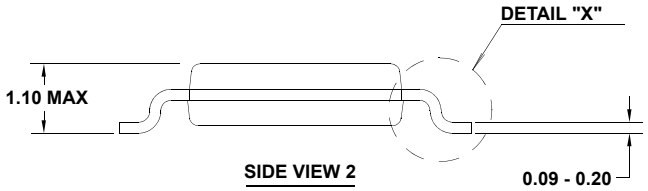
Package Outline Drawing

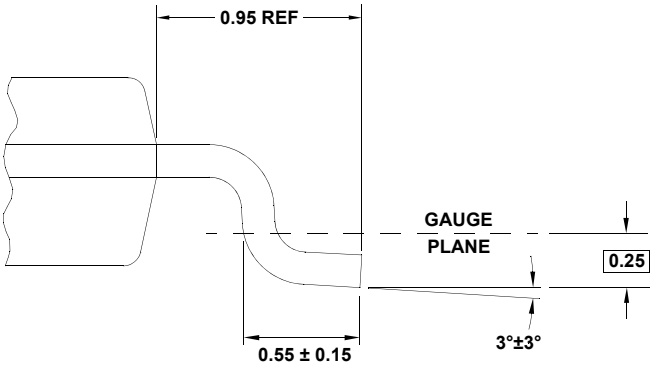
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10

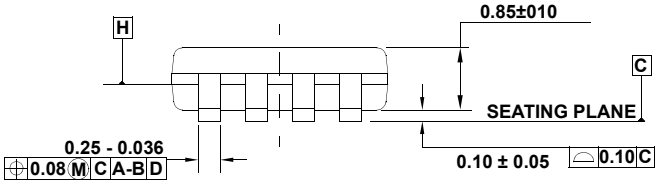


TOP VIEW

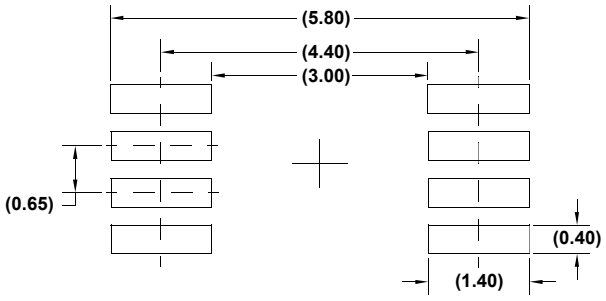




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

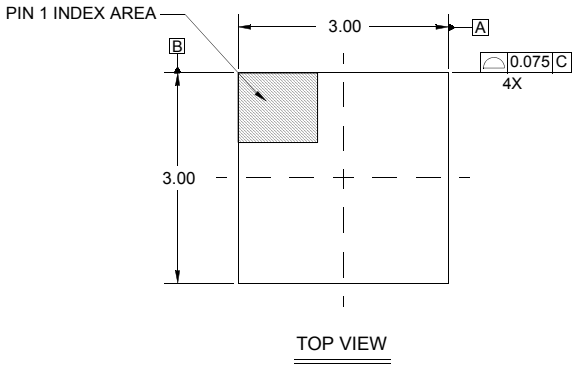
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

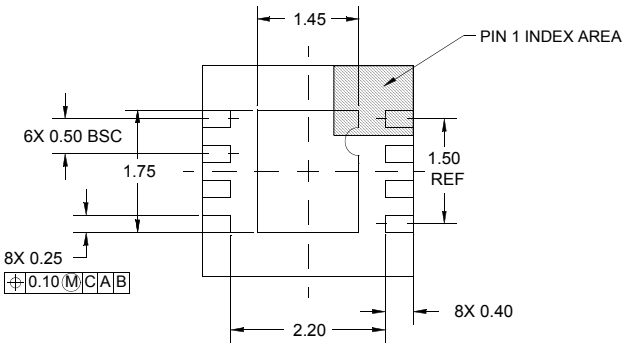
Package Outline Drawing

L8.3x3G

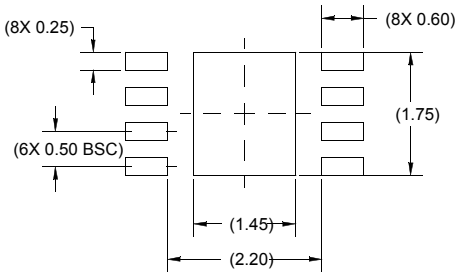
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN)
Rev 0, 5/07



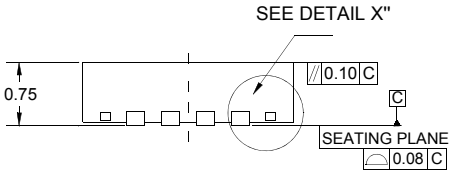
TOP VIEW



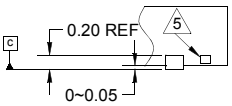
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Controlling dimensions are in mm.
   Dimensions in ( ) for reference only.
2. Unless otherwise specified, tolerance : Decimal ±0.05
   Angular ±2°
3. Dimensioning and tolerancing conform to JEDEC STD MO220-D.
4. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
5. Tiebar shown (if present) is a non-functional feature.