Four-Channel 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1334

FEATURES

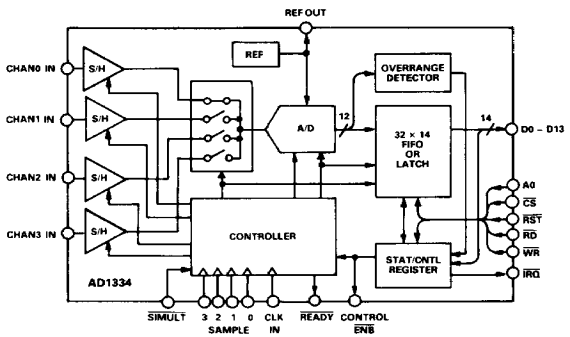
Four-Channel A/D Converter for DSP Includes:
- **Simultaneous or Independent Sampling Capability**
- **12-Bit Accurate A/D Converter**
- **2-Bit Channel ID Tags Each Conversion Result**
- **32-Word FIFO Memory**
- **Fully Asynchronous, High Speed Digital Interface**

Single-Channel Sample Rate Up to 67 kHz
Four-Channel Simultaneous Sample Rate Up to 28 kHz
Entire System Dynamically Characterized
Minimal Effective Aperture Delay Mismatch from Channel-to-Channel & Device-to-Device
15 ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230
Low Power, 250 mW/Channel

APPLICATIONS

Sonar Signal Processing
Robotics/Machine Control
Disk-Drive Head Positioning
Vibration Analysis

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1334 is a four-channel, 12-bit, sampling A/D converter system optimized for use in multichannel digital signal processing (DSP) applications. The device consists of four independent sample-and-hold amplifiers, a multiplexer, an A/D converter, a controller, a 32-word FIFO memory and a fully asynchronous high speed digital interface. The product is packaged in a 40-pin hermetic DIP.

The channel controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

For effective use in simultaneous sampling applications, the sample-and-hold amplifiers are designed to provide a minimum amount of aperture delay time mismatch from channel-to-channel and device-to-device.

The 12-bit A/D converter can convert ±5 V full scale signals at sample rates up to 67 kHz for single-channel operation. In the simultaneous mode, the AD1334 has a four-channel sample rate up to 28 kHz. The entire converter system is specified and tested for signal-to-noise ratio, total harmonic distortion and channel-to-channel isolation.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). The AD1334 can also generate an interrupt when the A/D conversion results are overrange.

The AD1334 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

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This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD1334—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V and f_{CLK} = 2.5 MHz unless noted)

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
S/H, MUX & A/D CONVERTER[1]							
Input Impedance	2	2.5		2	2.5		kΩ
Voltage Range		−5 to +5			−5 to +5		V
Output Coding		Offset Binary			Offset Binary		
CLK IN Frequency, (f_{CLK})	1.0		2.5	1.0		2.5	MHz
High Time	200			200			ns
Low Time	200			200			ns
Sampling Rate Per Channel (f_S)							
Simultaneous Mode ($\overline{SIMULT}$ = LOW)							
1 Channel			67			67	kHz
2 Channels			46			46	kHz
3 Channels			35			35	kHz
4 Channels			28			28	kHz
Independent Mode ($\overline{SIMULT}$ = HIGH)							
1 Channel			67			67	kHz
2 Channels			67			67	kHz
3 Channels			44			44	kHz
4 Channels			33			33	kHz
S/H							
Acquisition Time to 0.01%		6.5	7.5		6.5	7.5	µs
Droop Rate		0.2	1.0		0.2	1.0	mV/ms
Over Temperature		Doubles Every 10°C			Doubles Every 10°C		
−3 dB Small Signal Bandwidth		200			200		kHz
Group Delay[2] (f_{IN}<10 kHz)		785			785		ns
Aperture Delay[3]	0	10	15	0	10	15	ns
Effective Aperture Delay[4] (f_{IN}<10 kHz)	−700	−775	−850	−700	−775	−850	ns
Static Characteristics							
Integral Linearity Error		±1/2	+1		±1/2	+1	LSB
Over Temperature			±1			±1 1/2	LSB
Differential Linearity Error			±1			±1	LSB
Over Temperature			±1			±2	LSB
−Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
+Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
Dynamic Characteristics[5, 6]							
Signal-to-Noise Ratio, f_{IN} = 13.6 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 13.6 kHz		−86	−76		−86	−76	dB
Intermodulation Distortion, f_{IN1} = 13.1 kHz & f_{IN2} = 13.6 kHz		−86	−76		−86	−76	dB
Channel-to-Channel Isolation[7], f_{IN} = 8.009 kHz							
$\overline{SIMULT}$ = LOW	70	78		70	78		dB
$\overline{SIMULT}$ = HIGH		74			74		dB
Reference Voltage	−5.05		−4.95	−5.05		−4.95	V
Output Current	±1	±2		±1	±2		mA
Drift		±10	±30		±10	±30	ppm/°C

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS[6]							
Voltage Input, LOW			+0.8			+0.8	V
HIGH	+2.0			+2.25			V
Input Current			±250			±250	μA
Input Capacitance		5			5		pF
$\overline{RST}$ LOW Pulse Width	10			10			ns
DIGITAL OUTPUTS[6]							
D0–D13, $\overline{READY}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
Output Voltage, Logic HIGH[8]	+2.4			+2.4			V
3-State Leakage Current			±250			±250	μA
$\overline{IRQ}$, CONTROL $\overline{ENB}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
$\overline{IRQ}$ Off-State Leakage			±10			±10	μA
Output Capacitance		5			5		pF
FIFO Fall-Thru Time		400	800		400	800	ns
$\overline{IRQ}$ LOW to D0–D13 Valid[9]			0			0	ns
POWER REQUIREMENTS							
Operating Range							
$\pm V_S$	±11.4		±15.75	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	+4.75		+5.25	V
Supply Current							
$+V_S$		47	60		47	60	mA
$-V_S$		39	50		39	50	mA
$+V_{DD}$		7	15		7	15	mA
Consumption							
$\pm V_S$ = ±12 V		1.0	1.2		1.0	1.2	W
$\pm V_S$ = ±15 V		1.25	1.5		1.25	1.5	W
TEMPERATURE RANGE							
Operating and Specified	−40		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]Specifications are per channel in 4 Channel Simultaneous Mode (SAMPLE 0–3 connected together and $\overline{SIMULT}$ & CONTROL $\overline{ENB}$ = LOW), at f_S = 28 kHz, and with SAMPLE 0–3 having an 80% duty cycle unless noted.
[2]Group delay is the negative of the 1st derivative of phase with respect to frequency and is a measure of the analog time delay through the S/H.
[3]Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of the digital time delay through the S/H.
[4]Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).
[5]THD of harmonics 2–7 of the fundamental. SNR of fundamental less harmonics 2–7.
[6]Guaranteed over operating temperature and power supply voltage range.
[7]Isolation of any one channel from remaining three channels which have near maximum amplitude ac signals at their inputs.
[8]I_{OL} = 4 mA for AD1334BD, I_{OL} = 3.2 mA for AD1334TD; I_{OH} = −4 mA for AD1334BD, I_{OH} = −3.2 mA for AD1334TD.
[9]$\overline{RD}$, $\overline{CS}$, A0 = LOW; $\overline{WR}$, $\overline{RST}$ = HIGH.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1334BD	−40°C to +85°C	DH-40A
AD1334TD/883B	−55°C to +125°C	DH-40A

*D = Hermetic Ceramic DIP. For outline information see Package Information section.

SWITCHING CHARACTERISTICS (over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25		ns
		C_{OUT} = 100 pF	35		ns
t_A	Data Access Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{A0RD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDA0}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		4		ns
t_{A0WR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRA0}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

Specifications subject to change without notice.
All specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Input to APWR/ASIG GND . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE0–SAMPLE3, CLK IN, $\overline{SIMULT}$, CONTROL $\overline{ENB}$ . . . . . −0.3 V to +7 V
Digital Input to DGND
D0–D13, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$ . . −0.3 V to V_{DD}+0.3 V
Output Short Circuit Duration
REF OUT, TP . . . . . Indefinite
Digital Output . . . . . 1 Output for 1 sec
Lead Temperature Range,
Soldering for 10 sec . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.