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SOLID-STATE DISPLAYS WITH INTEGRAL TTL MSI CIRCUIT CHIP FOR USE IN ALL SYSTEMS REQUIRING A DISPLAY OF BCD DATA

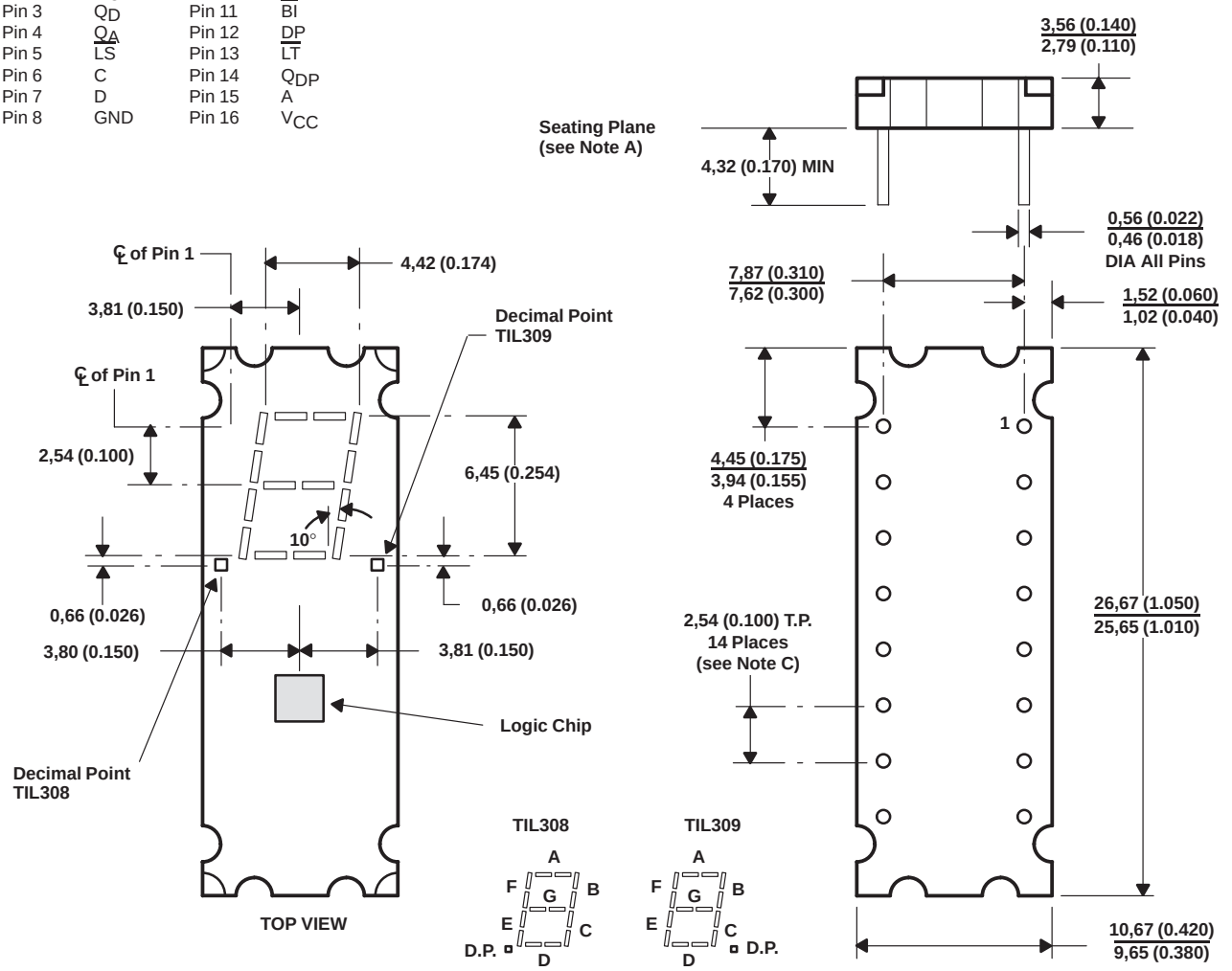
- **6,9-mm (0.270-Inch) Character Height**
- **TIL308 Has Left Decimal**
- **TIL309 Has Right Decimal**
- **Easy System Interface**
- **Wide Viewing Angle**
- **Internal TTL MSI Chip With Latch, Decoder, and Driver**
- **Constant-Current Drive for Light-Emitting Diodes**

mechanical data

These assemblies consist of display chips and a TTL MSI chip mounted on a header with a red molded plastic body. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.

PIN ASSIGNMENTS

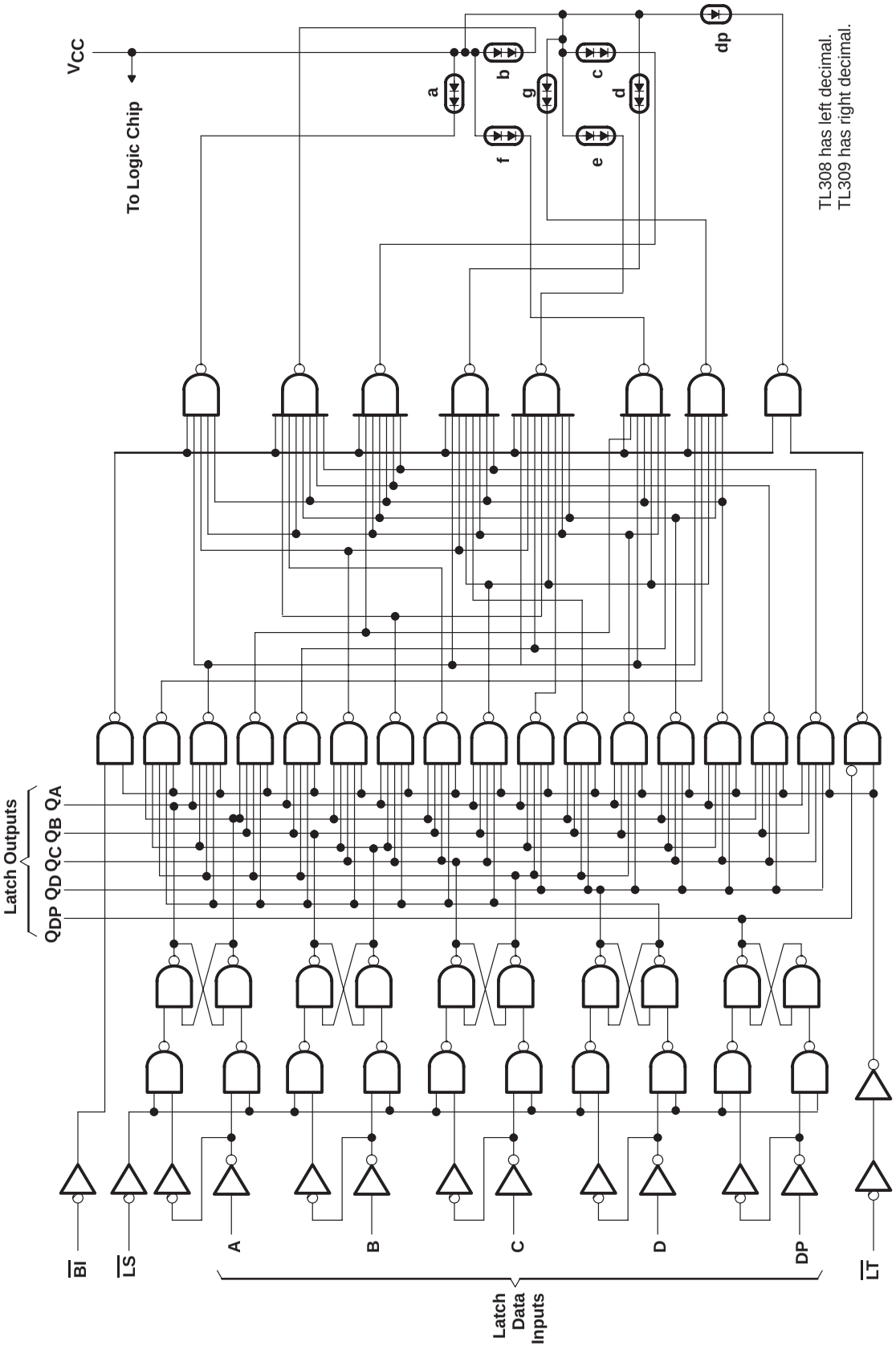
Pin 1	Q_B	Pin 9	NC
Pn 2	Q_C	Pin 10	$\overline{B}$
Pin 3	Q_D	Pin 11	$\overline{BI}$
Pin 4	Q_A	Pin 12	$\overline{DP}$
Pin 5	$\overline{LS}$	Pin 13	$\overline{LT}$
Pin 6	C	Pin 14	Q_{DP}
Pin 7	D	Pin 15	A
Pin 8	GND	Pin 16	V_{CC}



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Lead dimensions are not controlled above the seating plane.
B. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.
C. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located with 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 16.

logic diagram



description

These internally-driven seven-segment light-emitting-diode (LED) displays contain a five-bit latch and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices are in the terminal function table.

The TTL MSI circuits contain the equivalent of 78 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input.

Some of the additional features of these displays are as follows:

- Latched BCD and decimal point logic outputs provided to drive logic processors simultaneously with the displayed data
- Minimum number of inputs required . . . 4-line BCD plus decimal point
- Overriding blanking for suppressing entire display or pulse-modulation of LED brightness
- LED test input to simultaneously turn on all display segments and decimal point
- Can be operated in a real-time mode or latched-update-only mode by use of the latch strobe input
- Displays numbers 0 through 9 as well as A, C, E, F, or minus sign
- Can be blanked by entry of BCD 13 or by use of the blanking input
- Decimal point controlled independently with decimal-point latch
- Constant-current-source TTL-LED interface for optimum performance.

The latch outputs except Q_{DP} are active pullup, and each one, except Q_{DP}, is capable of driving three standard Series 54/74 loads. The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately 7 mA through each LED segment and decimal point. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 575 mW with all segments on.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
BLANKING Input ($\overline{BI}$)	11	When low, will blank (turn off) the entire display. Mus be high for normal operation of the display.
Latch Data Inputs A, B, C, D, DP	15, 10, 6, 7, 12	Data on these inputs are entered into the latches under the control of the latch strobe input. The binary weights of the inputs are: A = 1, B = 2, C = 4, D = 8. DP is decimal point latch data input.
Latch Outputs Q_A, Q_B, Q_C, Q_D, Q_{DP}	4, 1, 2, 3, 14	The BCD data that drives the decoder is stored in the five latches and is available at these outputs. The binary weights of the outputs are: Q_A = 1, Q_B = 2, Q_C = 4, Q_D = 8. Q_{DP} is decimal point latch output.
LATCH STROBE Input (LS)	5	When low, the data in latches follow the data on the latch inputs. When high, the data in the latches are held constant and are unaffected by new data on the latch inputs.
LED TEST Input ($\overline{LT}$)	13	When low, will turn on the entire display, overriding the data in the latches and the blanking input. Must be high for normal operation of the display.

FUNCTION TABLE

FUNCTION	LATCH INPUTS						BLANKING INPUT	LED TEST	LATCH OUTPUTS					DISPLAY	
	D	C	B	A	DP	STROBE			Q_D	Q_C	Q_B	Q_A	Q_{DP}	TIL308	TIL309
0	L	L	L	L	L	L	H	H	L	L	L	L	L	0	0
1	L	L	L	H	H	L	H	H	L	L	L	H	H	.1	1
2	L	L	H	L	L	L	H	H	L	L	H	L	L	2	2
3	L	L	H	H	H	L	H	H	L	L	H	H	H	.3	3.
4	L	H	L	L	L	L	H	H	L	H	L	L	L	4	4
5	L	H	L	H	H	L	H	H	L	H	L	H	H	.5	5.
6	L	H	H	L	L	L	H	H	L	H	H	L	L	6	6
7	L	H	H	H	H	L	H	H	L	H	H	H	H	.7	7.
8	H	L	L	L	L	L	H	H	H	L	L	L	L	8	8
9	H	L	L	H	H	L	H	H	H	L	L	H	H	.9	9.
A	H	L	H	L	L	L	H	H	H	L	H	L	L	A	A
Minus Sign	H	L	H	H	H	L	H	H	H	L	H	H	H	.-	-.
C	H	H	L	L	L	L	H	H	H	H	L	L	L	C	C
Blank	H	H	L	H	H	L	H	H	H	H	L	H	H	.	.
E	H	H	H	L	L	L	H	H	H	H	H	L	L	E	E
F	H	H	H	H	H	L	H	H	H	H	H	H	H	.F	F.
Blank	X	X	X	X	X	X	L	H	X	X	X	X	X		
LED TEST ($\overline{LT}$)	X	X	X	X	X	X	X	L	X	X	X	X	X	.8	8.

H = high level, L = low level, X = irrelevant.
DP input has arbitrarily been shown activated (high) on every other line of the table.

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): Continuous . . . . . 5.5 V
Nonrepetitive peak, $t_W \le 100$ ms . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating case temperature range, T_C (see Note 2) . . . . . 0°C to 85°C
Storage temperature range . . . . . –25°C to 85°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Normalilzed fanout from each output, N (to Series 54/74 integrated circuits)	Low logic level	Q_{DP}			1	
		Q_A, Q_B, Q_C, Q_D			3	
	High logic level	Q_{DP}			3	
		Q_A, Q_B, Q_C, Q_D			6	
Latch strobe pulse duration, t_W			45			ns
Setup time, t_{su}	Latch data input (DP) before latch strobe ($\overline{LS}$)↑		60			ns
Hold time, t_h	Latch data input (DP) after latch strobe ($\overline{LS}$)↑		0			ns
Operating case temperature, T_C			0		70	°C

electrical characteristics at 25°C case temperature

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_I = –12 mA			–1.5	V
V_{OH}	High-level output voltage	Q_{DP}	V_{CC} = 4.75 V,	I_{OH} = –120 µA	2.4			V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75 V,	I_{OH} = –240 µA				
V_{OL}	Low-level output voltage (see Note 3)	Q_{DP}	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75 V,	I_{OL} = 4.8 mA				
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 2.4 V			20	µA
I_{IL}	Low-level input current		V_{CC} = 5.25 V,	V_I = 0.4 V			–0.8	mA
I_{OS}	Short-circuit output current	Q_A, Q_B, Q_C, Q_D	V_{CC} = 5.25 V		–9		–27.5	mA
		Q_{DP}			–1		–3.2	
I_{CC}	Supply current		V_{CC} = 5.25 V,	All inputs at 0 V		115	180	mA
I_v	Luminous intensity (see Note 4)	Figure 8	V_{CC} = 5 V		700	1200		µcd
		DP Input			40	70		
λ_p	Wavelength at peak emission		V_{CC} = 5 V,	See Note 5		660		nm
$\Delta\lambda$	Spectral bandwidth		V_{CC} = 5 V,	See Note 5		20		nm

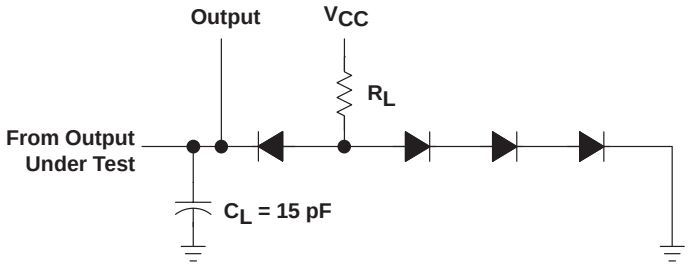
† All typical values are at V_{CC} = 5 V.

NOTES: 3. This parameter is measured with the display blanked.
4. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.
5. These parameters are measured with all LED segments and the decimal point on.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C, D, DP	Q_A, Q_B, Q_C, Q_D, Q_{DP}	C_L = 15 pF, R_L = 1.2 kΩ, See Figure 1		35		ns
t_{PHL}					40		

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. Measurements mode with $\overline{LS}$ input grounded.

Figure 1. Load Circuit

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

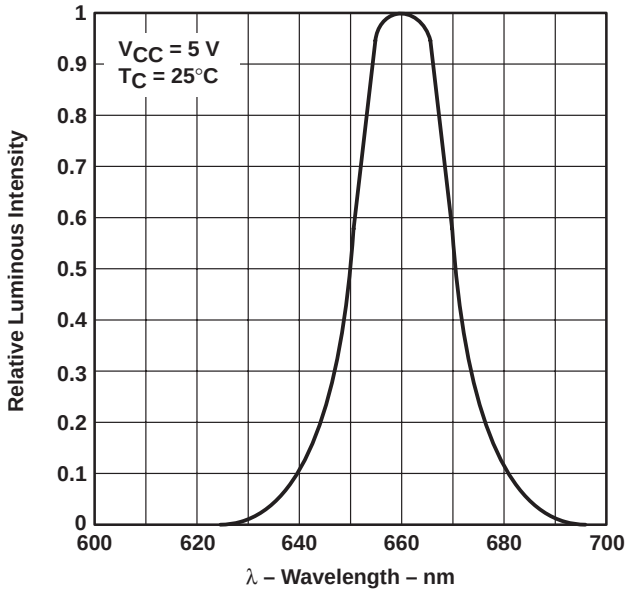


Figure 2

RELATIVE LUMINOUS INTENSITY vs CASE TEMPERATURE

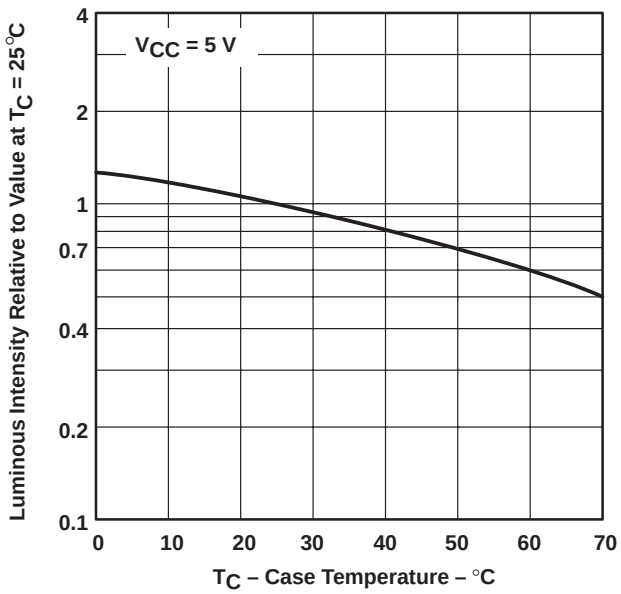


Figure 3

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