

# NT511740D5J

## DATA SHEET

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## DESCRIPTION

This is a family of 4,194,304 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V), refresh cycle (2K Ref), access time (-5 or -6), power consumption (Normal or Low power) and package type (SOJ) are optional features of this family.

All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx4 EDO Mode DRAM family is fabricated using NANYA's advanced CMOS process to realize high bandwidth, low power consumption and high reliability.

It may be used as main memory unit for microcomputer, high level computer and personal computer.

## FEATURES

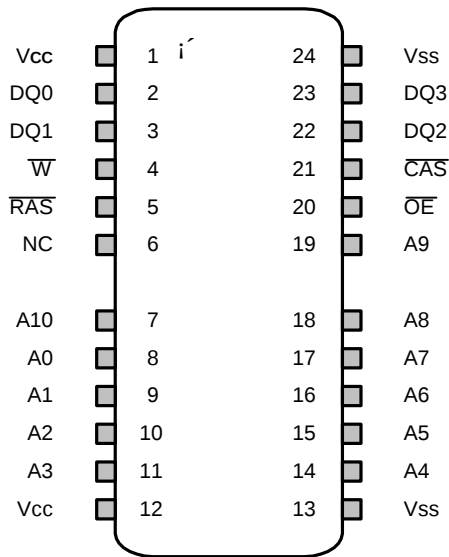
- Extended Data Out Mode operation (Fast Page Mode with Extended Data Out)
- TTL(5V) compatible inputs and outputs
- Single +5V  $\pm$  10% power supply (5V product)
- JEDEC Standard pinout
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Refresh : 2048 cycles / 32 ms
- Self-refresh capability (L-ver only)
- Multi-bit test mode capability
- Available in plastic SOJ packages

## PRODUCT FAMILY

| Family              | Access Time (Max.) |      |       |      | Active Power<br>Dissipation | Voltage | Package           |
|---------------------|--------------------|------|-------|------|-----------------------------|---------|-------------------|
|                     | tRAC               | tCAC | tRC   | tHPC |                             |         |                   |
| NT511740D5J - 50/5L | 50ns               | 15ns | 84ns  | 20ns | 605mW                       | 5V      | 26(24)-pin<br>SOJ |
| NT511740D5J - 60/6L | 60ns               | 17ns | 104ns | 25ns | 550mW                       |         |                   |

PIN CONFIGURATION (TOP VIEW)

NT511740D5J



300mil 26(24)-pin SOJ

| Pin Name | Pin Function            |
|----------|-------------------------|
| A0-A10   | Address Inputs          |
| DQ0-DQ3  | Data Input / Output     |
| Vss      | Ground                  |
| RAS      | Row Address Strob       |
| CAS      | Column Address Strob    |
| W        | Read/Write Input        |
| OE       | Data Output Enable      |
| Vcc      | Power +5.0 V ( + 3.3V ) |
| NC       | No Connection           |

## ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

| Parameter                                       | Symbol            | Rating       | Unit |
|-------------------------------------------------|-------------------|--------------|------|
| Voltage on Any Pin Relative to $V_{SS}$         | $V_{IN}, V_{OUT}$ | -1.0 to +7.0 | V    |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{CC}$          | -1.0 to +7.0 | V    |
| Short Circuit Output Current                    | $I_{OS}$          | 50           | mA   |
| Power Dissipation                               | $P_D^*$           | 1            | W    |
| Operation Temperature                           | $T_{opr}$         | 0 to 70      | °C   |
| Storage Temperature                             | $T_{stg}$         | -55 to 150   | °C   |

\*:  $T_a = 25^\circ\text{C}$ 

- Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

(Voltage referenced to  $V_{SS}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

| Parameter          | Symbol   | Min.        | Typ. | Max.              | Unit |
|--------------------|----------|-------------|------|-------------------|------|
| Supply Voltage     | $V_{CC}$ | 4.5         | 5.0  | 5.5               | V    |
| Ground             | $V_{SS}$ | 0           | 0    | 0                 | V    |
| Input High Voltage | $V_{IH}$ | 2.4         | -    | $V_{CC}+1.0^{*1}$ | V    |
| Input Low Voltage  | $V_{IL}$ | $-1.0^{*2}$ | -    | 0.8               | V    |

\*1 :  $V_{CC} + 2.0\text{V}/20\text{ns}(5\text{V})$ , Pulse width is measured at  $V_{CC}$ \*2 :  $-2.0\text{V}/20\text{ns}(5\text{V})$ , Pulse width is measured at  $V_{SS}$ 

## Capacitance

(  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$  )

| Parameter                                                                                     | Symbol    | Typ. | Max. | Unit |
|-----------------------------------------------------------------------------------------------|-----------|------|------|------|
| Input Capacitance (A0-A11)                                                                    | $C_{IN1}$ | -    | 5    | pF   |
| Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ ) | $C_{IN2}$ | -    | 7    | pF   |
| Output Capacitance (DQ0-DQ3)                                                                  | $C_{I/O}$ | -    | 7    | pF   |

## DC Characteristics

(Recommended operating conditions unless otherwise noted.)

| Max | Parameter                                                                                                                | Symbol     | Min | Max | Units         |
|-----|--------------------------------------------------------------------------------------------------------------------------|------------|-----|-----|---------------|
| 5V  | Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{IN}+0.5\text{V}$ , all other input pins not under test = 0 Volt) | $I_{I(L)}$ | -5  | 5   | $\mu\text{A}$ |
|     | Output Leakage Current<br>(Data out is disabled, $0 \leq V_{OUT} \leq V_{CC}$ )                                          | $I_{O(L)}$ | -5  | 5   | $\mu\text{A}$ |
|     | Output High Voltage Level ( $I_{OH} = -5\text{mA}$ )                                                                     | $V_{OH}$   | 2.4 | -   | V             |
|     | Output Low Voltage Level ( $I_{OL} = 4.2\text{mA}$ )                                                                     | $V_{OL}$   | -   | 0.4 | V             |

## DC CHARACTERISTICS ( Continued )

| Symbol | Power      | Speed      | Max | Units |
|--------|------------|------------|-----|-------|
| ICC1   | Don't care | -5         | 110 | mA    |
|        |            | -6         | 100 | mA    |
| ICC2   | Normal     | Don't care | 2   | mA    |
|        | L          |            | 1   | mA    |
| ICC3   | Don't care | -5         | 110 | mA    |
|        |            | -6         | 100 | mA    |
| ICC4   | Don't care | -5         | 90  | mA    |
|        |            | -6         | 80  | mA    |
| ICC5   | Normal     | Don't care | 3   | mA    |
|        | L          |            | 200 | uA    |
| ICC6   | Don't care | -5         | 110 | mA    |
|        |            | -6         | 100 | mA    |
| ICC7   | L          | Don't care | 300 | uA    |
| ICCS   | L          | Don't care | 250 | uA    |

ICC1\* : Operating Current (  $\overline{RAS}$  and  $\overline{CAS}$  cycling @  $t_{RC} = \min.$  )

ICC2 : Standby Current (  $\overline{RAS} = \overline{CAS} = \overline{W} = V_{IH}$  )

ICC3\* :  $\overline{RAS}$ -only Refresh Current (  $\overline{RAS} = V_{IH}$ ,  $\overline{RAS}$  cycling @  $t_{RC} = \min.$  )

ICC4\* : Hyper Page Mode Current (  $\overline{RAS} = V_{IL}$ ,  $\overline{CAS}$  Address cycling @  $t_{HPC} = \min.$  )

ICC5 : Standby Current (  $\overline{RAS} = \overline{CAS} = \overline{W} = V_{CC} - 0.2V$  )

ICC6\* : CAS-Before-  $\overline{RAS}$  Refresh Current (  $\overline{RAS}$ ,  $\overline{CAS}$  Cycling @  $t_{RC} = \min.$  )

ICC7 : Battery back-up current, Average power supply current, Battery back-up mode Input high voltage ( $V_{IH}$ )= $V_{CC} - 0.2V$ , Input low voltage ( $V_{IL}$ )= $0.2V$ ,  $\overline{CAS} = 0.2V$ ,  $DQ = \text{Don't care}$ ,  $t_{RC} = 125\mu s$  (2K/L-ver) ,  $t_{RAS} = t_{RASmin} \sim 300ns$

ICCS : Self Refresh Current

(  $\overline{RAS} = \overline{CAS} = 0.2V$ ,  $\overline{W} = \overline{OE} = A0 \sim A11 = V_{CC} - 0.2V$  or  $0.2V$ ,  $DQ0 \sim DQ3 = V_{CC} - 0.2V$ ,  $0.2V$  or open )

\*Note : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3 and ICC6, address can be changed maximum once while  $\overline{RAS} = V_{IL}$ . In ICC4, address can be changed maximum once within one hyper page mode cycle time,  $t_{HPC}$ .

## AC CHARACTERISTICS

(0°C ≤ Ta ≤ 70°C, See note 1,2) ; Test condition : VCC=5.0V ± 10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.0/0.8V

| Parameter                                                         | Symbol | -50 |     | -60 |     | Unit | Notes  |
|-------------------------------------------------------------------|--------|-----|-----|-----|-----|------|--------|
|                                                                   |        | Min | Max | Min | Max |      |        |
| Random read or write cycle time                                   | t RC   | 84  | -   | 104 | -   | ns   |        |
| Read-modify-write cycle time                                      | t RWC  | 110 |     | 135 |     | ns   |        |
| Access time from $\overline{\text{RAS}}$                          | t RAC  |     | 50  |     | 60  | ns   | 3,4,10 |
| Access time from $\overline{\text{CAS}}$                          | t CAC  |     | 13  |     | 15  | ns   | 3,4,5  |
| Access time from column address                                   | t AA   |     | 25  |     | 30  | ns   | 3,10   |
| $\overline{\text{CAS}}$ to output in Low-Z                        | t CLZ  | 0   |     | 0   |     | ns   | 3      |
| Output buffer turn-off delay from $\overline{\text{CAS}}$         | t CEZ  | 0   |     | 0   |     | ns   | 6,14   |
| $\overline{\text{OE}}$ to output in Low-Z                         | t OLZ  | 0   |     | 0   |     | ns   | 3      |
| Transition time (rise and fall)                                   | t T    | 1   |     | 1   |     | ns   | 2      |
| $\overline{\text{RAS}}$ precharge time                            | t RP   | 30  |     | 40  |     | ns   |        |
| $\overline{\text{RAS}}$ pulse width                               | t RAS  | 50  |     | 60  |     | ns   |        |
| $\overline{\text{RAS}}$ hold time                                 | t RSH  | 7   |     | 10  |     | ns   |        |
| $\overline{\text{CAS}}$ hold time                                 | t CSH  | 35  |     | 40  |     | ns   |        |
| $\overline{\text{CAS}}$ pulse width                               | t CAS  | 7   |     | 10  |     | ns   |        |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time     | t RCD  | 11  |     | 14  |     | ns   | 4      |
| $\overline{\text{RAS}}$ to column address delay time              | t RAD  | 9   |     | 12  |     | ns   | 10     |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | t CRP  | 5   |     | 5   |     | ns   |        |
| Row address set-up time                                           | t ASR  | 0   |     | 0   |     | ns   |        |
| Row address hold time                                             | t RAH  | 7   |     | 10  |     | ns   |        |
| Column address set-up time                                        | t ASC  | 0   |     | 0   |     | ns   |        |
| Column address hold time                                          | t CAH  | 7   |     | 10  |     | ns   |        |
| Column address to $\overline{\text{RAS}}$ lead time               | t RAL  | 25  |     | 30  |     | ns   |        |
| Read command set-up time                                          | t RCS  | 0   |     | 0   |     | ns   |        |
| Read command hold time referenced to $\overline{\text{CAS}}$      | t RCH  | 0   |     | 0   |     | ns   | 8      |
| Read command hold time referenced to $\overline{\text{RAS}}$      | t RRH  | 0   |     | 0   |     | ns   | 8      |
| Write command hold time                                           | t WCH  | 7   |     | 10  |     | ns   |        |
| Write command pulse width                                         | t WP   | 7   |     | 10  |     | ns   |        |
| Write command to $\overline{\text{RAS}}$ lead time                | t RWL  | 7   |     | 10  |     | ns   |        |
| Write command to $\overline{\text{CAS}}$ lead time                | t CWL  | 7   |     | 10  |     | ns   |        |
| Data set-up time                                                  | t DS   | 0   |     | 0   |     | ns   | 9      |
| Data hold time                                                    | t DH   | 7   |     | 10  |     | ns   | 9      |
| Refresh period (2K, Normal)                                       | t REF  |     | 32  |     | 32  | ms   |        |
| Refresh period (L-ver)                                            | t REF  |     | 128 |     | 128 | ms   |        |
| Write command set-up time                                         | t WCS  | 0   |     | 0   |     | ns   | 7      |

## AC CHARACTERISTICS (Continued)

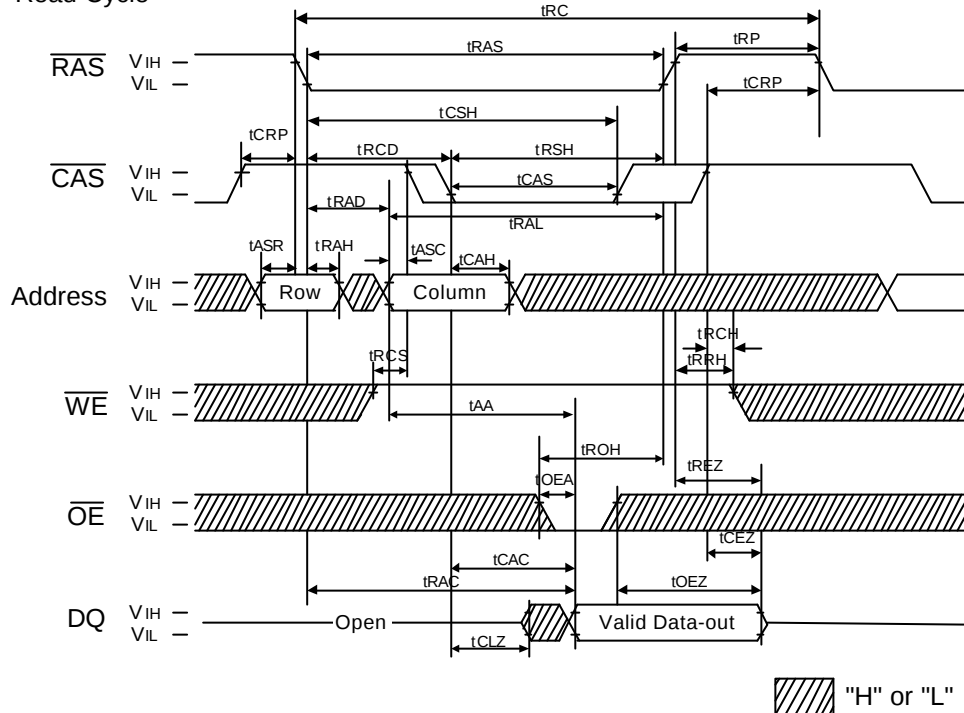
| Parameter                                                                                               | Symbol  | -50 |      | -60 |      | Unit | Notes    |
|---------------------------------------------------------------------------------------------------------|---------|-----|------|-----|------|------|----------|
|                                                                                                         |         | Min | Max  | Min | Max  |      |          |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time                                             | t CWD   | 30  |      | 34  |      | ns   | 7        |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time                                             | t RWD   | 67  |      | 79  |      | ns   | 7        |
| Column address to $\overline{\text{W}}$ delay time                                                      | t AWD   | 42  |      | 49  |      | ns   | 7        |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time                                   | t CPWD  | 47  |      | 54  |      | ns   |          |
| $\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | t CSR   | 5   |      | 5   |      | ns   |          |
| $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)   | t CHR   | 10  |      | 10  |      | ns   |          |
| $\overline{\text{RAS}}$ to CAS precharge time                                                           | t RPC   | 5   |      | 5   |      | ns   |          |
| Access time from $\overline{\text{CAS}}$ precharge                                                      | t CPA   |     | 28   |     | 35   | ns   | 3        |
| Hyper Page cycle time                                                                                   | t HPC   | 20  |      | 25  |      | ns   | 13       |
| Hyper Page read-modify-write cycle time                                                                 | t HPRWC | 47  |      | 56  |      | ns   | 13       |
| $\overline{\text{CAS}}$ precharge time (Hyper Page cycle)                                               | t CP    | 7   |      | 10  |      | ns   |          |
| $\overline{\text{RAS}}$ pulse width (Hyper Page cycle)                                                  | t RASP  | 50  | 100k | 60  | 100k | ns   |          |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge                                | t RHCP  | 30  |      | 35  |      | ns   |          |
| $\overline{\text{OE}}$ access time                                                                      | t OEA   |     | 13   |     | 15   | ns   |          |
| $\overline{\text{OE}}$ to data delay                                                                    | t OED   | 12  |      | 15  |      | ns   |          |
| Output buffer turn off delay time from $\overline{\text{OE}}$                                           | t OEZ   | 3   |      | 3   |      | ns   | 6        |
| $\overline{\text{OE}}$ command hold time                                                                | t OEH   | 7   |      | 10  |      | ns   |          |
| Write command set-up time (Test mode in)                                                                | t WTS   | 7   |      | 10  |      | ns   | 11       |
| Write command hold time (Test mode in)                                                                  | t WTH   | 10  |      | 10  |      | ns   | 11       |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)                          | t WRP   | 10  |      | 10  |      | ns   |          |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)                               | t WRH   | 10  |      | 10  |      | ns   |          |
| Output data hold time                                                                                   | t DOH   | 5   |      | 5   |      | ns   |          |
| Output buffer turn off delay from $\overline{\text{RAS}}$                                               | t REZ   | 0   |      | 0   |      | ns   | 6,14     |
| Output buffer turn off delay from $\overline{\text{W}}$                                                 | t WEZ   | 0   |      | 0   |      | ns   | 6        |
| $\overline{\text{W}}$ to data delay                                                                     | t WED   | 10  |      | 10  |      | ns   |          |
| $\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time                                             | t OCH   | 5   |      | 5   |      | ns   |          |
| $\overline{\text{CAS}}$ hold time to OE                                                                 | t CHO   | 5   |      | 5   |      | ns   |          |
| $\overline{\text{OE}}$ precharge time                                                                   | t OEP   | 7   |      | 10  |      | ns   |          |
| $\overline{\text{W}}$ pulse width (Hyper Page Cycle)                                                    | t WPE   | 7   |      | 10  |      | ns   |          |
| $\overline{\text{RAS}}$ pulse width (C-B-R self refresh)                                                | t RASS  | 100 |      | 100 |      | ns   | 15,16,17 |
| $\overline{\text{RAS}}$ precharge time (C-B-R self refresh)                                             | t RPS   | 90  |      | 110 |      | ns   | 15,16,17 |
| $\overline{\text{CAS}}$ hold time (C-B-R self refresh)                                                  | t CHS   | -50 |      | -50 |      | ns   | 15,16,17 |



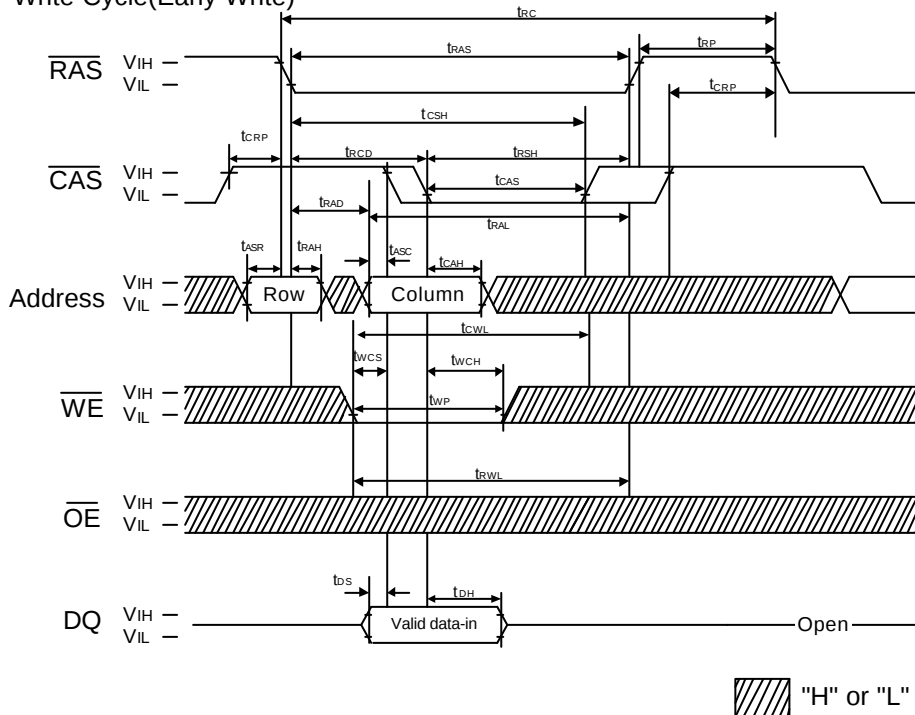
## NOTES

1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh Cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD >= tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS >= tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD >= tCWD(min), tRWD >= tRWD(min) and tAWD >= tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{W}}$  falling edge in  $\overline{\text{OE}}$  controlled Write Cycle and read-modify-write cycles.
9. Operation within the tRAD (max) limit insures that tRAD(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA .
10. These specifications are applied in the test mode.
11. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These Parameters should specified in test mode cycles by adding the above value to the specified value in this data sheet.
12. tASC >= 6ns, Assume t $\tau$  = 2.0ns
13. If  $\overline{\text{RAS}}$  goes high before  $\overline{\text{CAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{CAS}}$  high going.  
If  $\overline{\text{CAS}}$  goes high before  $\overline{\text{RAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{RAS}}$  high going.
14. If tRASS >= 100us, then  $\overline{\text{RAS}}$  precharge time must use tRPS instead of tRP.
15. For RAS-only refresh and burst  $\overline{\text{CAS}}$  -before- $\overline{\text{RAS}}$  refresh mode, 2048(2K) cycles of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification..
16. For distributed  $\overline{\text{CAS}}$  -before- $\overline{\text{RAS}}$  with 15.6us interval  $\overline{\text{CAS}}$  -before- $\overline{\text{RAS}}$  refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

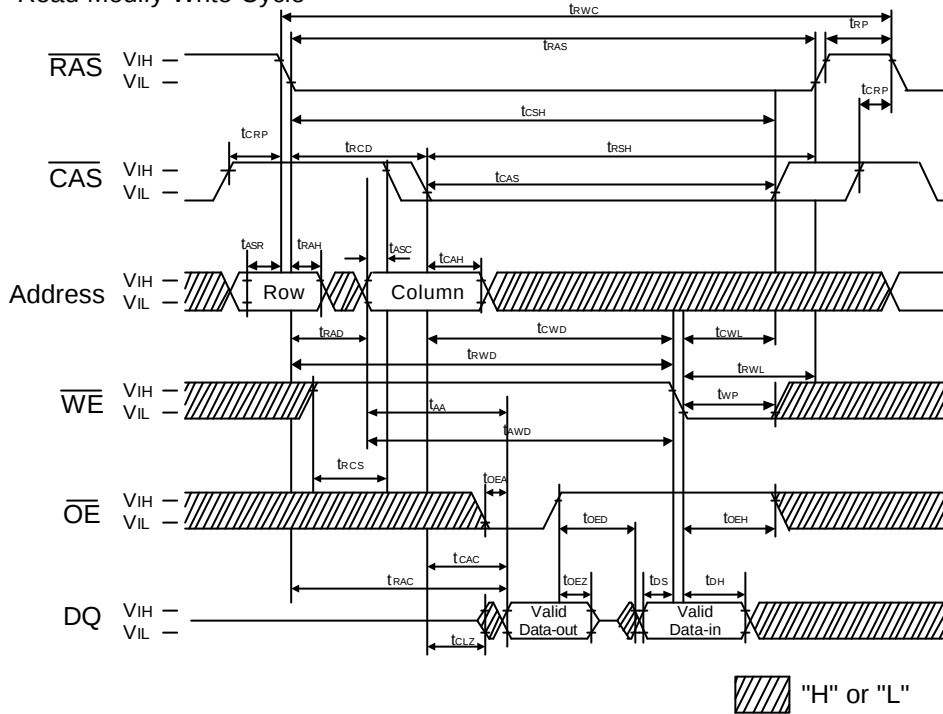
### Read Cycle



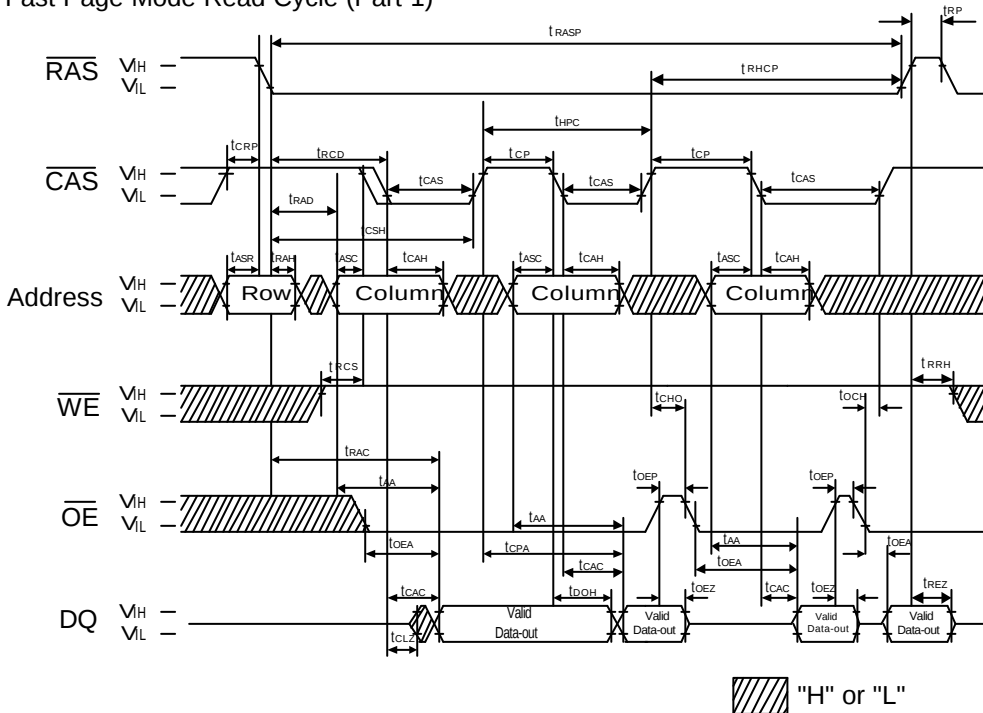
Write Cycle(Early Write)



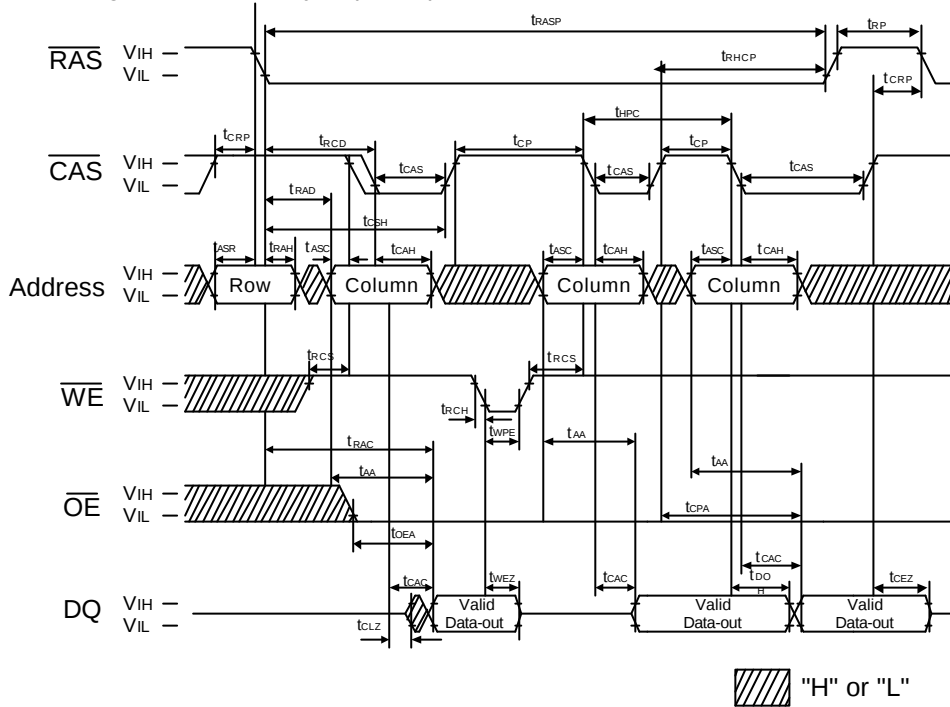
## Read Modify Write Cycle



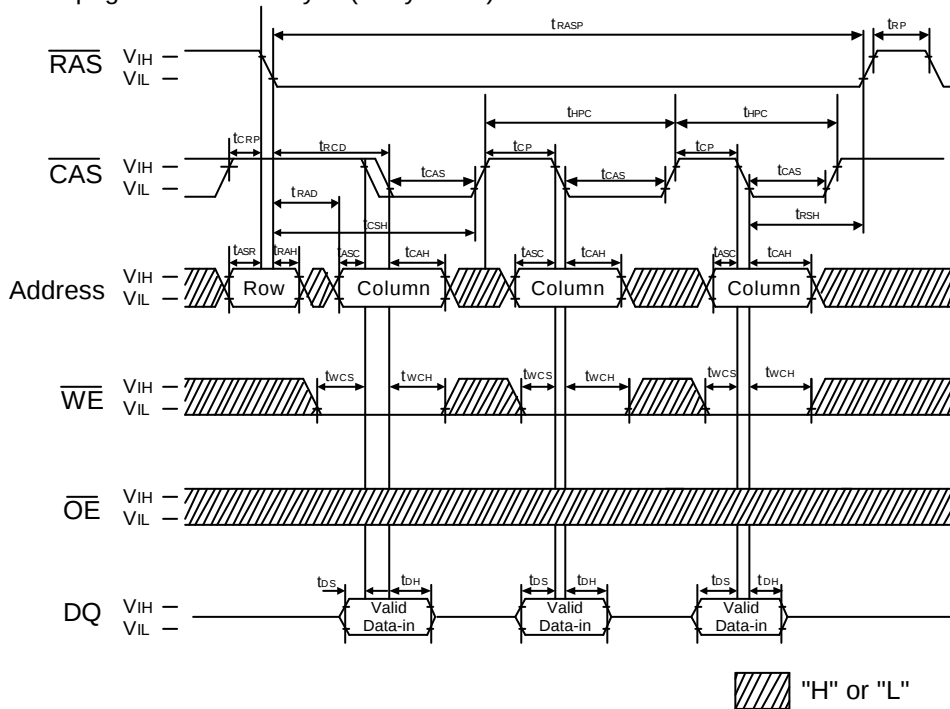
## Fast Page Mode Read Cycle (Part-1)



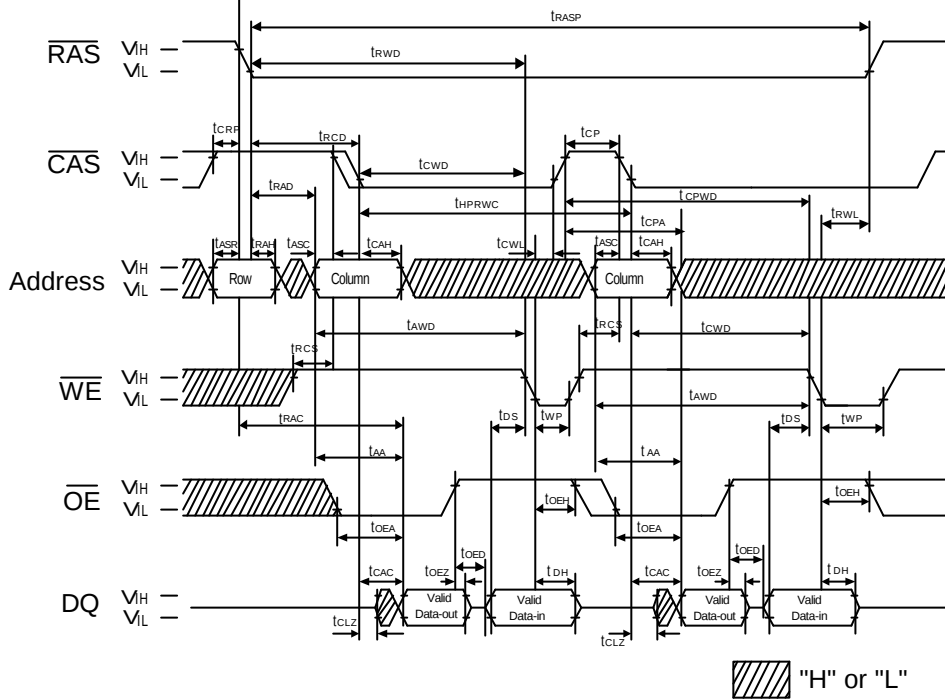
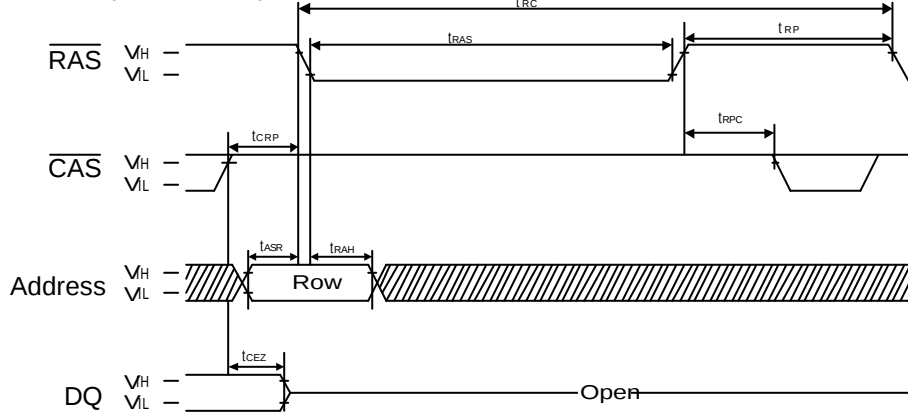
## Fast Page Mode Read Cycle(Part-2)

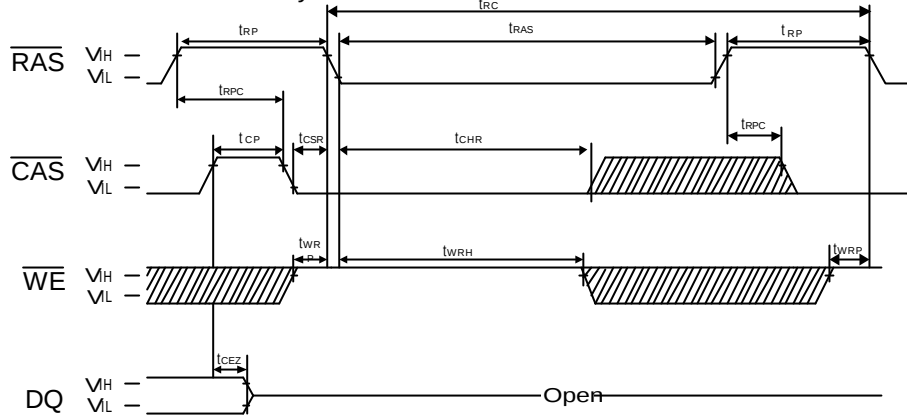


## Fast page Mode Write Cycle(Early Write)



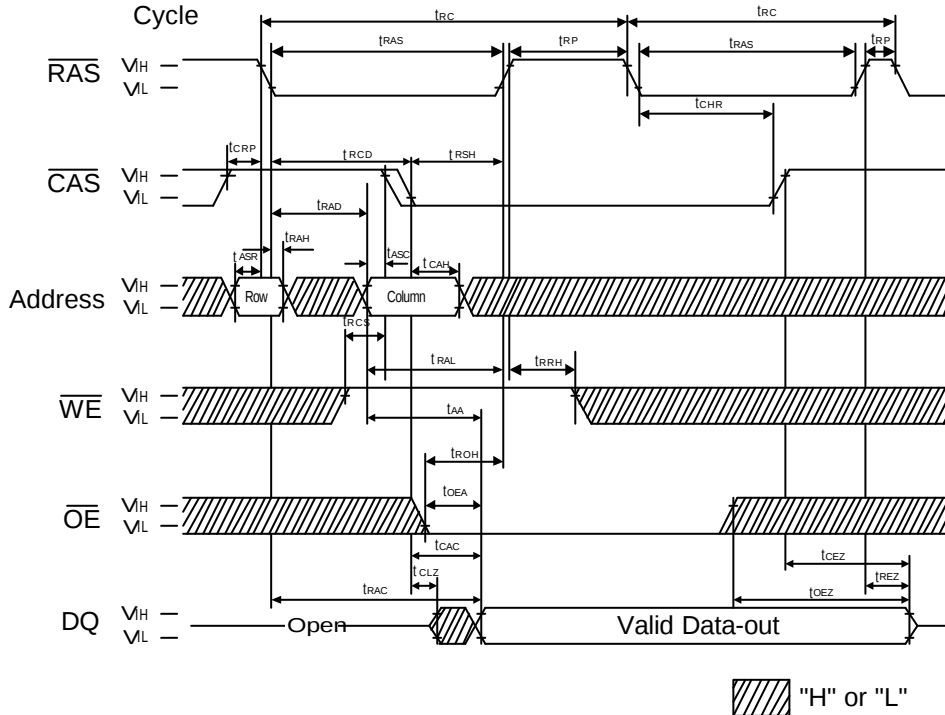
## Fast Page Mode Read Modify Write Cycle

 $\overline{\text{RAS}}$ -only Refresh CycleNote:  $\overline{\text{WE}}, \overline{\text{OE}}$  = "H" or "L" "H" or "L"

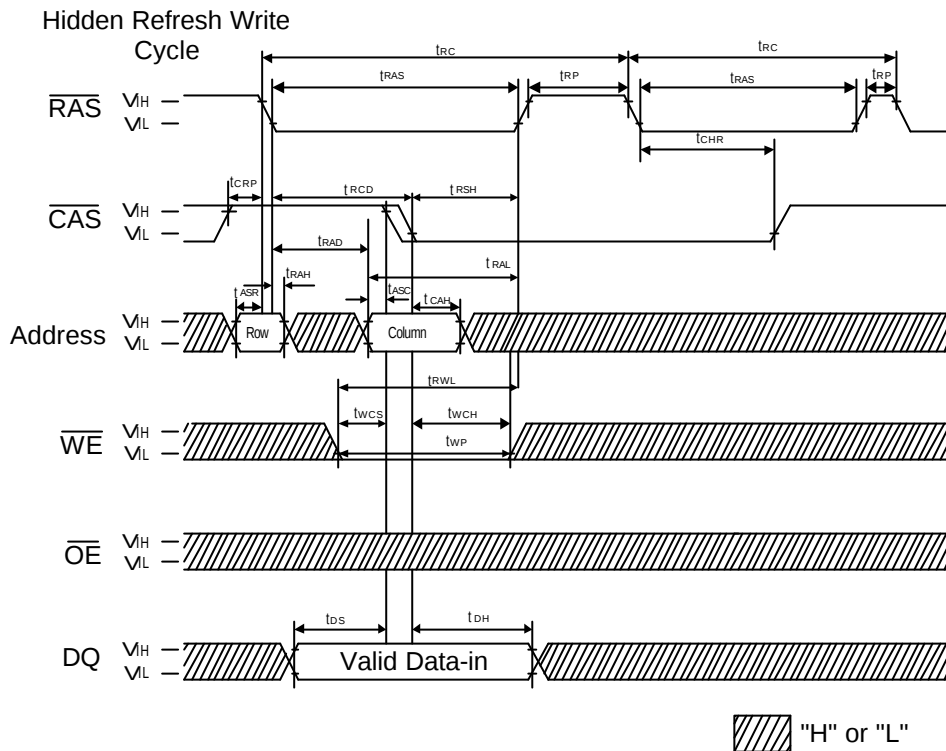
$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle

Note:  $\overline{\text{OE}}$ , Address="H" or "L"  "H" or "L"

## Hidden Refresh Read Cycle



 "H" or "L"



# NT511740D5J

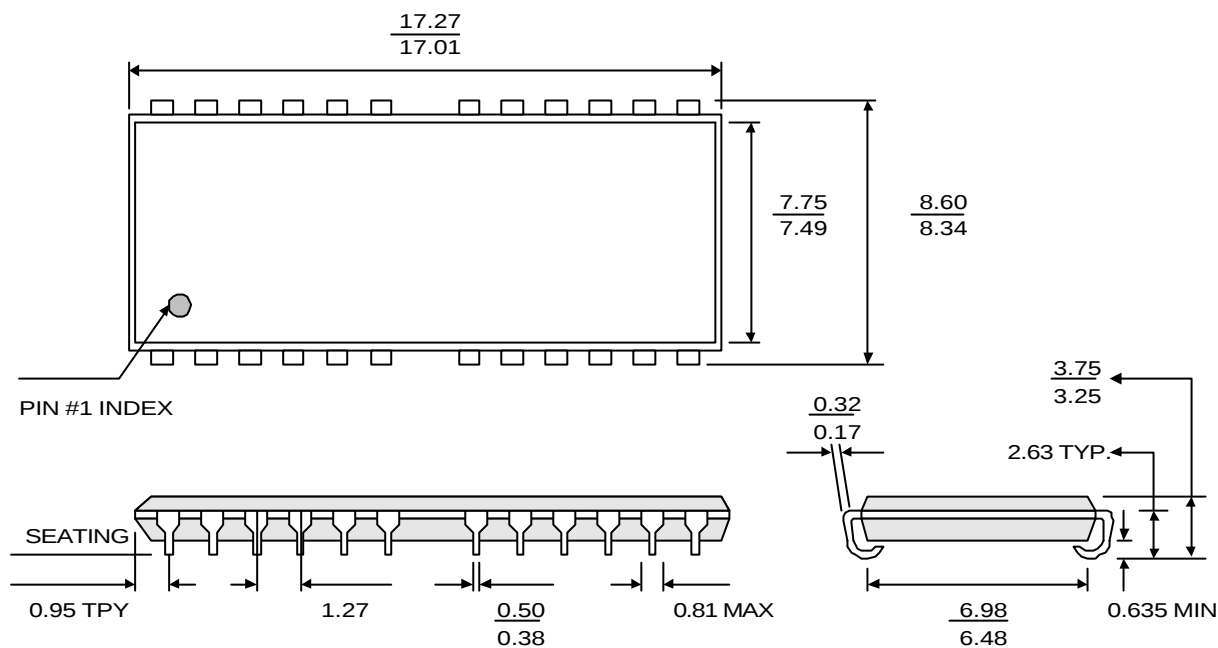
16MEG : x4

CMOS with Extended Data Out



## PACKAGE DIMENSION

24/26-PIN PLASTIC SOJ (300mil)



**NOTE :** All dimensions in millimeters <sup>MAX</sup> or typical where noted.