User's Guide

TPS40074 Buck Controller Evaluation Module User's Guide

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1 Introduction

The TPS40074EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.5-V output at up to 15 A from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40074 high frequency controller with remote sense.

1.1 Description

The TPS40074EVM-001 is designed to use a regulated 12-V (between 10-V and 14-V) bus to produce a high current, regulated 1.5-V output at up to 15 A of load current. The TPS40074EVM-001 is design to demonstrate the TPS40074 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40074 in a given application. The EVM can be modified to support output voltages from 0.9 V to 3.3 V by changing a single resistor. The TPS40074EVM-001 has been built to the sample application used in the *TPS40074 Midrange Input Synchronous Buck Controller With Voltage Feed-Forward Data Sheet*, except the switching frequency has been lowered to 400 kHz to reduce switching losses in the power FETs, and the R_{KFF} resistor (R10) increased to maintain the UVLO level.

1.2 Applications

- Non-isolated medium current point of load and low voltage bus converters
- Merchant power modules
- Networking equipment
- Telecommunications equipment
- DC power distributed systems

1.3 Features

- 10-V to 14-V input range
- 1.5-V fixed output, adjustable with single resistor
- 15-A_{DC} steady state output current
- 400-kHz switching frequency
- Single main switch MOSFET and single synchronous rectifier MOSFET single
- Component side, surface mount design on a 3-inch × 3-inch evaluation board
- Four-layer PCB with all components on the top side
- Convenient test points for probing critical waveforms and non-invasive loop response testing

2 TPS40074EVM-001 Electrical Performance Specifications

Table 2-1. TPS40074EVM-001 Electrical and Performance Specifications

PARAMETER	NOTES AND CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range			10		14	V
Max input current	V_{IN} = 10 V, I_{OUT} = 15 A			2.75		A
No-load input current	V_{IN} = 14 V, I_{OUT} = 0 A			45		mA
OUTPUT CHARACTERISTICS						
Output voltage	R6 = 9.53 k, R5 = 105 k		1.45	1.50	1.55	V
Output voltage regulation	Line regulation (10 V < V_{IN} < 14 V, I_{OUT} = 5 A)				1%	
	Load regulation (10 V < I_{OUT} < 15 A, V_{IN} = 12 V)				1%	
Output voltage ripple	V_{IN} = 14 V, I_{OUT} = 15 A			25	50	mVpp
Output load current			0		15	A
Output over current				23		A
SYSTEM CHARACTERISTICS						
Switching frequency			360	400	440	kHz
Peak efficiency	V_{OUT} = 1.5 V, 8 A < I_{OUT} < 12 A	V_{12V_IN} = 10 V		87%		
		V_{12V_IN} = 12 V		85%		
		V_{12V_IN} = 14 V		83%		

Table 2-1. TPS40074EVM-001 Electrical and Performance Specifications (continued)

PARAMETER	NOTES AND CONDITIONS		MIN	TYP	MAX	UNIT
Full load efficiency	V_{OUT} = 1.5 V, I_{OUT} = 15 A	V_{12V_IN} = 10 V		84%		
		V_{12V_IN} = 12 V		83%		
		V_{12V_IN} = 14 V		81%		

3 Schematic

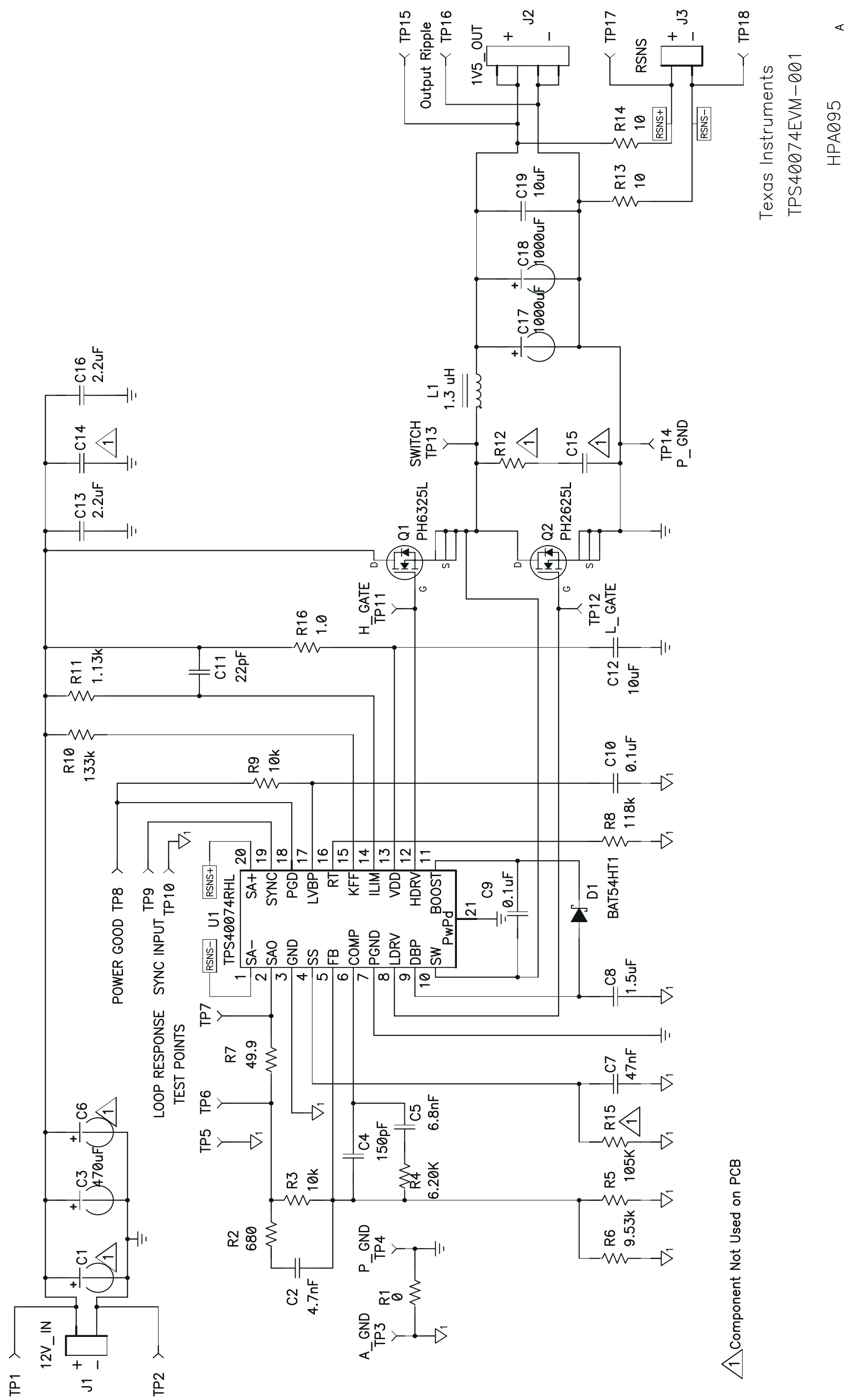

Figure 3-1. TPS40074EVM-001 Power Stage/Control Schematic Reference Only, See Table 3 for Specific Values

3.1 Adjusting Output Voltage (R5 and R6)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R6 and R5). The output voltage is given by Equation 1.

$$V_{VOUT} = V_{VREF} \times \frac{R5 + R65 + R3}{R5 + R6} \qquad (1)$$

where

- V_{VREF} = 0.700 V
- R3 = 10.0 kΩ

Table 3-1 contains common values for R6 to generate popular output voltages with R5 open R5 can be used to increase the accuracy that can be obtained without using more expensive resistors. The TPS40074EVM-001 is stable through these output voltages but the efficiency can suffer as the power stage is optimized for the 1.5-V output.

Table 3-1. Adjusting V_{1V5_OUT} With R14

VOUT	R16
3.3 V(1)	2.67 K
2.5 V(1)	3.83 K
2.2 V(1)	4.64 K
2.0 V(1)	8.36 K
1.8 V	6.34 K
1.5 V	8.66 K
1.2 V	14.0 K

(1) Due to higher duty cycles associated with higher output voltages or lower input voltages, output current should be limited to 10 A when operating with output voltages greater than 2.0 V or input voltages below 6 V to reduce conduction losses in the main switching FET (Q1). Under these conditions, a lower R_{dsON} FET would normally be selected.

3.2 Using Remote Sense (J3)

The TPS40074EVM-001 provides the user with remote sense capabilities through the connector J3. When remote sense is used, J3 should be connected at the load to provide more accurate load regulation by compensating for losses over the terminal connections and load wire connections. When remote sense is connected the output voltage measured between TP15 and TP16 can show a positive load regulation characteristic (increasing output voltage with increasing load). This is the result of the compensation of the controller of resistive losses between the local sense voltage (TP15 and TP16) and the remote sense connection (J3). TP17 and TP18 are connected to the remote sense lines and thus will show the voltage at the load when remote sense is connected.

Excessive phase shift from inductive components in the load or remote sense connections can cause instability if care is not taken to minimize these parasitic effects in the remote sense line. A twisted pair of insulated cables from the load connection to J3 is preferred to minimize noise injection and inductance in the remote sense line. In a device layout, care should be taken to shield the remote sense line from high-noise, high-current, or digital signals to limit noise injection into the feedback path and provide the most accurate regulation possible.

3.3 5V Input Operation (R10 and R15)

To operate with a 5-V input, two resistors need to be changed. R10 (RKFF) sets the voltage ramp amplitude and needs to be reduced to 53.6 kΩ to lower the UVLO to 3.9 V for 5-V operation. In addition, a 330-kΩ resistor should be added at R15 to prevent an internal race condition during soft start.[1]

[1] Due to higher duty cycles associated with higher output voltages or lower input voltages, output current should be limited to 10 A when operating with output voltages greater than 2.0 V or input voltages below 6 V to reduce conduction losses in the main switching FET (Q1). Under these conditions, a lower RdsON FET would normally be selected.

4 Test Setup

4.1 Equipment

4.1.1 Voltage Source

V_{12V_IN}

The input voltage source (V_{12V_IN}) should be a 0-V to 15-V variable DC source capable of 5 A_{DC}. Connect V_{12V_IN} to J1 as shown in Figure 4-2.

4.1.2 Meters

A1: 0 A_{DC} 5 A_{DC}, ammeter

V1: V_{12V_IN}, 0-Vto 15-V voltmeter

V2: V_{1V5_OUT} 0-V to 5-V voltmeter

4.1.3 Loads

LOAD1

The output load (LOAD1) should be an electronic constant current mode load capable of 0 A_{DC}–15 A_{DC} at 1.5 V.

4.1.4 Recommended Wire Gauge

V_{12V_IN} to J1

The connection between the source voltage, V12V_IN, and J1 of HPA095 can carry as much as 3 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than four feet (2-feet input, 2-feet return).

J2 to LOAD1 (Power)

The power connection between J2 of HPA095 and LOAD1 can carry as much as 15 A_{DC}. The minimum recommended wire size is 2× AWG #16, with the total length of wire less than four feet (2-feet output, 2-feet return).

J3 to LOAD1 (Remote Sense)

If remote sense is used, the remote sense connection between J3 of HPA095 and LOAD1 can carry less than 1 A_{DC}. The minimum recommended wire size is AWG #22, with the total length of wire less and four feet (2-feet output, 2-feet return).

4.1.5 Other

FAN

This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200–400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered or probed while the fan is not running.

OSCILLOSCOPE

A 60-MHz or faster oscilloscope can be used to determine the ripple voltage on 1V5_OUT. The oscilloscope should be set for the following to take output ripple measurements:

- 1-MΩ impedance
- AC coupling
- 1-µs/division horizontal resolution
- 20-mV/division vertical resolution

TP15 and TP16 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP15 and holding the ground barrel to TP16 as shown in Figure 4-2. For a hands-free approach, the loop in TP16 can be cut and opened to cradle the probe barrel. Using a leaded ground connection can induce additional noise due to the large ground loop area.

4.2 Equipment Setup

Figure 4-2 shows the basic recommended test setup to evaluate the TPS40074EVM-001. Note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 4-1.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. An electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{12V_IN}, it is advisable to limit the source current from V_{12V_IN} to 5.0-A maximum. Make sure V_{12V_IN} is initially set to 0 V and connected as shown in Section 4.2.2.
3. Connect the ammeter A1 (0-A to 5-A range) between V_{12V_IN} and J1 as shown in Figure 4-1.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 4-1.
5. Connect LOAD1 to J2 as shown in Figure 3-1. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{12V_IN} is applied.
6. Connect voltmeter, V2 across TP17 and TP18 as shown in Figure 4-1.
7. Connect an oscilloscope probe to TP16 and TP15 as shown in Figure 4-2.
8. Place a fan as shown in Figure 4-1. Turn it on, making sure air is flowing across the EVM.

4.2.2 Diagram

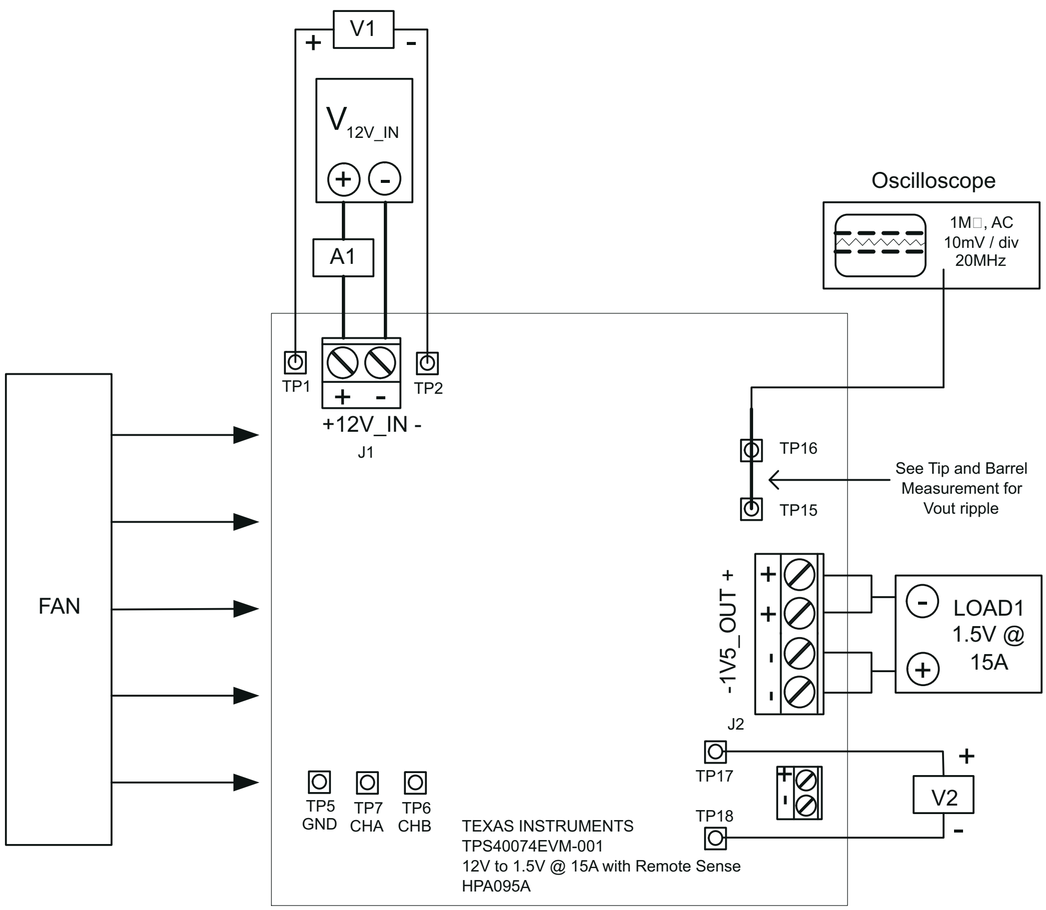

Figure 4-1. TPS40074EVM-001 Recommended Test Setup

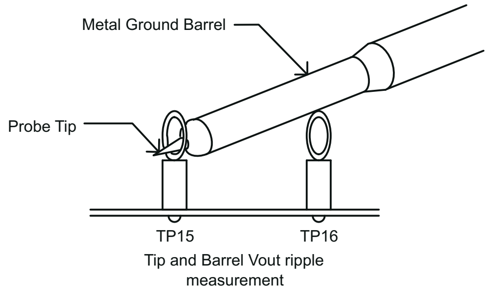

Figure 4-2. Output Ripple Measurement – Tip and Barrel using TP15 and TP16

4.3 Start-Up/Shutdown Procedure

1. Increase V_{12V_IN} (V1) from 0 V to 10 V_{DC}.
2. Vary LOAD1 from 0 A–10 A_{DC}.
3. Vary V_{12V_IN} (V1) from 10 V_{DC} to 14 V_{DC}.
4. Decrease LOAD1 to 0 A.
5. Decrease V_{12V_IN} to 0 V.

4.4 Equipment Shutdown

1. Shut down the oscilloscope.
2. Shut down LOAD1.
3. Shut down V_{12V_IN}.
4. Shut down FAN.

5 TPS40074EVM Typical Performance Data and Characteristic Curves

Figure 5-1 through Figure 6-2 present typical performance curves for the TPS40074EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

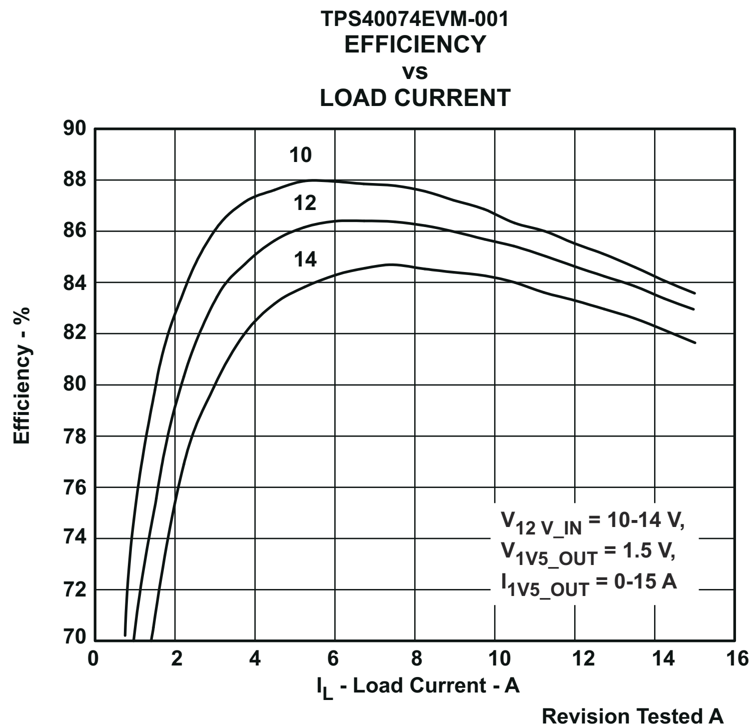

Figure 5-1. TPS40074EVM-001 Efficiency V_{12V_IN} = 10 V–14 V, V_{1V5_OUT} = 1.5 V, I_{1V5_OUT} = 0 A–15 A

5.2 Line and Load Regulation

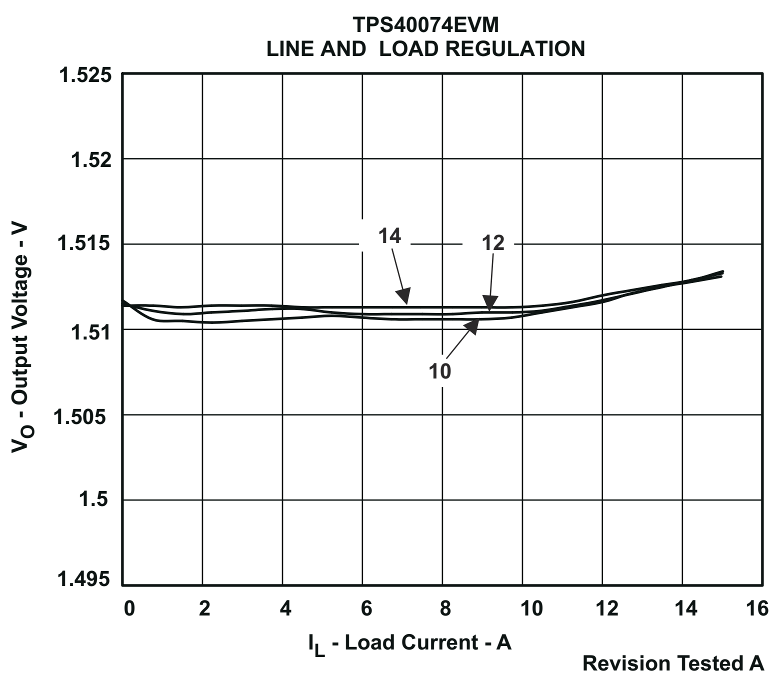

Figure 5-2. TPS40074EVM-001 Line and Load Regulation – ±1% Window

6 EVM Assembly Drawings and Layout

Figure 6-1 through Figure 6-6 show the design of the TPS40074EVM-001 printed circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board 3.0 inch × 3.0 inch with all components on the top side to allow the user to easily view, probe, and evaluate the TPS40074 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

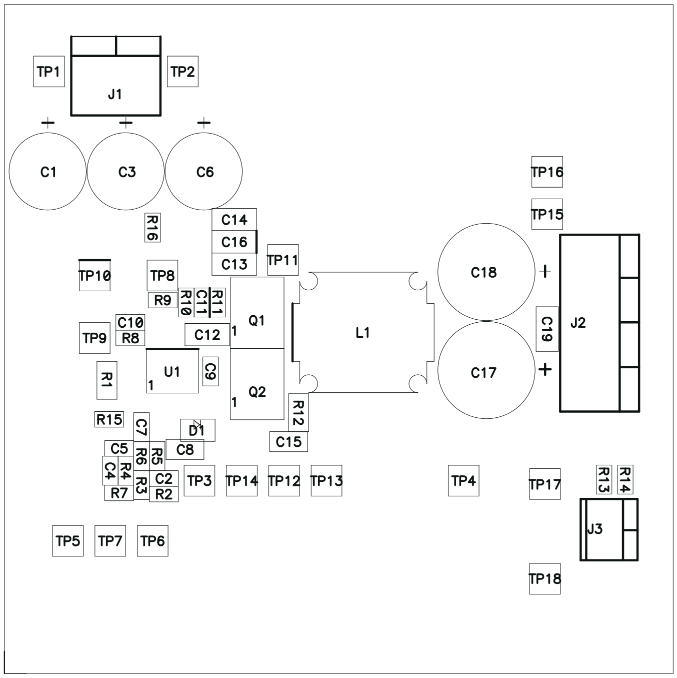

Figure 6-1. TPS40074EVM-001 Component Placement (Viewed from Top)

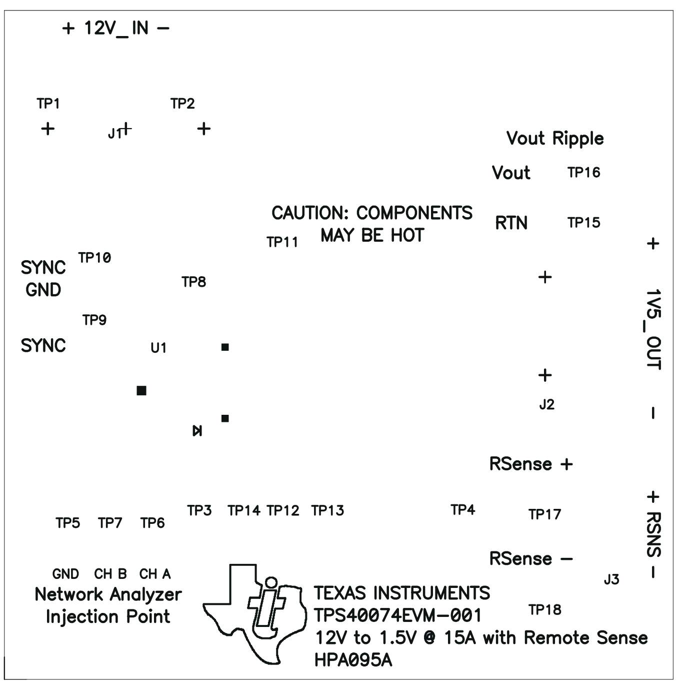

Figure 6-2. TPS40074EVM-001 Silkscreen (Viewed from Top)

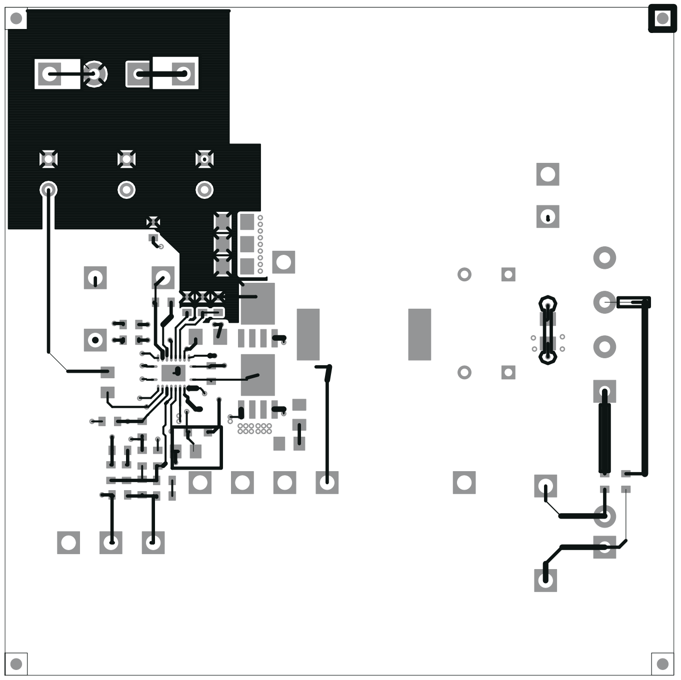

Figure 6-3. TPS40074EVM-001 Top Copper (Viewed from Top)

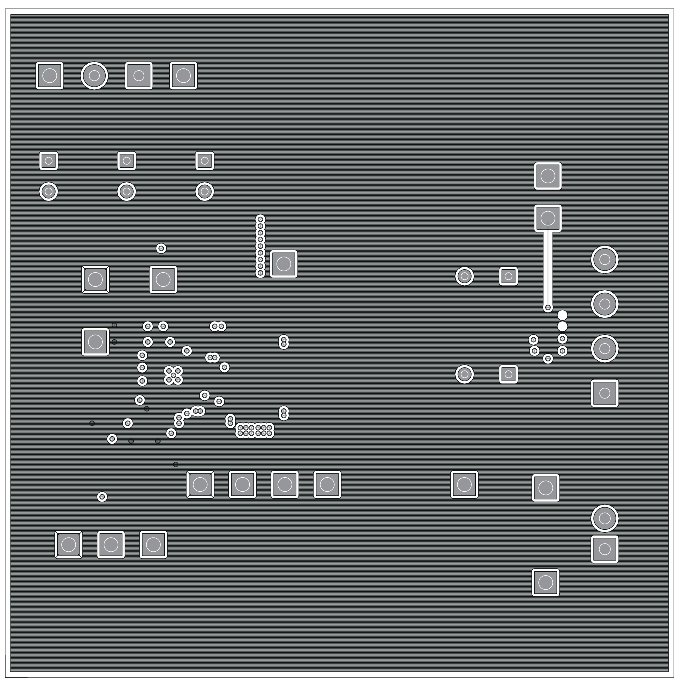

Figure 6-4. TPS40074EVM-001 Layer 2 (X-Ray View from Top)

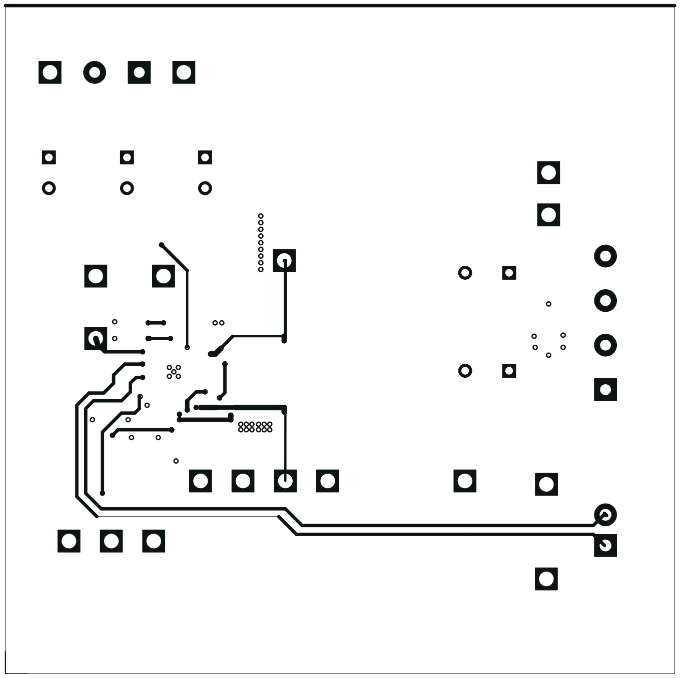

Figure 6-5. TPS40074EVM-001 Layer 3 (X-Ray View from Top)

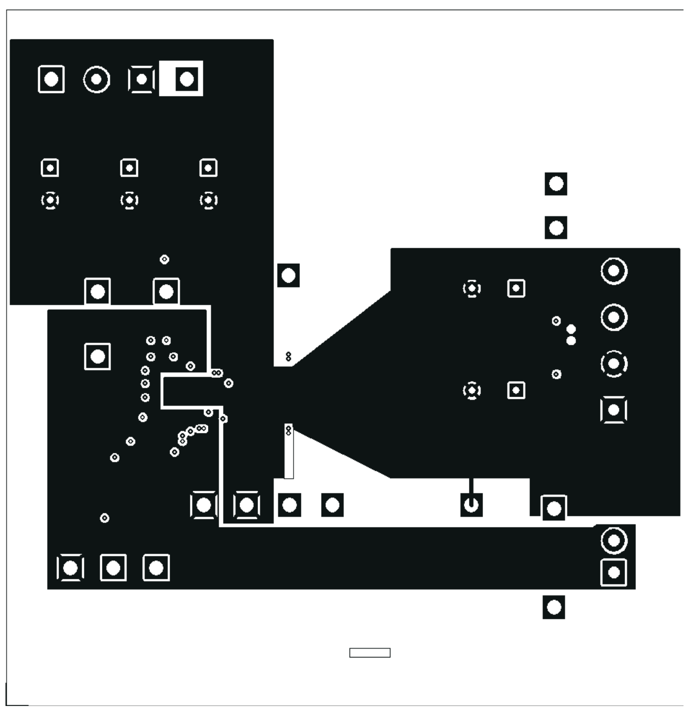

Figure 6-6. TPS40074EVM-001 Bottom Copper (X-Ray View from Top)

7 List of Materials

Table 7-1 lists the EVM components as configured according to the schematic shown in Figure 3-1 and Figure 4-1.

Table 7-1. TPS40074EVM-001 Bill of Materials

Count	RefDes	Description	Size	Mfr	Part Number
0	C1, C6	Capacitor, 470 µF, 16 V, 21 mΩ, 25%	8mm	Panasonic	EEUFL1C470U
1	C3	Capacitor, 470 µF, 16 V, 21 mΩ, 25%	8mm	Panasonic	EEUFL1C470U
1	C2	Capacitor, ceramic, 4700 pF, 50 V, X7R, 10%	0603	Std	Std
1	C4	Capacitor, ceramic, 150 pF, 50 V, X7R, 10%	0603	Std	Std
1	C5	Capacitor, ceramic, 6800 pF, 50 V, X7R, 10%	0603	Std	Std
1	C7	Capacitor, ceramic, 0.047 µF, 50 V, X7R, 10%	0603	Std	Std
1	C8	Capacitor, ceramic, 1.5 µF, 16 V, X7R, 20%	0805	TDK	C2012X7R1C115M
2	C9, C10	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 20%	0603	Std	Std
1	C11	Capacitor, ceramic, 22 pF, 50 V, NPO, 10%	0603	Std	Std
1	C12	Capacitor, ceramic, 10 µF, 16 V, X7R, 20%	1206	TDK	C3216X7R1C106M
2	C13, C16	Capacitor, ceramic, 2.2 µF, 16 V, X7R, 10%	1206	Std	Std
0	C14	Capacitor, ceramic, 2.2 µF, 16 V, X7R, 10%	1206	Std	Std
0	C15	Capacitor, ceramic, 1000 pF, 25 V, X7R, 20%	0805	Std	Std
2	C17, C18	Capacitor, 1000 µF, 10 V, 16 mΩ, 25%	8mm	Panasonic	EEUFL1A102U
1	C19	Capacitor, Ceramic, 10 µF, 6.3 V, X5R, 20%	1206	Std	Std
1	D1	Diode, Schottky, 200 mA, 30 V	SOD323	On-Semi	BAT54HT1
1	J1	Terminal Block, 2-pin, 15 A, 5,1 mm	0.40 × 0.35	OST	ED1609
1	J2	Terminal Block, 4-pin, 15 A, 5,1 mm	0.80 × 0.35	OST	ED2227
1	J3	Terminal Block, 2-pin, 6 A, 3,5 mm	0.27 × 0.25	OST	ED1514A
1	L1	Inductor, SMT, 1.3 µH, 26 A, 2 mΩ	0.51 × 0.51	Pulse	PG0077.142
1	Q1	Mosfet, N-Ch, 25 V, 81.4 A, 8.9 mΩ	LFPAK	Philips	PH6325L
1	Q2	Mosfet, N-Ch, 25 V, 118 A, 4.1 mΩ	LFPAK	Philips	PH2625L
1	R1	Resistor, Chip, 0-Ω jumper, 1/10-W, 5%	0805	Std	Std
1	R2	Resistor, Chip, 680 Ω, 1/16-W, 1%	0603	Std	Std
2	R3,R9	Resistor, Chip, 10 kΩ, 1/16-W, 1%	0603	Std	Std
1	R4	Resistor, Chip, 6.20 kΩ, 1/16-W, 1%	0603	Std	Std
1	R5	Resistor, Chip, 105 kΩ, 1/16-W, 1%	0603	Std	Std
1	R6	Resistor, Chip, 9.53 kΩ, 1/16-W, 1%	0603	Std	Std
1	R7	Resistor, Chip, 49.9 Ω, 1/16-W, 1%	0603	Std	Std
1	R8	Resistor, Chip, 118 kΩ, 1/16-W, 1%	0603	Std	Std
1	R10	Resistor, Chip, 133 kΩ, 1/16-W, 1%	0603	Std	Std
1	R11	Resistor, Chip, 1.13 kΩ, 1/16-W, 1%	0603	Std	Std
0	R12	Resistor, Chip, 3.3 Ω, 1/10-W, 1%	0805	Std	Std
2	R13, R14	Resistor, Chip, 10 Ω, 1/16-W, 1%	0603	Std	Std
0	R15	Resistor, Chip, Ω, 1/16-W, 1%	0603	N/A	N/A
1	R16	Resistor, Chip, 1.0 Ω, 1/16-W, 1%	0603	Std	Std
3	TP1, TP15, TP17	Test Point, Red, Thru Hole	0.125 × 0.125	Keystone	5010
8	TP2–TP5, TP10, TP14, TP16, TP18	Test Point, Black, Thru Hole	0.125 × 0.125	Keystone	5011
7	TP6–TP9, TP11–TP13	Test Point, White, Thru Hole	0.125 × 0.125	Keystone	5012
1	U1*	IC	QFN-20	TI	TPS40074RHL
1	—	PCB, 4-Layer FR4, 3.0 inch × 3.0 inch × 0.062 inch	2.4 inch × 2.1 inch	Any	HPA095A
4	—	Bumpon, Transparent	0.44 inch × 0.2 inch	3M	SJ5303

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

Table 7-1. TPS40074EVM-001 Bill of Materials (continued)

Count	RefDes	Description	Size	Mfr	Part Number
4. Install Bumpons on back side(unpopulated side) of PCB. Install one in each corner after cleaning.					
5. Ref designators marked with an * cannot be substituted. All other components can be substituted with equivalent components of MFG.					

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2006) to Revision A (January 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title.. 2