



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE- LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8806I	±1	±1	DB-28 (SSOP)	–40°C to +85°C	DAC8806	DAC8806IDB	Tubes, 48
						DAC8806IDBR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted)

		DAC8806	UNIT
V_{DD} to GND		–0.3 to +7	V
Digital input voltage to GND		–0.3 to $+V_{DD} + 0.3$	V
$V(I_{OUT})$ to GND		–0.3 to $+V_{DD} + 0.3$	V
Operating temperature range		–40 to +85	°C
REF, R_{OFS} , R_{FB} , R1, R_{COM} to AGND, and DGND		±25	V
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+125	°C
Power dissipation		$(T_J \text{ max} - T_A)/R_{\theta JA}$	W
Thermal impedance, $R_{\theta JA}$		55	°C/W
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at -40°C to $+85^{\circ}\text{C}$, $V_{\text{DD}} = +2.7\text{ V}$ to $+5.5\text{ V}$, $I_{\text{OUT}} = \text{virtual GND}$, $\text{GND} = 0\text{ V}$, $V_{\text{REF}} = 10\text{ V}$, and $T_{\text{A}} = \text{full operating temperature}$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8806			UNITS		
		MIN	TYP	MAX			
STATIC PERFORMANCE							
Resolution		14			Bits		
Relative accuracy	DAC8806	±1			LSB		
Differential nonlinearity		±0.5			LSB		
Output leakage current	Data = 0000h, T _A = +25°C	5			nA		
Output leakage current	Data = 0000h, T _A = T _{MAX}	10			nA		
Full-scale gain error	Unipolar, data = 3FFFh	1			±4	LSB	
	Bipolar, data = 3FFFh	1			±4	LSB	
Full-scale temperature coefficient		1			2	ppm/°C	
Bipolar zero scale error		±1			±3	LSB	
PSRR	Power-supply rejection ratio; V _{DD} = 5 V ±10%	±0.1			±1	LSB/V	
OUTPUT CHARACTERISTICS ⁽¹⁾							
Output current		1.66			mA		
Output capacitance	Code dependent	50			pF		
REFERENCE INPUT							
V _{REF} range		−15			15	V	
R _{REF}	Input resistance (unipolar)	4.5			6	7.5	kΩ
Input capacitance		5			pF		
R1/R2	R1/R2 resistance (bipolar)	9			12	15	kΩ
R _{OFS} , R _{FB}	Feedback and offset resistance	9			12	15	kΩ
LOGIC INPUTS AND OUTPUT ⁽¹⁾							
Input low voltage	V _{IL} V _{DD} = +2.7 V	0.6			V		
	V _{IL} V _{DD} = +5 V	0.8			V		
Input high voltage	V _{IH} V _{DD} = +2.7 V	2.1			V		
	V _{IH} V _{DD} = +5 V	2.4			V		
Input leakage current	I _{IL}	0.001			1	μA	
Input capacitance	C _{IL}	8			pF		
INTERFACE TIMING, V _{DD} = +5.0V ⁽¹⁾ (See Figure 40 and Table 1)							
	t _{DS} Data to $\overline{\text{WR}}$ setup time	20			ns		
	t _{DH} Data to $\overline{\text{WR}}$ hold time	0			ns		
	t _{WR} $\overline{\text{WR}}$ pulse width	20			ns		
	t _{LDAC} LDAC pulse width	20			ns		
Data setup time	t _{RST} $\overline{\text{RST}}$ pulse width	20			ns		
Data hold time	t _{LWD} $\overline{\text{WR}}$ to LDAC delay time	0			ns		
INTERFACE TIMING, V _{DD} = +2.7V ⁽¹⁾ (See Figure 40 and Table 1)							
	t _{DS} Data to $\overline{\text{WR}}$ setup time	35			ns		
	t _{DH} Data to $\overline{\text{WR}}$ hold time	0			ns		
	t _{WR} $\overline{\text{WR}}$ pulse width	35			ns		
	t _{LDAC} LDAC pulse width	35			ns		
Data setup time	t _{RST} $\overline{\text{RST}}$ pulse width	35			ns		
Data hold time	t _{LWD} $\overline{\text{WR}}$ to LDAC delay time	0			ns		

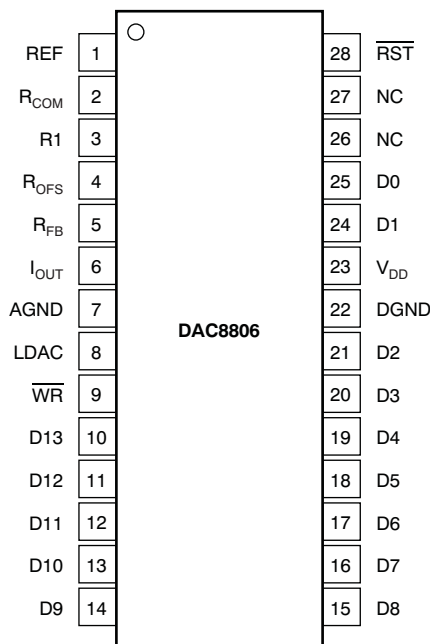
(1) Specified by design and characterization; not production tested.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at -40°C to $+85^{\circ}\text{C}$, $V_{\text{DD}} = +2.7\text{ V}$ to $+5.5\text{ V}$, $I_{\text{OUT}} = \text{virtual GND}$, $\text{GND} = 0\text{ V}$, $V_{\text{REF}} = 10\text{ V}$, and $T_{\text{A}} = \text{full operating temperature}$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8806			UNITS
		MIN	TYP	MAX	
POWER REQUIREMENTS					
V _{DD}		2.7		5.5	V
I _{DD} (normal operation)	Logic inputs = 0V			5	μA
V _{DD} = +4.5 V to +5.5 V	V _{IH} = V _{DD} and V _{IL} = GND		3	5	μA
V _{DD} = +2.7 V to +3.6 V	V _{IH} = V _{DD} and V _{IL} = GND		1	2.5	μA
AC CHARACTERISTICS ⁽²⁾					
Output current settling time			0.5		μs
Reference multiplying BW	V _{REF} = 5 V _{PP} , Data = 3FFFh		8		MHz
DAC glitch impulse	V _{REF} = 0 V to 10 V, Data = 1FFFh to 2000h to 1FFFh		2		nV–s
Feedthrough error V _{OUT} /V _{REF}	Data = 0000h, V _{REF} = 10 kHz; ±10 V _{PP}		–70		dB
Digital feedthrough	L _{DAC} = logic low, V _{REF} = –10 V to +10 V Any code change		2		nV–s
Total harmonic distortion	V _{REF} = 6 V _{RMS} , Data = 3FFF, f = 1 kHz		–105		dB
Output spot noise voltage			10		nV/√Hz

(2) Specified by design and characterization; not production tested.

PIN ASSIGNMENTS**TERMINAL FUNCTIONS**

PIN #	NAME	DESCRIPTION
1	REF	Reference input and 4-quadrant Resistor (R2).
2	R_{COM}	Center tap of two 4-quadrant resistors (R1 and R2).
3	R1	4-quadrant resistor (R1).
4	R_{OFS}	Bipolar offset resistor
5	R_{FB}	Internal matching feedback resistor
6	I_{OUT}	DAC current output
7	AGND	Analog ground
8	LDAC	Digital input load DAC control. When LDAC is high, data is loaded from input register into a DAC register, updating the DAC output.
9	$\overline{\text{WR}}$	Write control digital input. Active low. When $\overline{\text{WR}}$ is taken to logic low, data is loaded from the digital input pins (D0–D13) into a14-bit input register.
10–21	D13–D2	Digital input data bits. D13 is MSB.
22	DGND	Digital ground
23	V_{DD}	Positive power supply
24, 25	D1, D0	Digital Input data bits. D0 is LSB.
26, 27	NC	No connection
28	$\overline{\text{RST}}$	Reset. Active low. When $\overline{\text{RST}}$ is taken to logic low, the DAC register is set to zero code, resulting in the DAC output being set to 0 V.

TYPICAL CHARACTERISTICS: $V_{DD} = +5V$

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

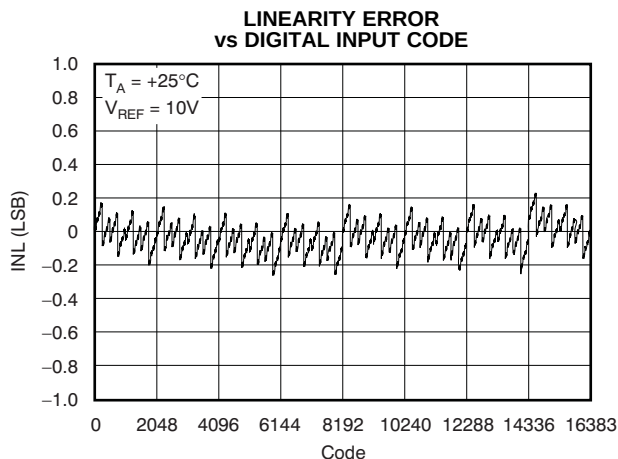


Figure 1.

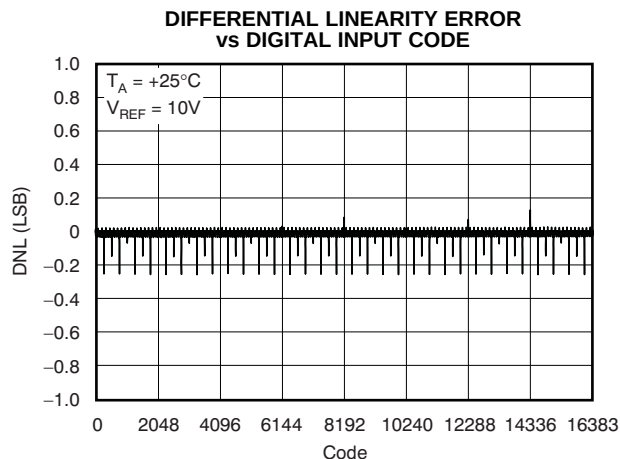


Figure 2.

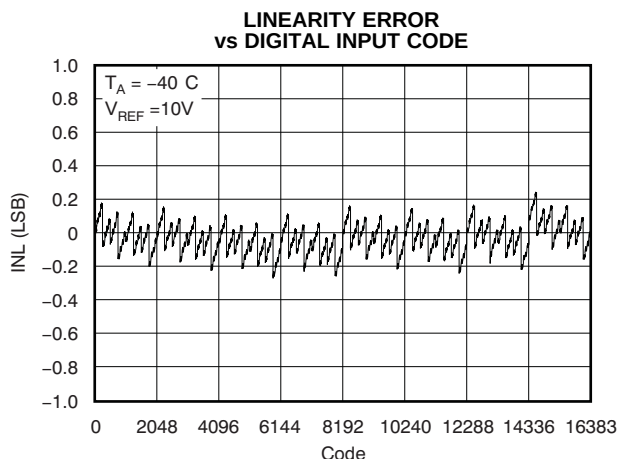


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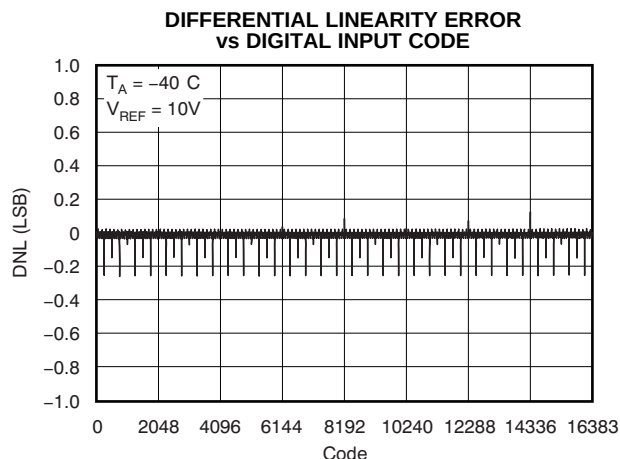


Figure 4.

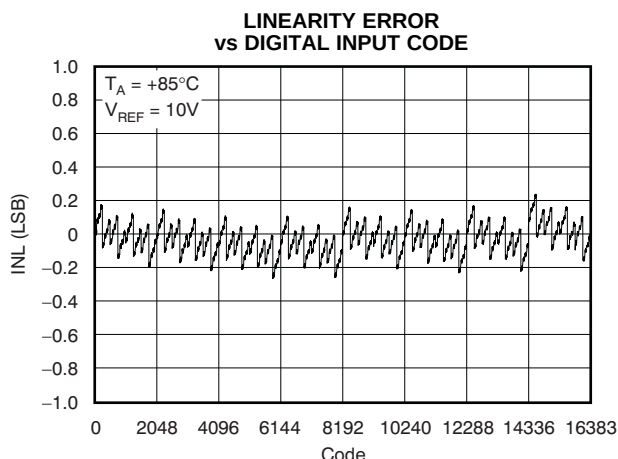


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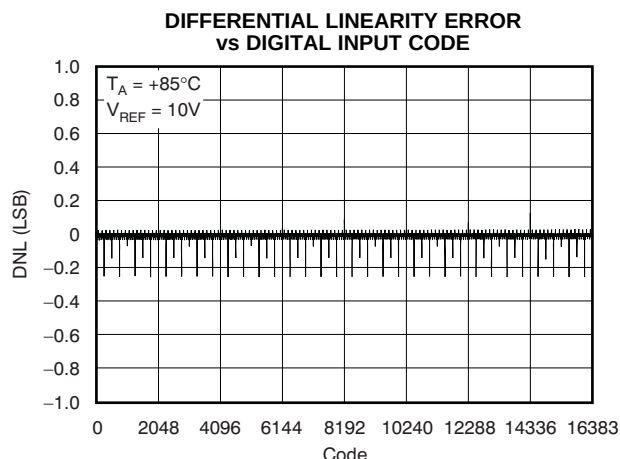
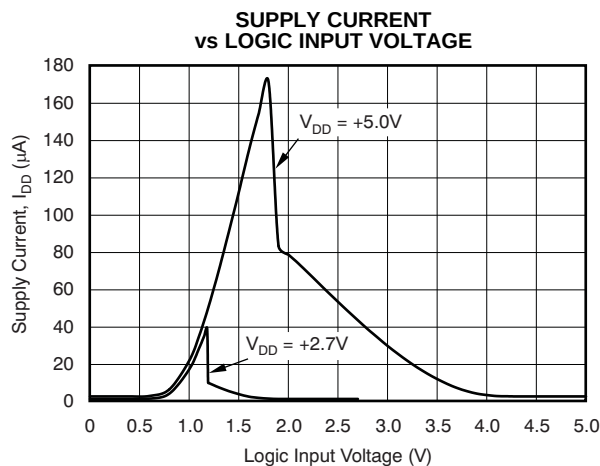
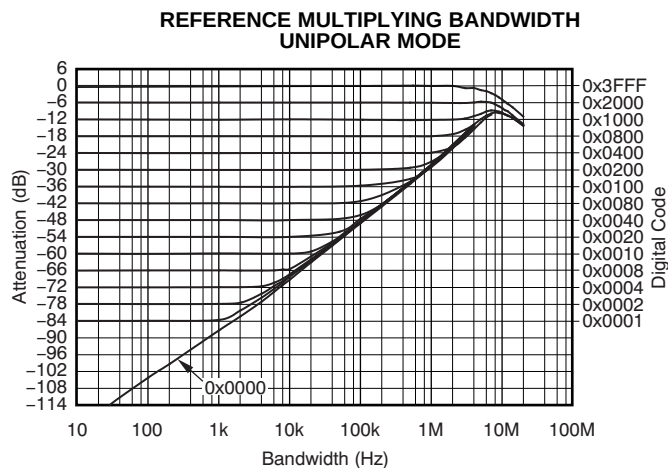
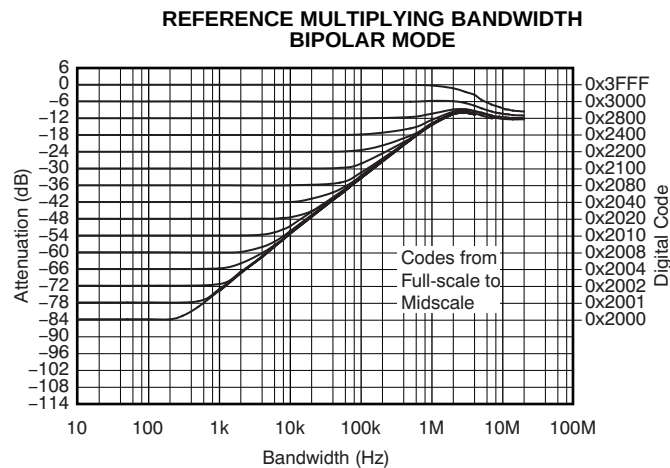
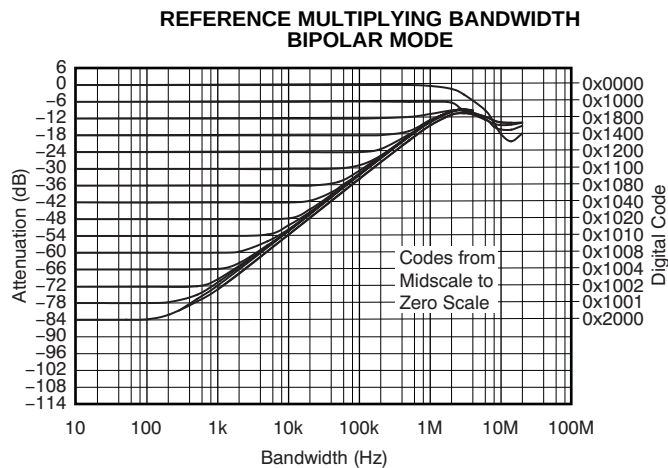
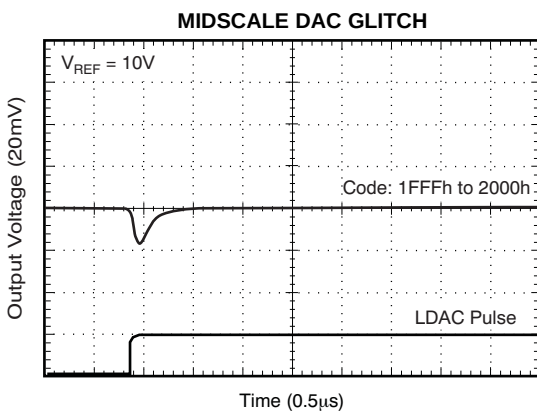
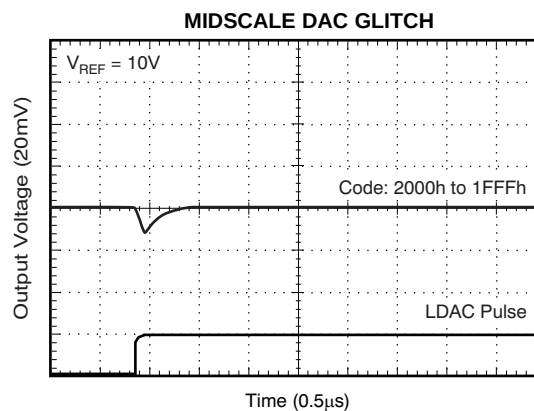
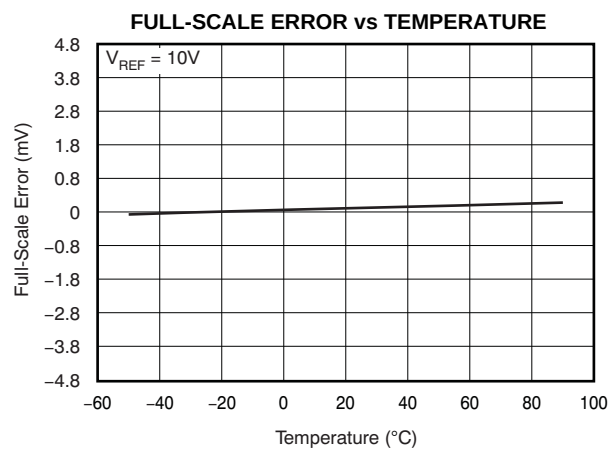
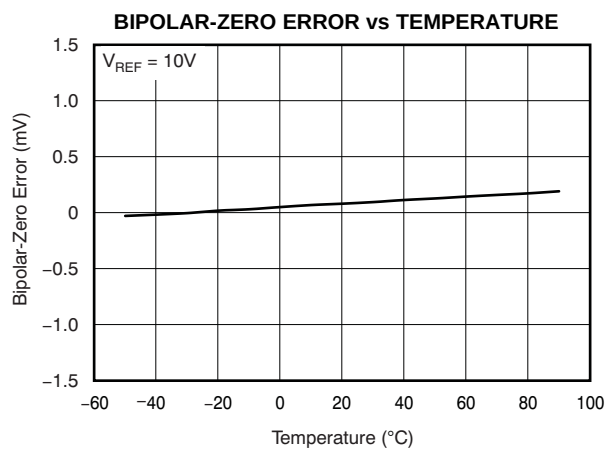


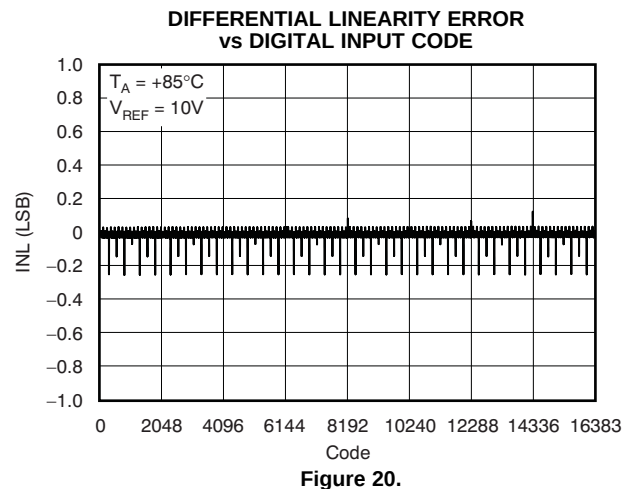
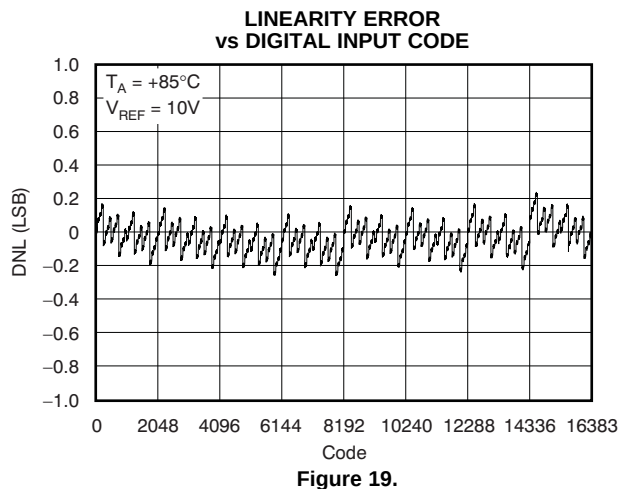
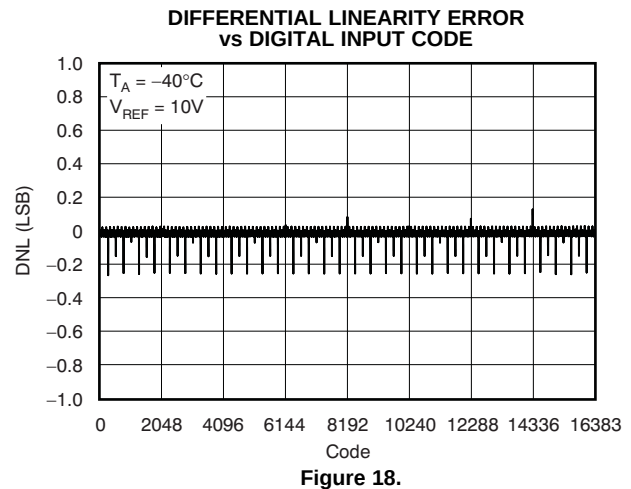
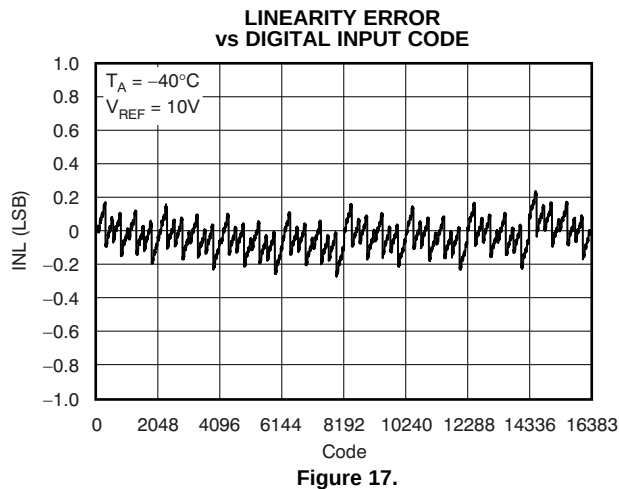
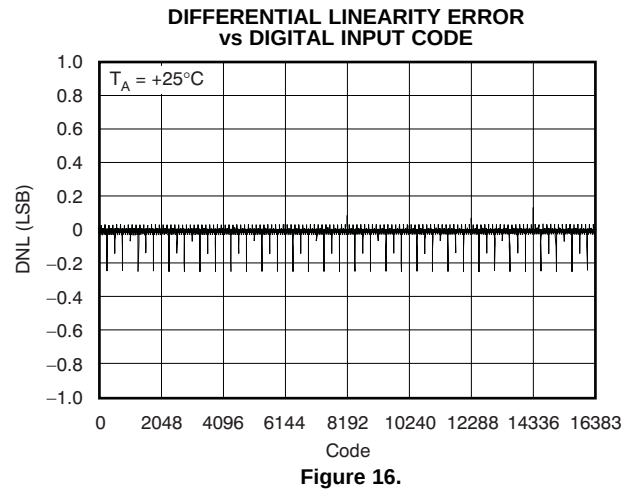
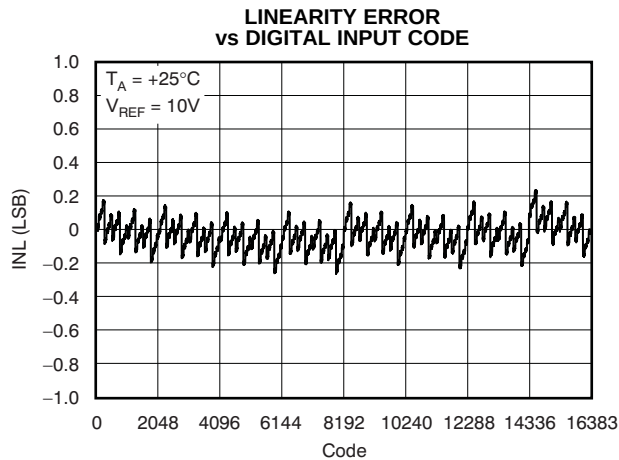
Figure 6.

TYPICAL CHARACTERISTICS: $V_{DD} = +5V$ (continued)At $T_A = +25^\circ C$, unless otherwise noted.**Figure 7.****Figure 8.****Figure 9.****Figure 10.****Figure 11.****Figure 12.**

TYPICAL CHARACTERISTICS: $V_{DD} = +5V$ (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

**Figure 13.****Figure 14.**

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7V$ At $T_A = +25^\circ\text{C}$, unless otherwise noted.

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7V$ (continued)

At $T_A = +25^\circ C$, unless otherwise noted.

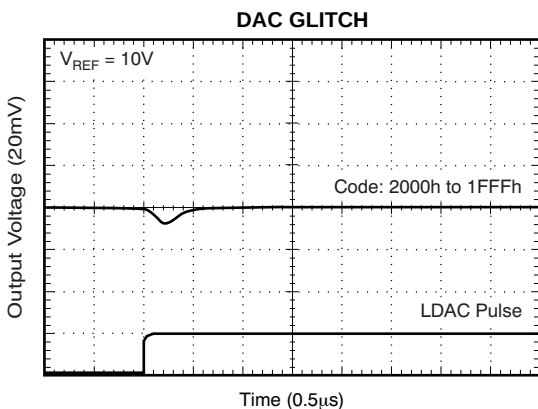


Figure 21.

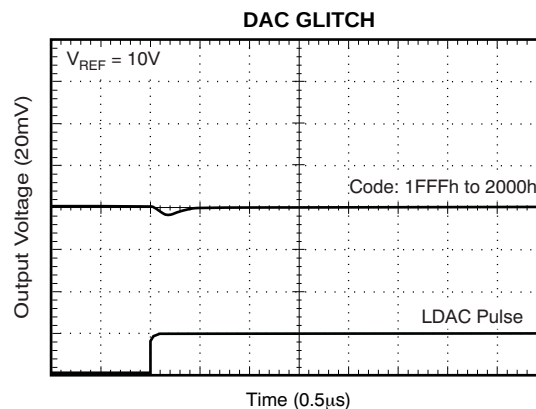


Figure 22.

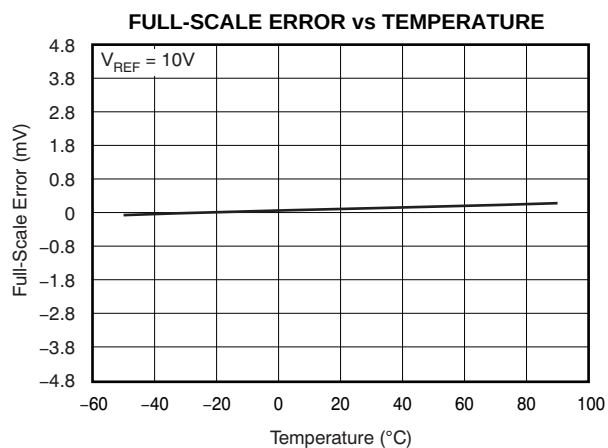


Figure 23.

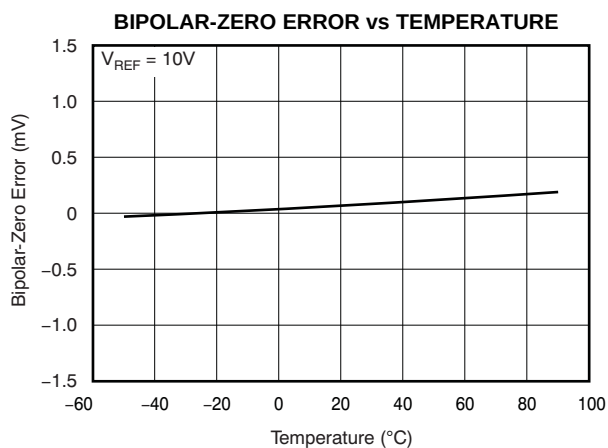
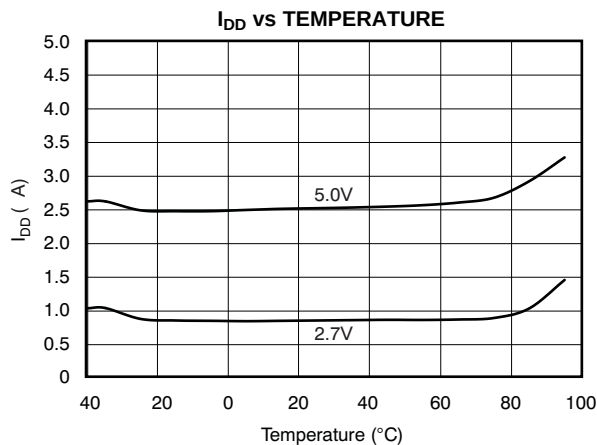
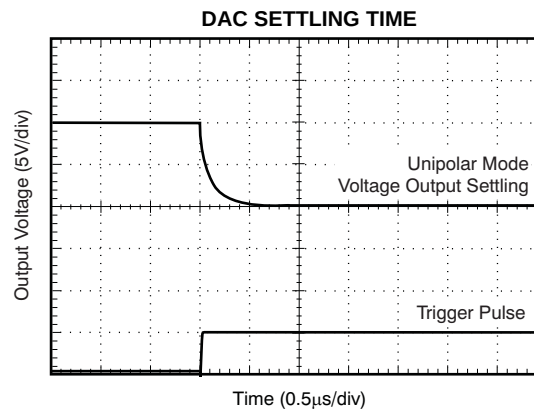
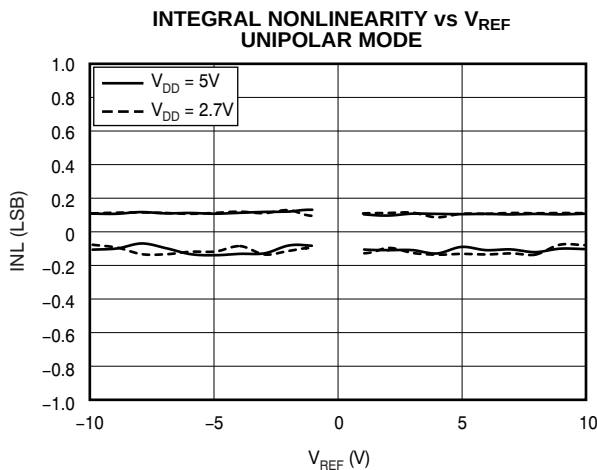
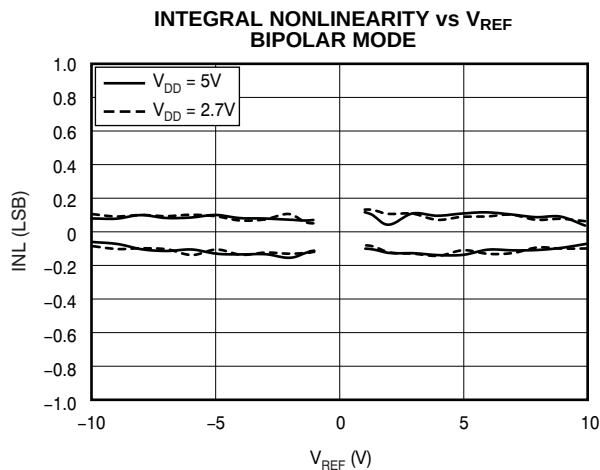
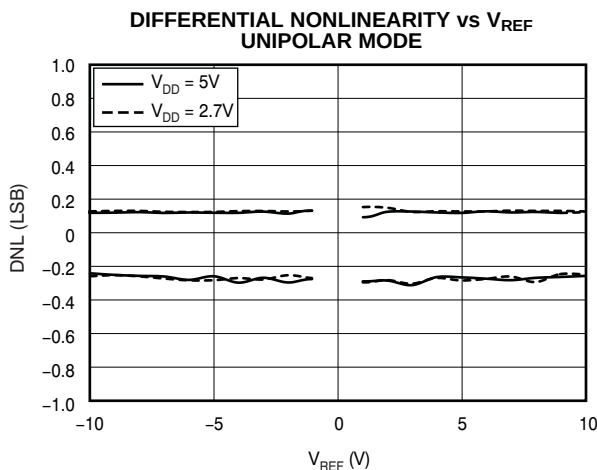
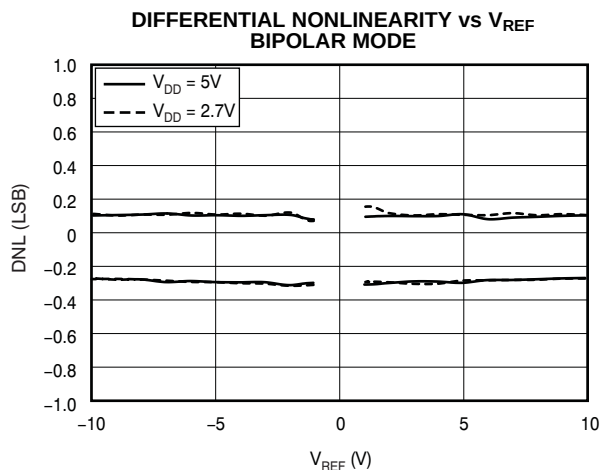


Figure 24.

TYPICAL CHARACTERISTICSAt $T_A = +25^\circ\text{C}$, unless otherwise noted.**Figure 25.****Figure 26.****Figure 27.****Figure 28.****Figure 29.****Figure 30.**

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

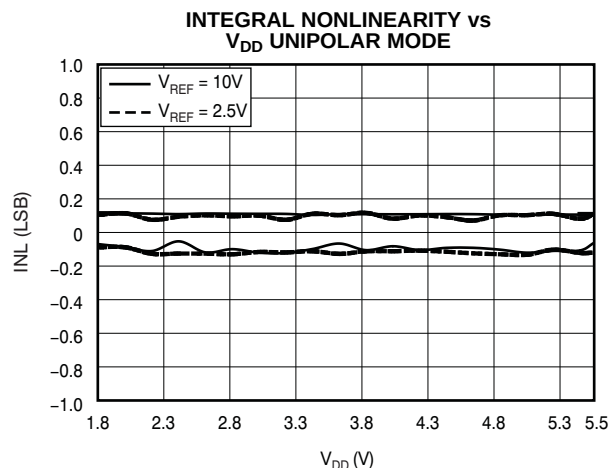


Figure 31.

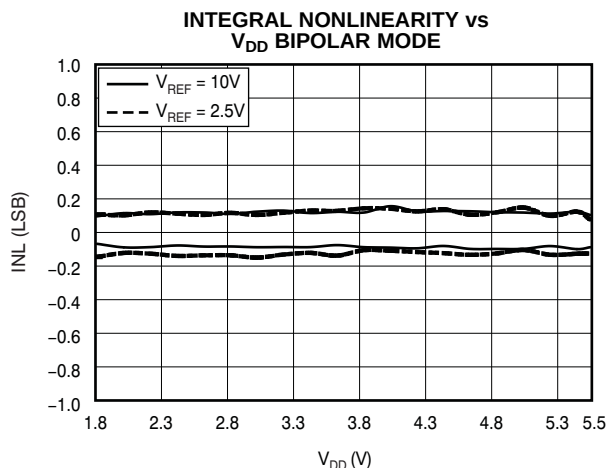


Figure 32.

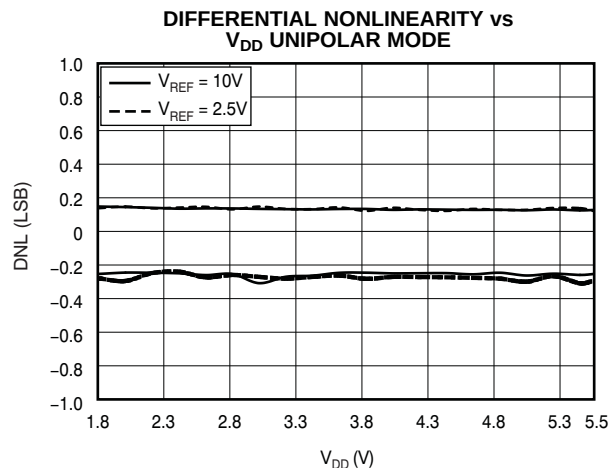


Figure 33.

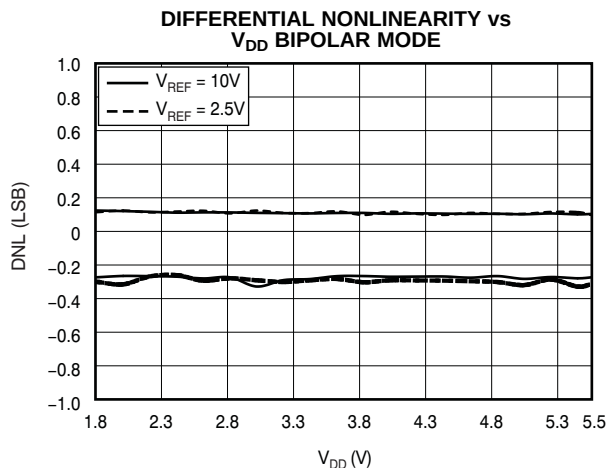


Figure 34.

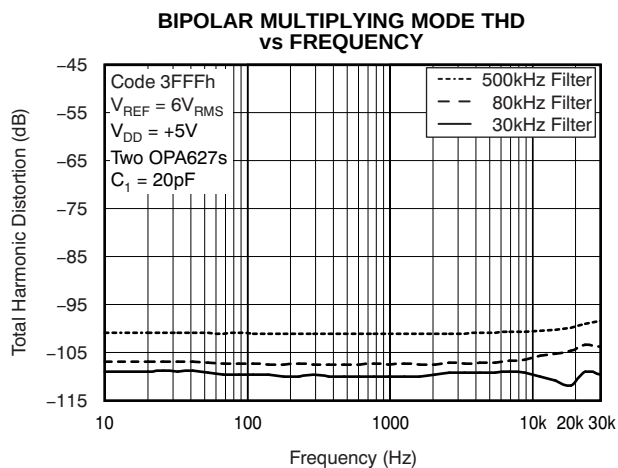


Figure 35.

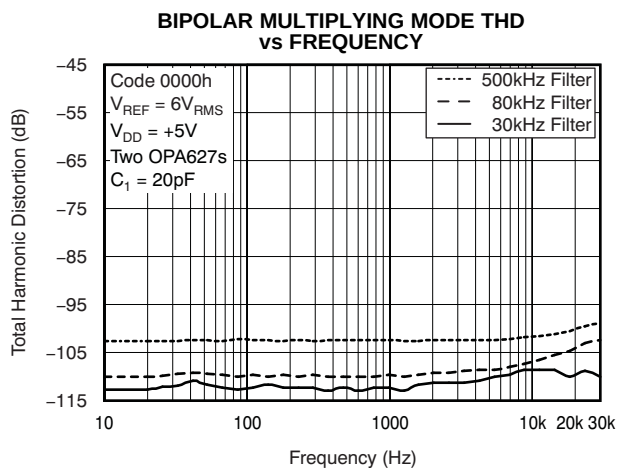
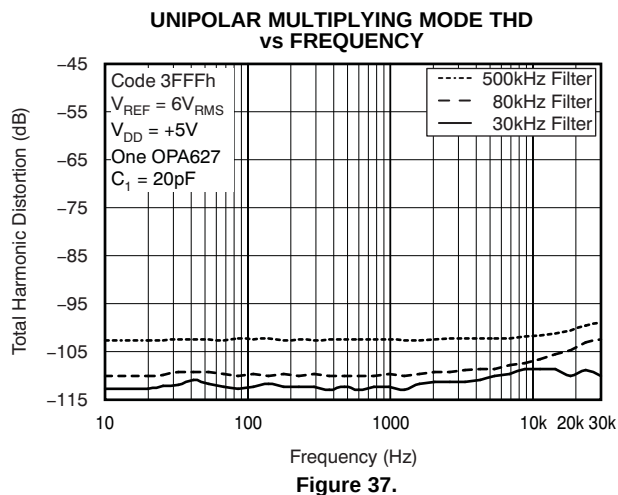


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.



THEORY OF OPERATION

The DAC8806 is a multiplying, single-channel current output, 14-bit DAC. The architecture, illustrated in [Figure 38](#), is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of $6\text{ k}\Omega \pm 25\%$. The external reference voltage can vary in a range of -10 V to $+10\text{ V}$, thus providing bipolar I_{OUT} current operation. By using an external I/V converter op amp and the R_{FB} resistor in the DAC8806, an output voltage range of $-V_{REF}$ to $+V_{REF}$ can be generated.

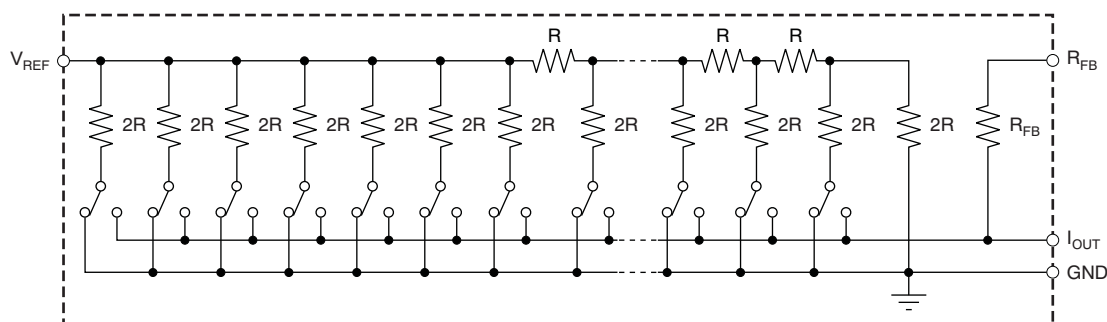


Figure 38. Equivalent R-2R DAC Circuit

The DAC output voltage is determined by V_{REF} and the digital data (D) according to [Equation 1](#):

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \quad (1)$$

Each DAC code determines the 2R-leg switch position to either GND or I_{OUT} . The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I_{OUT} terminal) changes versus code. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8806 because of offset modulation versus DAC code. For best linearity performance of the DAC8806, an op amp ([OPA277](#)) is recommended; see [Figure 39](#). This circuit allows V_{REF} to swing from -10 V to $+10\text{ V}$.

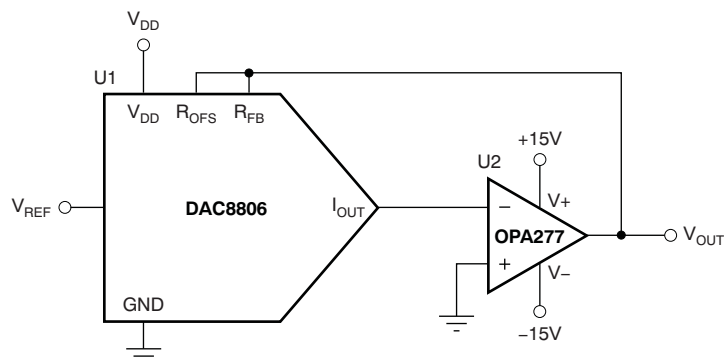


Figure 39. Voltage Output Configuration

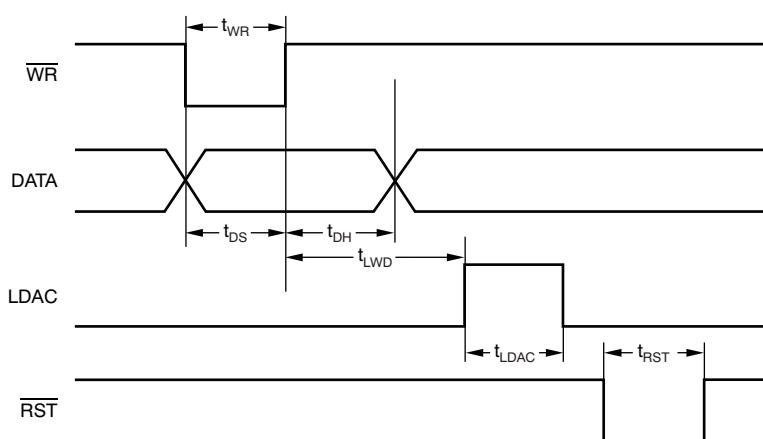


Figure 40. DAC8806 Timing Diagram

Table 1. Function of Control Inputs

CONTROL INPUTS			REGISTER OPERATION
RST	WR	LDAC	
0	X	X	Asynchronous operation. The DAC register is set to zero code, resulting in the DAC output being set to 0 V. The DAC input register contents are not reset by the RST signal.
1	0	0	Load the input register with all 14 data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC register are transparent.
1			LDAC and WR are tied together and programmed as a pulse. The 14 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

APPLICATION INFORMATION

Multiplying Mode THD versus Frequency

Figure 35 and Figure 36 show the DAC8806 bipolar 4-quadrant multiplying mode total harmonic distortion (THD) versus frequency. Figure 35 shows the bipolar mode THD with the DAC8806 set to a full-scale code of 3FFFh. Figure 36 shows the bipolar multiplying mode THD with the DAC8806 set to a minus full-scale code of 0000h. In both graphs, two OPA627s are used for both the DAC output op amp and the reference inverting amplifier. A 6 V_{RMS} sine wave is used for the reference input V_{REF} and is swept in frequency from 10 Hz to 30 kHz. The THD levels versus frequency are illustrated at various DAC output filtering levels using an external ac-coupled low-pass filter.

Figure 37 illustrates the DAC8806 unipolar 2-quadrant multiplying mode THD versus frequency. The DAC8806 is set to a full-scale code of 3FFFh. A single OPA627 is used for the DAC output op amp.

Stability Circuit

For a current-to-voltage (I/V) design, as shown in Figure 41, the DAC8806 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C1 (4 pF to 20 pF, typ) can be added to the design for circuit stability, as shown in Figure 41.

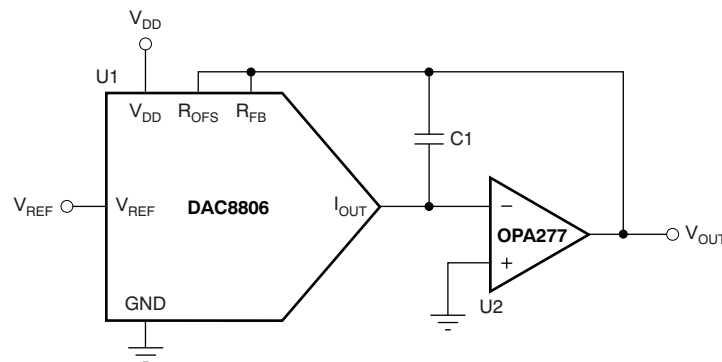


Figure 41. Gain Peaking Prevention Circuit with Compensation Capacitor

Bipolar Output Circuit

The DAC8806, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I_{OUT}) is the inverse of the input reference voltage at V_{REF}.

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 42 demonstrates a ±10 V_{OUT} circuit with a fixed +10 V reference.

$$V_{OUT} = \left(\frac{D}{8192} - 1 \right) \times V_{REF} \quad (2)$$

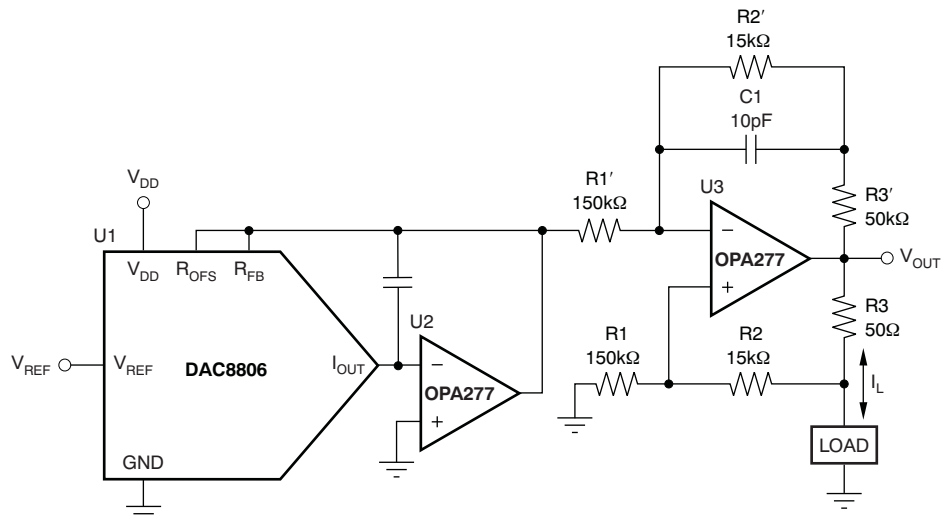


Figure 43. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC8806 has an industry-standard pinout. [Table 2](#) provides the cross-reference information.

Table 2. Cross-Reference

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8806IDB	14	±1	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1591AIG

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2006) to Revision B	Page
• Changed front page block diagram.....	1
• Fixed typo on 2nd <i>Interface Timing</i> subheader; changed from 5.0V to 2.7V	3
• Changed pin 28 description text in <i>Terminal Functions</i> table.....	4
• Changed first row description text in Table 1	13
• Changed Figure 42	15

Changes from Original (April 2006) to Revision A	Page
• Changed from "voltage-to-current" to "current-to-voltage"	1
• Changed from (V/I) to (I/V)	14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8806IDB	Active	Production	SSOP (DB) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806
DAC8806IDB.A	Active	Production	SSOP (DB) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806
DAC8806IDB.B	Active	Production	SSOP (DB) 28	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806
DAC8806IDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806
DAC8806IDBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806
DAC8806IDBR.B	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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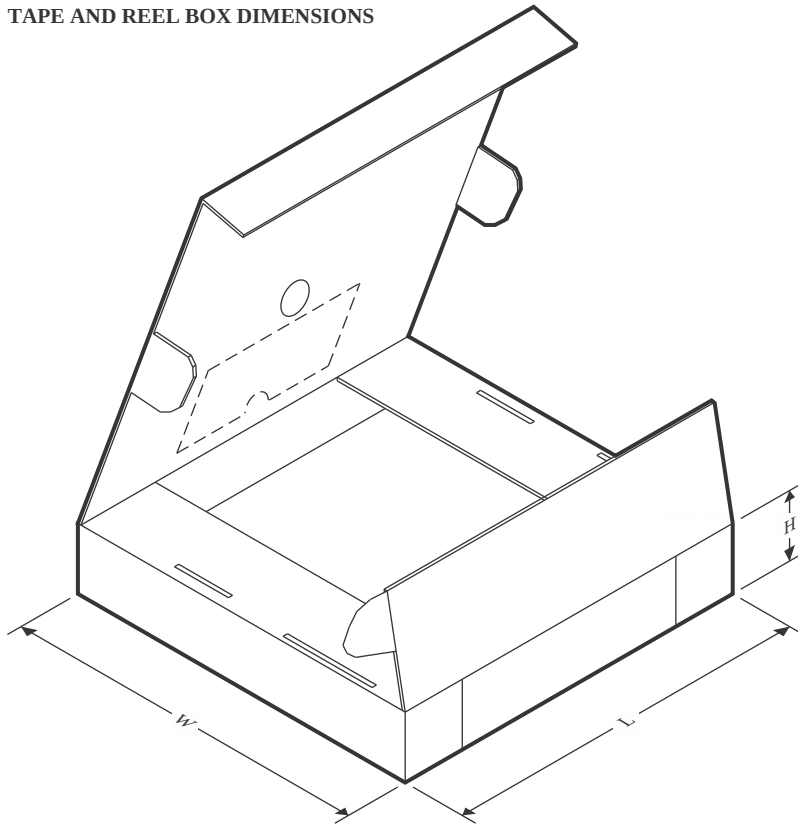
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8806IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

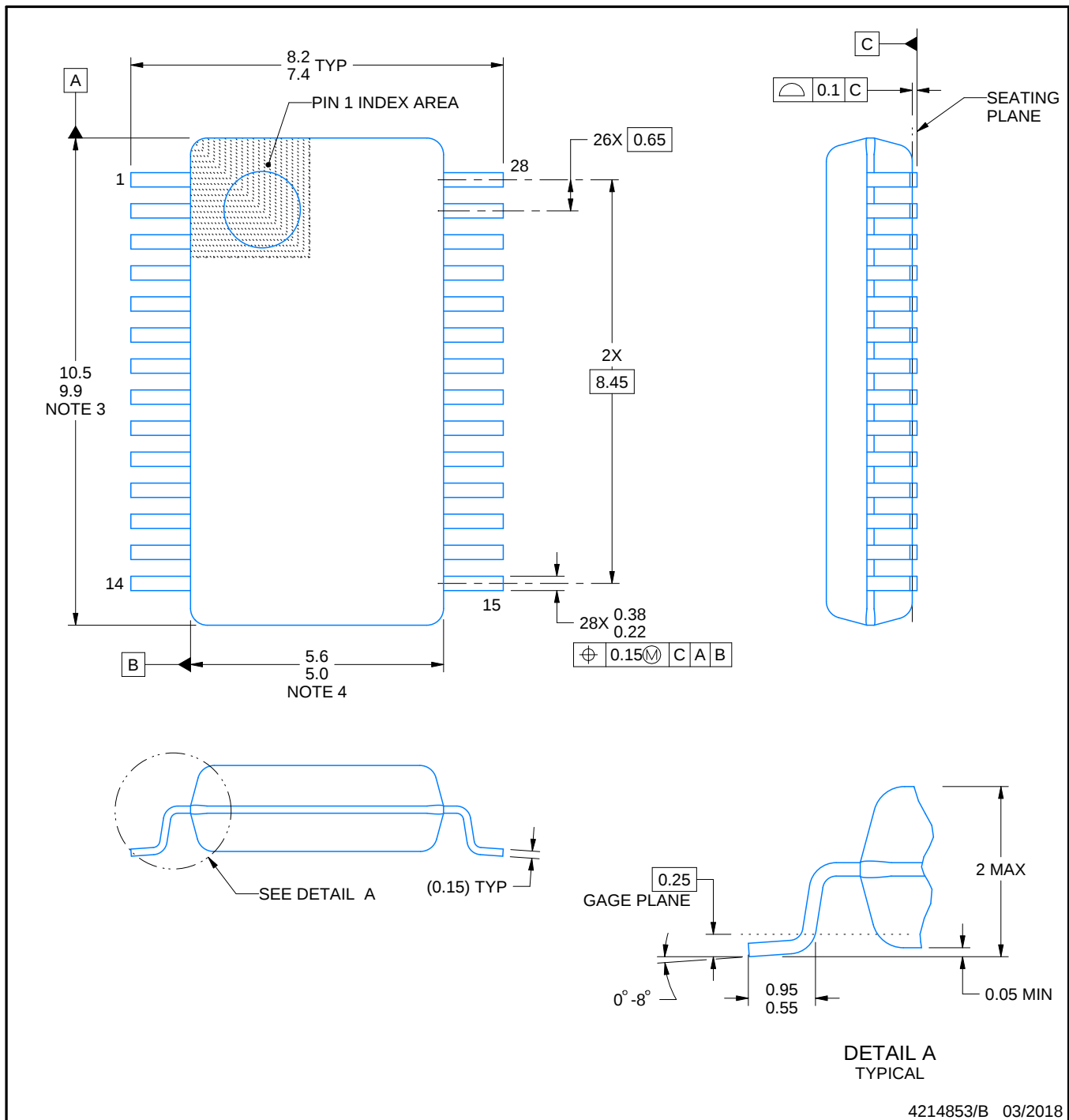
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8806IDBR	SSOP	DB	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC8806IDB	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8806IDB.A	DB	SSOP	28	50	530	10.5	4000	4.1
DAC8806IDB.B	DB	SSOP	28	50	530	10.5	4000	4.1



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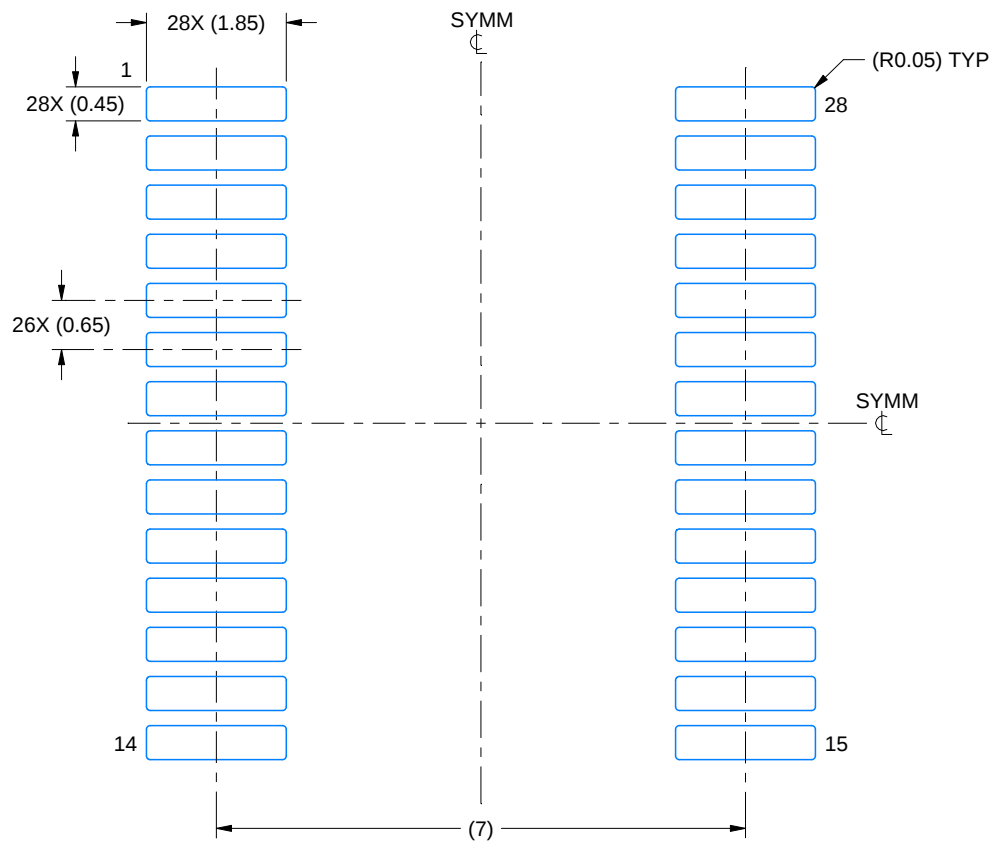
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

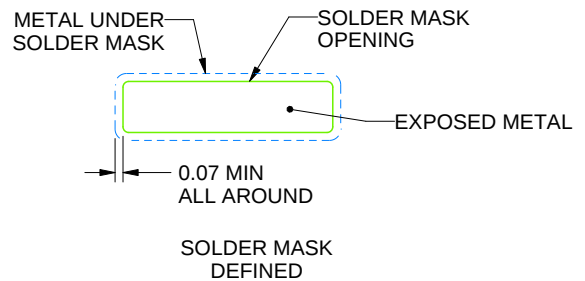
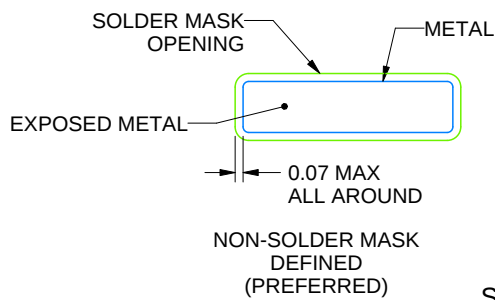
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

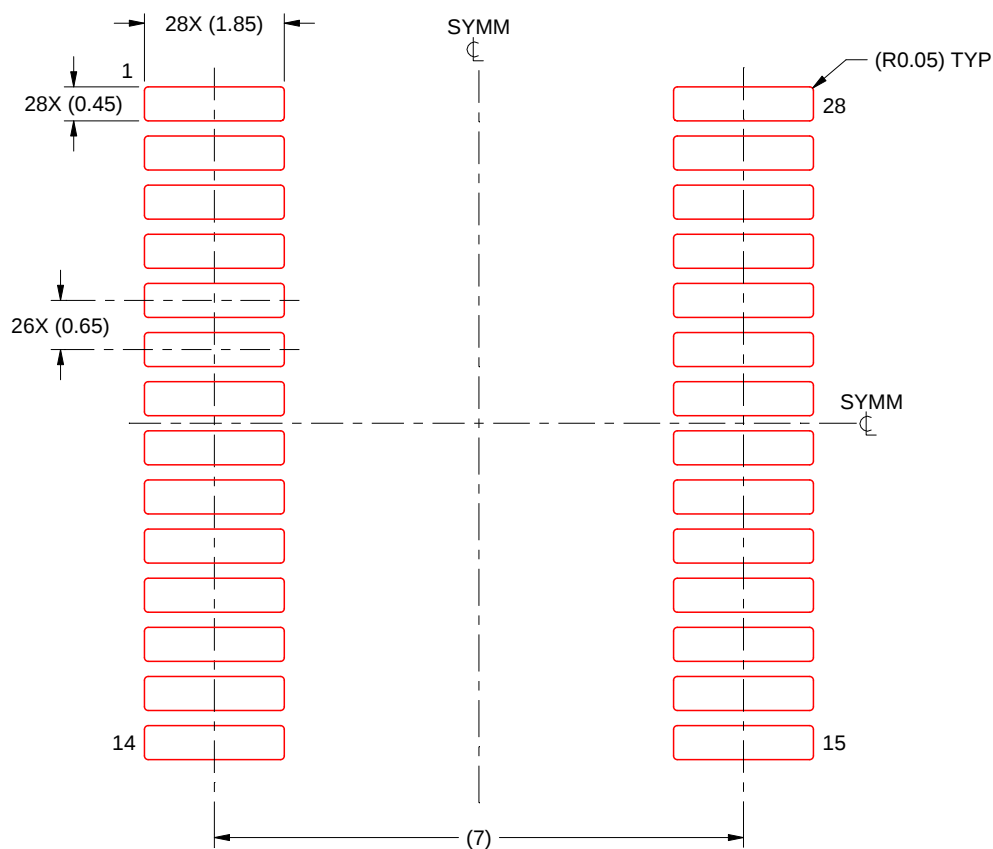
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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