# PCF2120 Quartz oscillator Rev. 01 — 5 February 2008

**Product data sheet** 

#### 1. **General description**

The PCF2120 is a CMOS quartz oscillator optimized for low power consumption. The 32 kHz output signal is gated using an enable signal.

#### **Features** 2.

- Clock operating voltage: 1.5 V to 5.5 V
- Low backup current: typical 0.85  $\mu$ A at  $V_{DD}$  = 3.0 V and  $T_{amb}$  = 25  $^{\circ}$ C
- 32.768 kHz output for peripheral devices
- Two integrated oscillator capacitors
- Push-pull output
- Internal power-on reset

#### **Applications** 3.

- Portable instruments
- Industrial products
- Battery powered products

#### **Quick reference data** 4.

Table 1. Quick reference data

| Symbol                         | Parameter             | Conditions   | Min           | Тур | Max  | Unit |
|--------------------------------|-----------------------|--|---------------|-----|------|------|
| $V_{DD}$                       | supply voltage        |  | <u>11</u> 1.5 | -   | 5.5  | V    |
| I <sub>DD</sub> supply current | clock output disabled |  |               |     |      |      |
|                                |                       | $V_{DD}$ = 2.0 V; $T_{amb}$ = 25 °C  | -             | 210 | 450  | nA   |
|                                |                       | $V_{DD} = 3.0 \text{ V};$<br>$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$ | -             | 265 | 650  | nA   |
|                                |                       | clock output enabled at 32 kHz   |               |     |      |      |
|                                |                       | $V_{DD}$ = 2.0 V; $T_{amb}$ = 25 °C  | -             | 615 | 900  | nA   |
|                                |                       | $V_{DD} = 3.0 \text{ V};$<br>$T_{amb} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}$         | -             | 875 | 1100 | nA   |
| $T_{stg}$                      | storage temperature   |  | -65           | -   | +150 | °C   |

<sup>[1]</sup> For reliable oscillator start-up at power-up:  $V_{DD} > V_{DD(min)} + 0.3 \text{ V}$ .



**Quartz oscillator** 

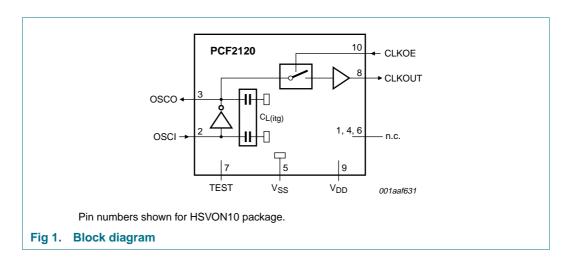
# 5. Ordering information

Table 2. Ordering information

| Туре        | Package |  |          |  |  |
|-------------|---------|--|----------|--|--|
| number      | Name    | Description  | Version  |  |  |
| PCF2120TK   | HVSON10 | plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body $3\times3\times0.85$ mm | SOT650-1 |  |  |
| PCF2120U[1] | -       | wire bond die; 7 bonding pads; $0.57 \times 1.1 \times 0.2$ mm   | PCF2120U |  |  |

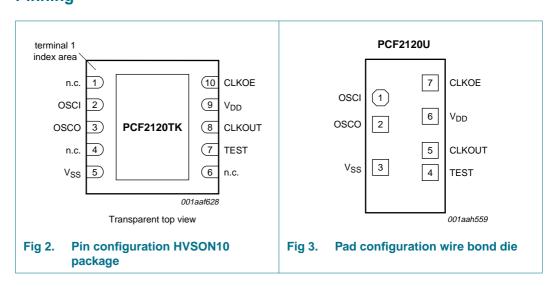
<sup>[1]</sup> Packing method: sawn wafer on Film Frame Carrier (FFC).

# 6. Block diagram



# 7. Pinning information

## 7.1 Pinning



Quartz oscillator

## 7.2 Pin description

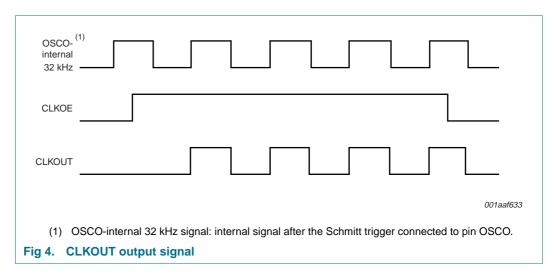
Table 3. Pin description

| Symbol   | Pin     | Pad           | Description               |  |
|----------|---------|---------------|---------------------------|--|
|          | HVSON10 | Wire bond die | •                         |  |
| n.c.     | 1       | -             | not connected             |  |
| OSCI     | 2       | 1             | oscillator input          |  |
| OSCO     | 3       | 2             | oscillator output         |  |
| n.c.     | 4       | -             | not connected             |  |
| $V_{SS}$ | 5       | 3             | ground                    |  |
| n.c.     | 6       | -             | not connected             |  |
| TEST     | 7       | 4             | test pin                  |  |
| CLKOUT   | 8       | 5             | clock output (push-pull)  |  |
| $V_{DD}$ | 9       | 6             | supply voltage            |  |
| CLKOE    | 10      | 7             | clock output enable input |  |

# 8. Functional description

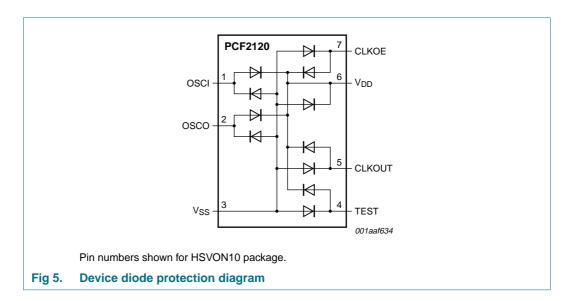
The 32 kHz quartz oscillator is optimized for directly connecting to a 32 kHz tuning fork quartz crystal. No additional tuning capacitors are required. Laser tuning of the quartz or quartz selection for matching is used to tune the oscillator if required.

A digital 32 kHz signal is available on pin CLKOUT. The signal on pin CLKOE is used to gate and synchronize the 32 kHz CLKOUT signal. Pin CLKOUT is a CMOS push-pull output. If disabled, it goes to LOW level.



**Quartz oscillator** 

# 9. Internal circuitry



# 10. Limiting values

**Table 4.** Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

|                  |                                 | • • •         | •            |       |      |
|------------------|---------------------------------|---------------|--------------|-------|------|
| Symbol           | Parameter                       | Conditions    | Min          | Max   | Unit |
| $V_{DD}$         | supply voltage                  |               | -0.5         | +6.5  | V    |
| $I_{DD}$         | supply current                  |               | -50          | +50   | mA   |
| $V_{I}$          | input voltage                   |               | -0.5         | +6.5  | V    |
| $V_{O}$          | output voltage                  |               | -0.5         | +6.5  | V    |
| II               | input current                   | at any input  | -10          | +10   | mA   |
| Io               | output current                  | at any output | -10          | +10   | mA   |
| $P_{tot}$        | total power dissipation         |               | -            | 300   | mW   |
| T <sub>stg</sub> | storage temperature             |               | -65          | +150  | °C   |
| V <sub>esd</sub> | electrostatic discharge voltage | HBM           | <u>[1]</u> _ | ±2000 | V    |
|                  |                                 | MM            | [2] _        | ±200  | V    |
|                  |                                 | CDM           | <u>[3]</u> _ | ±2000 | V    |
| I <sub>lu</sub>  | latch-up current                |               | <u>[4]</u> _ | 100   | mA   |
|                  |                                 |               |              |       |      |

<sup>[1]</sup> Human Body Model (HBM) according to JESD22-A114.

<sup>[2]</sup> Machine Model (MM) according to JESD22-A115.

<sup>[3]</sup> Charged-Device Model (CDM) according to JESD22-C101.

<sup>[4]</sup> Latch-up testing according to JESD78.

**Quartz oscillator** 

# 11. Static characteristics

Table 5. Static characteristics

 $V_{DD}$  = 1.5 V to 5.5 V;  $V_{SS}$  = 0 V;  $T_{amb}$  = -40 °C to +85 °C;  $f_{osc}$  = 32.768 kHz; quartz  $R_s$  = 40 k $\Omega$ ;  $C_L$  = 8 pF; unless otherwise specified.

| Symbol          | Parameter                 | Conditions  | Min                | Тур  | Max            | Unit |
|-----------------|---------------------------|---|--------------------|------|----------------|------|
| Supply          |                           |   |                    |      |                |      |
| $V_{DD}$        | supply voltage            |   | <u>[1]</u> 1.5     | -    | 5.5            | V    |
| $I_{DD}$        | supply current            | clock output disabled   |                    |      |                |      |
|                 |                           | T <sub>amb</sub> = 25 °C  |                    |      |                |      |
|                 |                           | $V_{DD} = 5.0 \text{ V}$  | -                  | 300  | 550            | nΑ   |
|                 |                           | $V_{DD} = 3.0 \text{ V}$  | -                  | 235  | 500            | nA   |
|                 |                           | $V_{DD} = 2.0 \text{ V}$  | -                  | 210  | 450            | nA   |
|                 |                           | $T_{amb} = -40  ^{\circ}\text{C} \text{ to } +85  ^{\circ}\text{C}$ |                    |      |                |      |
|                 |                           | $V_{DD} = 5.0 \text{ V}$  | -                  | 345  | 750            | nA   |
|                 |                           | $V_{DD} = 3.0 \text{ V}$  | -                  | 265  | 650            | nA   |
|                 |                           | $V_{DD} = 2.0 \text{ V}$  | -                  | 230  | 600            | nA   |
|                 |                           | clock output enabled at 32 kHz                                      | [2]                |      |                |      |
|                 |                           | T <sub>amb</sub> = 25 °C  |                    |      |                |      |
|                 |                           | $V_{DD} = 5.0 \text{ V}$  | -                  | 1310 | 1700           | nA   |
|                 |                           | $V_{DD} = 3.0 \text{ V}$  | -                  | 845  | 1100           | nA   |
|                 |                           | $V_{DD} = 2.0 \text{ V}$  | -                  | 615  | 900            | nA   |
|                 |                           | $T_{amb} = -40  ^{\circ}\text{C} \text{ to } +85  ^{\circ}\text{C}$ |                    |      |                |      |
|                 |                           | $V_{DD} = 5.0 \text{ V}$  | -                  | 1385 | 1700           | nA   |
|                 |                           | $V_{DD} = 3.0 \text{ V}$  | -                  | 875  | 1100           | nA   |
|                 |                           | $V_{DD} = 2.0 \text{ V}$  | -                  | 635  | 900            | nA   |
| Inputs          |                           |   |                    |      |                |      |
| Pin OSCI        |                           |   |                    |      |                |      |
| VI              | input voltage             |   | -0.5               | -    | $V_{DD} + 0.5$ | V    |
| Pin CLKOE       |                           |   |                    |      |                |      |
| VI              | input voltage             |   | -0.5               | -    | $V_{DD} + 0.5$ | V    |
| V <sub>IL</sub> | LOW-level input voltage   |   | -                  | -    | $0.3V_{DD}$    | V    |
| $V_{IH}$        | HIGH-level input voltage  |   | 0.7V <sub>DD</sub> | -    | -              | V    |
| ILI             | input leakage current     | $V_I = V_{DD}$ or $V_{SS}$  | -1                 | 0    | +1             | μΑ   |
| Outputs         |                           |   |                    |      |                |      |
| Pin OSCO        |                           |   |                    |      |                |      |
| Vo              |                           |   | -0.5               | -    | $V_{DD} + 0.5$ | V    |
| Pin CLKOU       |                           |   |                    |      |                |      |
| Vo              | output voltage            |   | -0.5               | -    | $V_{DD} + 0.5$ | V    |
| l <sub>OL</sub> | LOW-level output current  | $V_{OL} = 0.4 \text{ V}; V_{DD} = 5 \text{ V}$                      | -1                 | -    | -              | mΑ   |
| I <sub>OH</sub> | HIGH-level output current | $V_{OH} = 4.6 \text{ V}; V_{DD} = 5 \text{ V}$                      | -                  | -    | 1              | mΑ   |
| $I_{LO}$        | output leakage current    | $V_O = V_{DD}$ or $V_{SS}$  | -1                 | 0    | +1             | μΑ   |

<sup>[1]</sup> For reliable oscillator start-up at power-up:  $V_{DD} > V_{DD(min)} + 0.3 \text{ V}$ .

**Quartz** oscillator

[2] Pin CLKOUT is loaded with a 7.5 pF capacitor.

When pin CLKOUT is enabled the current consumption is a function of the load on that pin, the output frequency and the supply voltage. The additional current consumption for a given load can be calculated from the formula  $I_{DD} = C_{CLKOUT} \times V_{DD} \times f_{CLKOUT}$ 

Where:

I<sub>DD</sub> = supply current

 $C_{CLKOUT}$  = capacitance on pin CLKOUT

V<sub>DD</sub> = supply voltage

f<sub>CLKOUT</sub> = output frequency on pin CLKOUT

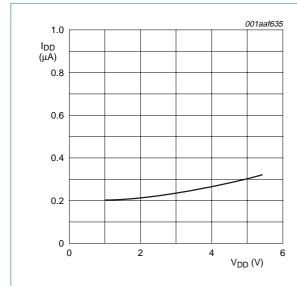
# 12. Dynamic characteristics

#### Table 6. Dynamic characteristics

 $V_{DD}$  = 1.5 V to 5.5 V;  $V_{SS}$  = 0 V;  $T_{amb}$  = -40 °C to +85 °C;  $f_{osc}$  = 32.768 kHz; quartz  $R_s$  = 40 k $\Omega$  and  $C_L$  = 8 pF; unless otherwise specified.

| Symbol                           | Parameter                               | Conditions                                  | Min          | Тур | Max | Unit |
|----------------------------------|---|---|--------------|-----|-----|------|
| Oscillator                       |   |   |              |     |     |      |
| C <sub>L(itg)</sub>              | integrated load capacitance             |   | <u>[1]</u> 6 | 8   | 10  | pF   |
| $\Delta f_{\rm osc}/f_{\rm osc}$ | relative oscillator frequency variation | $\Delta V_{DD}$ = 200 mV; $T_{amb}$ = 25 °C | -            | 0.2 | -   | ppm  |

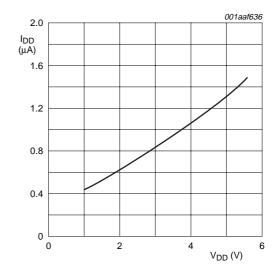
[1] C<sub>L(itg)</sub> is the combined equivalent integrated oscillator input and output capacitances.



a. CLKOUT disabled

 $T_{amb}$  = 25 °C.

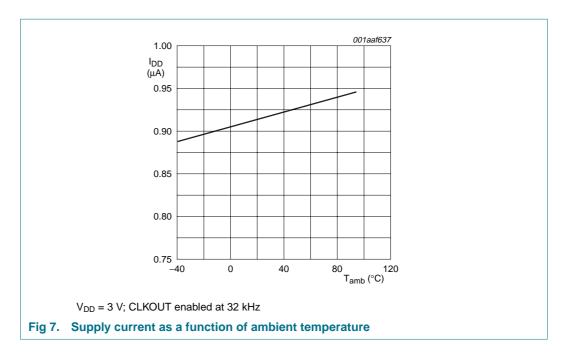
Fig 6. Supply current as a function of supply voltage



b. CLKOUT enabled at 32 kHz

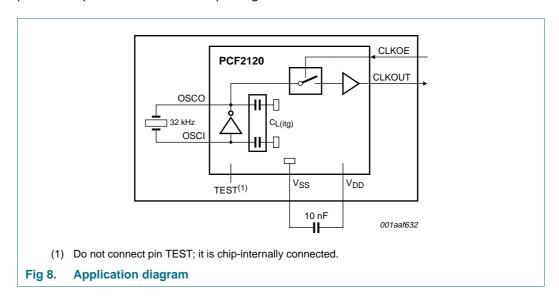
 $T_{amb} = 25 \, ^{\circ}C.$ 

**Quartz oscillator** 



# 13. Application information

You can mount the PCF2120 oscillator together with the quartz crystal as an accurate and pre-tuned quartz oscillator in one package.



Quartz oscillator

# 14. Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body  $3 \times 3 \times 0.85 \text{ mm}$ 

SOT650-1

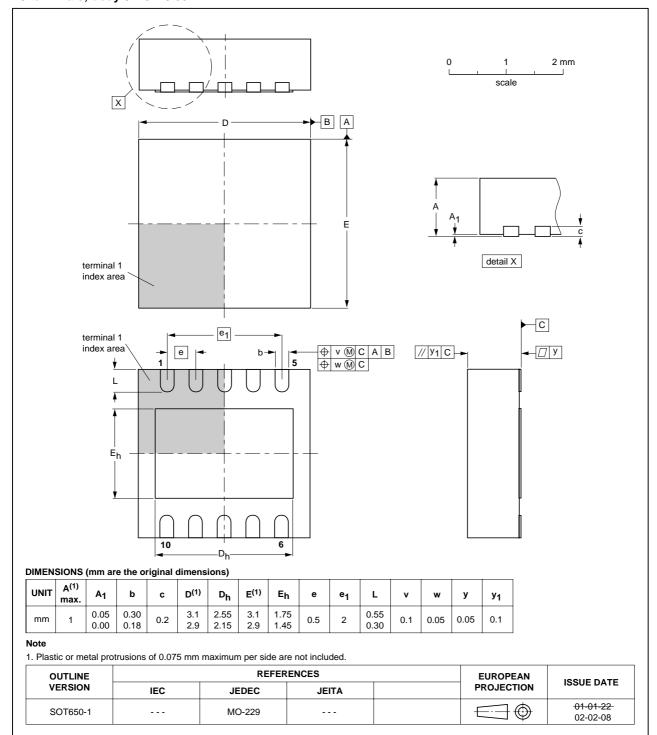


Fig 9. Package outline SOT650-1 (HVSON10)

**Quartz** oscillator

## 15. Bare die outline

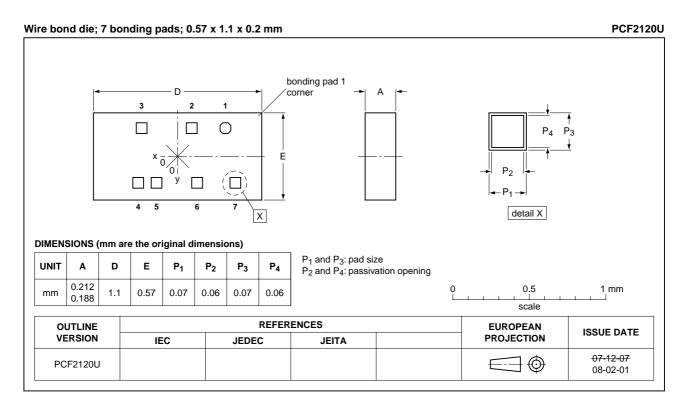


Fig 10. Bare die outline PCF2120U

Table 7. Bonding pad coordinates Values x and y in  $\mu m$ .

|     | •           |             |  |
|-----|-------------|-------------|--|
| Pad | x           | у           |  |
| 1   | +313        | +187        |  |
| 2   | +93         | +187        |  |
| 3   | -236        | +187        |  |
| 4   | -259        | -172        |  |
| 5   | <b>–137</b> | <b>–172</b> |  |
| 6   | +127        | <b>–172</b> |  |
| 7   | +380        | -172        |  |

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

Quartz oscillator

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- · Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

#### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

#### 16.4 Reflow soldering

Key characteristics in reflow soldering are:

 Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see <u>Figure 11</u>) than a SnPb process, thus reducing the process window

Quartz oscillator

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

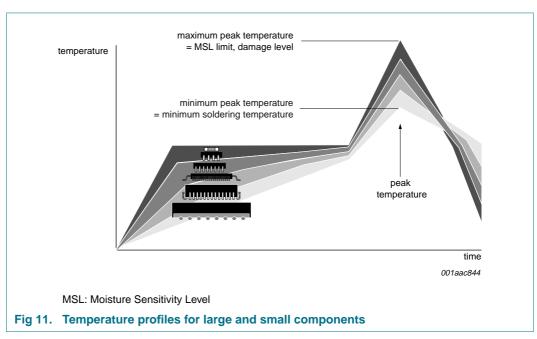
| Package thickness (mm) | Package reflow temperature (°C) |       |  |
|------------------------|---------------------------------|-------|--|
|                        | Volume (mm³)                    |       |  |
|                        | < 350                           | ≥ 350 |  |
| < 2.5                  | 235                             | 220   |  |
| ≥ 2.5                  | 220                             | 220   |  |

Table 9. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) |             |        |  |
|------------------------|---------------------------------|-------------|--------|--|
|                        | Volume (mm³)                    |             |        |  |
|                        | < 350                           | 350 to 2000 | > 2000 |  |
| < 1.6                  | 260                             | 260         | 260    |  |
| 1.6 to 2.5             | 260                             | 250         | 245    |  |
| > 2.5                  | 250                             | 245         | 245    |  |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



**Quartz oscillator** 

For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

# 17. Revision history

#### Table 10. Revision history

| Document ID | Release date | Data sheet status  | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| PCF2120_1   | 20080205     | Product data sheet | -             | -          |

Quartz oscillator

# 18. Legal information

#### 18.1 Data sheet status

| Document status[1][2]          | Product status[3] | Definition  |
|--------------------------------|-------------------|---|
| Objective [short] data sheet   | Development       | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification     | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production        | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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**PCF2120 NXP Semiconductors** 

#### **Quartz oscillator**

# 20. Contents

| 1    | General description          |
|------|------------------------------|
| 2    | Features                     |
| 3    | Applications                 |
| 4    | Quick reference data 1       |
| 5    | Ordering information 2       |
| 6    | Block diagram 2              |
| 7    | Pinning information          |
| 7.1  | Pinning                      |
| 7.2  | Pin description              |
| 8    | Functional description 3     |
| 9    | Internal circuitry 4         |
| 10   | Limiting values 4            |
| 11   | Static characteristics 5     |
| 12   | Dynamic characteristics 6    |
| 13   | Application information 7    |
| 14   | Package outline 8            |
| 15   | Bare die outline 9           |
| 16   | Soldering of SMD packages 9  |
| 16.1 | Introduction to soldering    |
| 16.2 | Wave and reflow soldering 10 |
| 16.3 | Wave soldering               |
| 16.4 | Reflow soldering             |
| 17   | Revision history 12          |
| 18   | Legal information            |
| 18.1 | Data sheet status            |
| 18.2 | Definitions                  |
| 18.3 | Disclaimers                  |
| 18.4 | Trademarks                   |
| 19   | Contact information          |
| 20   | Contents                     |

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