

## FEATURES

5 MHz to 16 MHz external clock input rate  
 16 bits, no missing codes  
 Signal-to-noise ratio (SNR): 88 dB typical  
 Effective number of bits (ENOB): 14.2 bits typical  
 Offset drift vs. temperature: 1.6  $\mu\text{V}/^\circ\text{C}$  typical  
 On-board digital isolator  
 On-board reference  
 Full-scale analog input range:  $\pm 320$  mV  
 High common-mode transient immunity:  $>25$  kV/ $\mu\text{s}$   
 Wide-body SOIC with increased creepage package  
 Slew rate limited output for low EMI

### Safety and regulatory approvals

#### UL recognition

5000 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE Certificate of Conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{\text{IORM}} = 1250$  V<sub>PEAK</sub>

## ENHANCED PRODUCT FEATURES

Defense and aerospace applications (AQEC standard)

Military temperature range:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

## APPLICATIONS

Shunt current monitoring

AC motor controls

Power and solar inverters

Wind turbine inverters

Data acquisition systems

Analog-to-digital and optoisolator replacements

## GENERAL DESCRIPTION

The AD7403-EP<sup>1</sup> is a high performance, second-order,  $\Sigma$ - $\Delta$  modulator that converts an analog input signal into a high speed, single-bit data stream, with on-chip digital isolation based on Analog Devices, Inc., iCoupler® technology. The device operates from a 5 V ( $V_{\text{DD1}}$ ) power supply and accepts a differential input signal of  $\pm 250$  mV ( $\pm 320$  mV full-scale). The differential input is ideally suited to shunt voltage monitoring in high voltage applications where galvanic isolation is required.

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. 0

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## FUNCTIONAL BLOCK DIAGRAM

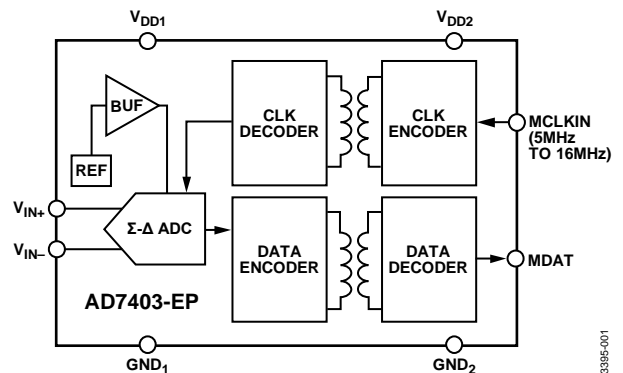


Figure 1.

13395-001

The analog input is continuously sampled by a high performance analog modulator, and converted to a one's density digital output stream with a data rate of up to 16 MHz. The original

information can be reconstructed with an appropriate digital filter to achieve 88 dB signal to noise ratio (SNR) at 78.1 kSPS.

The serial interface is digitally isolated. High speed complementary metal oxide semiconductor (CMOS) technology, combined with monolithic transformer technology, means the on-chip isolation provides outstanding performance characteristics, superior to alternatives such as optocoupler devices. The AD7403-EP device is offered in a 16-lead, wide-body SOIC package and has an operating temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Additional application and technical information can be found in the AD7403 data sheet.

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REVISION HISTORY

4/16—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD1} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{DD2} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{IN+} = -250\text{ mV to }+250\text{ mV}$ ,  $V_{IN-} = 0\text{ V}$ ,  $T_A = -55^{\circ}\text{C to }+125^{\circ}\text{C}$ ,  $f_{MCLKIN} = 5\text{ MHz to }16\text{ MHz}$ , tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity (INL) <sup>1</sup>		±2	±12	LSB	Guaranteed no missed codes to 16 bits  0°C to 85°C
Differential Nonlinearity (DNL) <sup>1</sup>			±0.99	LSB	
Offset Error <sup>1</sup>		±0.2	±0.9	mV	
Offset Drift vs. Temperature <sup>2</sup>		1.6	3.8	µV/°C	
		1.3	3.1	µV/°C	
Offset Drift vs. V <sub>DD1</sub> <sup>2</sup>		50		µV/V	
Gain Error <sup>1</sup>		±0.2	±0.95	% FSR	
Gain Error Drift vs. Temperature <sup>2</sup>		65	95	ppm/°C	
		40	60	µV/°C	
Gain Error Drift vs. V <sub>DD1</sub> <sup>2</sup>		±0.6		mV/V	
ANALOG INPUT					
Input Voltage Range	−320		+320	mV	Full-scale range
	−250		+250	mV	For specified performance
Input Common-Mode Voltage Range		−200 to +300		mV	
Dynamic Input Current		±45	±50	µA	V <sub>IN+</sub> = ±250 mV, V <sub>IN−</sub> = 0 V
		0.05		µA	V <sub>IN+</sub> = 0 V, V <sub>IN−</sub> = 0 V
DC Leakage Current		±0.01	±0.6	µA	
Input Capacitance		14		pF	
DYNAMIC SPECIFICATIONS <sup>1</sup>					
Signal-to-Noise-and-Distortion Ratio (SINAD)	82	87		dB	V <sub>IN+</sub> = 1 kHz
Signal-to-Noise Ratio (SNR)	86	88		dB	
Total Harmonic Distortion (THD)		−94		dB	
Peak Harmonic or Spurious Noise (SFDR)		−95		dB	
Effective Number of Bits (ENOB)	13.1	14.2		Bits	
Noise Free Code Resolution	14			Bits	
ISOLATION TRANSIENT IMMUNITY <sup>1</sup>					
	25	30		kV/µs	
LOGIC INPUTS					
Input Voltage	0.8 × V <sub>DD2</sub>				CMOS with Schmitt trigger
High (V <sub>IH</sub> )					
Low (V <sub>IL</sub> )					
Input Current (I <sub>IN</sub> )			±0.6	µA	
Input Capacitance (C <sub>IN</sub> )			10	pF	
LOGIC OUTPUTS					
Output Voltage	V <sub>DD2</sub> − 0.1				I <sub>O</sub> = −200 µA I <sub>O</sub> = 200 µA
High (V <sub>OH</sub> )					
Low (V <sub>OL</sub> )					
POWER REQUIREMENTS					
V <sub>DD1</sub>	4.5		5.5	V	V <sub>DD1</sub> = 5.5 V V <sub>DD2</sub> = 5.5 V V <sub>DD1</sub> = V <sub>DD2</sub> = 5.5 V
V <sub>DD2</sub>	4.5		5.5	V	
I <sub>DD1</sub>		30	36	mA	
I <sub>DD2</sub>		12	18	mA	
Power Dissipation		231	297	mW	

<sup>1</sup> See the Terminology section of the AD7403 datasheet.

<sup>2</sup> Not production tested. Sample tested during initial release to ensure compliance.

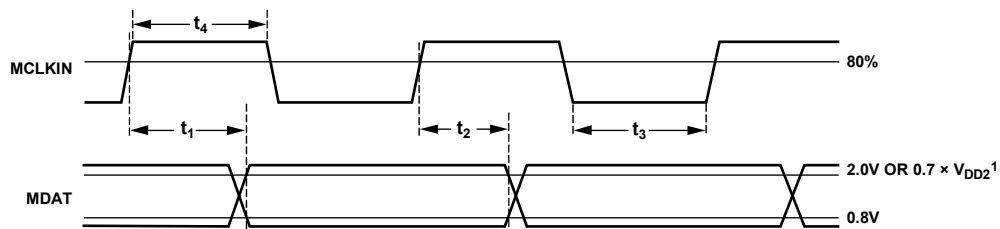
## TIMING SPECIFICATIONS

$V_{DD1} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read MDAT on the MCLKIN rising edge.

Table 2.

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$			Unit	Description
	Min	Typ	Max		
$f_{MCLKIN}$	5		16	MHz	Master clock input frequency
$t_1^1$			45	ns	Data access time after MCLKIN rising edge
$t_2^1$	12			ns	Data hold time after MCLKIN rising edge
$t_3$	$0.45 \times t_{MCLKIN}$			ns	Master clock low time
$t_4$	$0.45 \times t_{MCLKIN}$			ns	Master clock high time

<sup>1</sup> Defined as the time required from an 80% MCLKIN input level to when the output crosses 0.8 V or 2.0 V for  $V_{DD2} = 3\text{ V}$  to  $3.6\text{ V}$  or when the output crosses 0.8 V or  $0.7 \times V_{DD2}$  for  $V_{DD2} = 4.5\text{ V}$  to  $5.5\text{ V}$  as outlined in Figure 2. Measured with a  $\pm 200\text{ }\mu\text{A}$  load and a 25 pF load capacitance.



<sup>1</sup>SEE NOTE 1 OF TABLE 3 FOR FURTHER DETAILS.

Figure 2. Data Timing

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## PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	f = 1 MHz
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces

<sup>1</sup> The device is considered a 2-terminal device. For AD7403-EP, Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together.

## INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Input to Output Momentary Withstand Voltage	V <sub>ISO</sub>	5000 min	V	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3 min <sup>1, 2</sup>	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3 min <sup>1</sup>	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.034 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1 <sup>3</sup>
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table I) <sup>3</sup>

<sup>1</sup> In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

<sup>2</sup> Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

<sup>3</sup> CSA CTI rating for the AD7403-EP is >575 V and therefore Material Group II isolation group.

## REGULATORY INFORMATION

Table 5.

UL <sup>1</sup>	CSA	VDE <sup>2</sup>
Recognized under 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup>
5000 V rms Isolation Voltage Single Protection	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 830 V rms (1173 V <sub>PEAK</sub> ), maximum working voltage <sup>3</sup> Reinforced insulation per CSA 60950-1-07 and IEC 60950-1. 415 V rms (586 V <sub>PEAK</sub> ) maximum working voltage <sup>3</sup> Reinforced insulation per IEC 60601-1, 250 V rms (353 V <sub>PEAK</sub> ) maximum working voltage	Reinforced insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 1250 V <sub>PEAK</sub>
File E214100	File 205078	File 2471900-4880-0001

<sup>1</sup> In accordance with UL 1577, each AD7403-EP is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 μA).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each AD7403-EP is proof tested by applying an insulation test voltage ≥ 2344 V<sub>PEAK</sub> for 1 second (partial discharge detection limit = 5 pC).

<sup>3</sup> Rating is calculated for a pollution degree of 2 and a Material Group III. The AD7403-EP RI-16-2 package material is rated by CSA to a CTI of >575 V and therefore Material Group II.

**DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS**

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

**Table 6.**

Description	Symbol	Characteristic	Unit
INSTALLATION CLASSIFICATION PER DIN VDE 0110 For Rated Mains Voltage $\leq 300$ V rms For Rated Mains Voltage $\leq 450$ V rms For Rated Mains Voltage $\leq 600$ V rms For Rated Mains Voltage $\leq 1000$ V rms		I to IV I to IV I to IV I to IV	
CLIMATIC CLASSIFICATION		40/105/21	
POLLUTION DEGREE (DIN VDE 0110, TABLE 1)		2	
MAXIMUM WORKING INSULATION VOLTAGE	$V_{IORM}$	1250	$V_{PEAK}$
INPUT TO OUTPUT TEST VOLTAGE, METHOD B1 $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ Second, Partial Discharge $< 5$ pC	$V_{PD(M)}$	2344	$V_{PEAK}$
INPUT TO OUTPUT TEST VOLTAGE, METHOD A After Environmental Test Subgroup 1 $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ Seconds, Partial Discharge $< 5$ pC After Input and/or Safety Test Subgroup 2/ Safety Test Subgroup 3 $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ Seconds, Partial Discharge $< 5$ pC	$V_{PR(M)}$	2000 1500	$V_{PEAK}$ $V_{PEAK}$
HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, $t_{TR} = 10$ Seconds)	$V_{IOTM}$	8000	$V_{PEAK}$
SURGE ISOLATION VOLTAGE 1.2 $\mu$ s Rise Time, 50 $\mu$ s, 50% Fall Time	$V_{IOSM}$	7500	$V_{PEAK}$ $V_{PEAK}$
SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, SEE Figure 3) Case Temperature Side 1 ( $P_{VDD1}$ ) and Side 2 ( $P_{VDD2}$ ) Power Dissipation	$T_S$ $P_{SO}$	150 2.78	$^{\circ}\text{C}$ W
INSULATION RESISTANCE AT $T_S$ , $V_{IO} = 500$ V	$R_{IO}$	$> 10^9$	$\Omega$

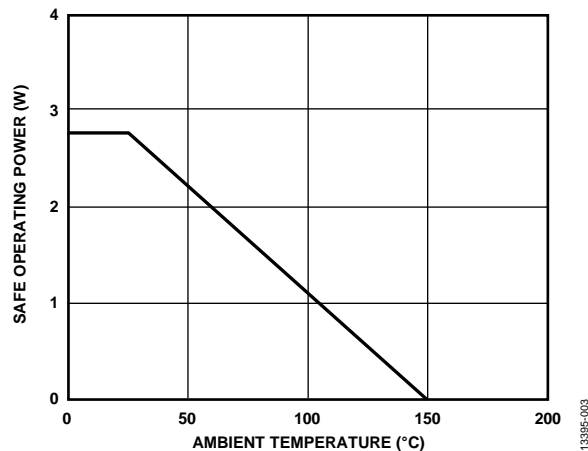


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. All voltages are relative to their respective ground.

Table 7.

Parameter	Rating
$V_{DD1}$ to $\text{GND}_1$	$-0.3\text{ V to }+6.5\text{ V}$
$V_{DD2}$ to $\text{GND}_2$	$-0.3\text{ V to }+6.5\text{ V}$
Analog Input Voltage to $\text{GND}_1$	$-1\text{ V to }V_{DD1} + 0.3\text{ V}$
Digital Input Voltage to $\text{GND}_2$	$-0.3\text{ V to }V_{DD2} + 0.5\text{ V}$
Output Voltage to $\text{GND}_2$	$-0.3\text{ V to }V_{DD2} + 0.3\text{ V}$
Input Current to Any Pin Except Supplies <sup>1</sup>	$\pm 10\text{ mA}$
Operating Temperature Range	$-55^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	$150^\circ\text{C}$
Pb-Free Temperature, Soldering	
Reflow	$260^\circ\text{C}$
ESD	$2\text{ kV}$
FICDM <sup>2</sup>	$\pm 1250\text{ V}$
HBM <sup>3</sup>	$\pm 4000\text{ V}$

<sup>1</sup> Transient currents of up to 100 mA do not cause SCR to latch up.

<sup>2</sup> JESD22-C101; RC network: 1  $\Omega$ , Cpkg; Class: IV.

<sup>3</sup> ESDA/JEDEC JS-001-2011; RC network: 1.5 k $\Omega$ , 100 pF; Class: 3A.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Max	Unit	Constraint
AC Voltage			
Bipolar Waveform	1250	$V_{PEAK}$	20-year minimum lifetime (VDE approved working voltage)
Unipolar Waveform	1250	$V_{PEAK}$	20-year minimum lifetime
DC Voltage	1250	$V_{PEAK}$	20-year minimum lifetime

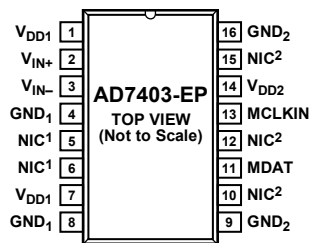
<sup>1</sup> Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



<sup>1</sup>NIC = NOT INTERNALLY CONNECTED. CONNECT TO  $V_{DD1}$ ,  $GND_1$ , OR LEAVE FLOATING.

<sup>2</sup>NIC = NOT INTERNALLY CONNECTED. CONNECT TO  $V_{DD2}$ ,  $GND_2$ , OR LEAVE FLOATING.

13395-004

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	$V_{DD1}$	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7403-EP and is relative to $GND_1$ . For device operation, connect the supply voltage to both Pin 1 and Pin 7. Decouple each supply pin to $GND_1$ with a 10 $\mu$ F capacitor in parallel with a 1 nF capacitor.
2	$V_{IN+}$	Positive Analog Input.
3	$V_{IN-}$	Negative Analog Input. Normally connected to $GND_1$ .
4, 8	$GND_1$	Ground 1. This pin is the ground reference point for all circuitry on the isolated side.
5, 6	NIC	Not Internally Connected. These pins are not internally connected. Connect to $V_{DD1}$ , $GND_1$ , or leave floating.
9, 16	$GND_2$	Ground 2. This pin is the ground reference point for all circuitry on the nonisolated side.
10, 12, 15	NIC	Not Internally Connected. These pins are not internally connected. Connect to $V_{DD2}$ , $GND_2$ , or leave floating.
11	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge.
13	MCLKIN	Master Clock Logic Input. 5 MHz to 20 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
14	$V_{DD2}$	Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to $GND_2$ . Decouple this supply to $GND_2$ with a 100 nF capacitor.



## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 5\text{ V}$ ,  $V_{IN+} = -250\text{ mV}$  to  $+250\text{ mV}$ ,  $V_{IN-} = 0\text{ V}$ ,  $f_{MCLKIN} = 16\text{ MHz}$ , using a sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

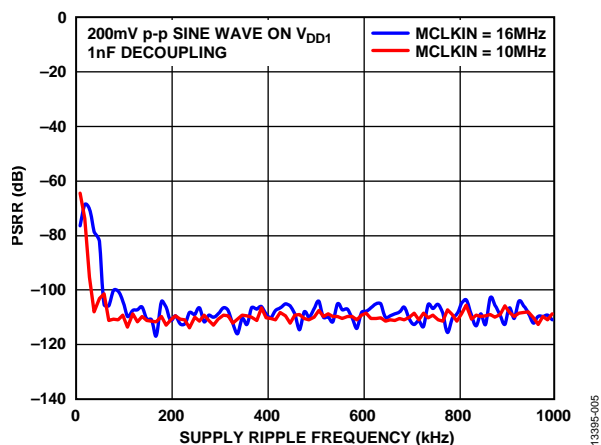


Figure 5. PSRR vs. Supply Ripple Frequency

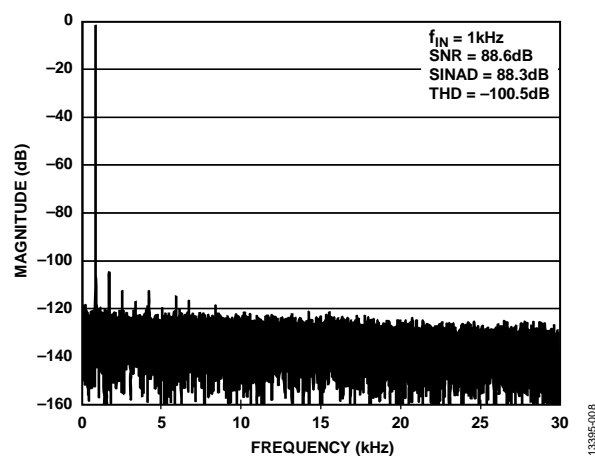


Figure 8. Typical Fast Fourier Transform (FFT)

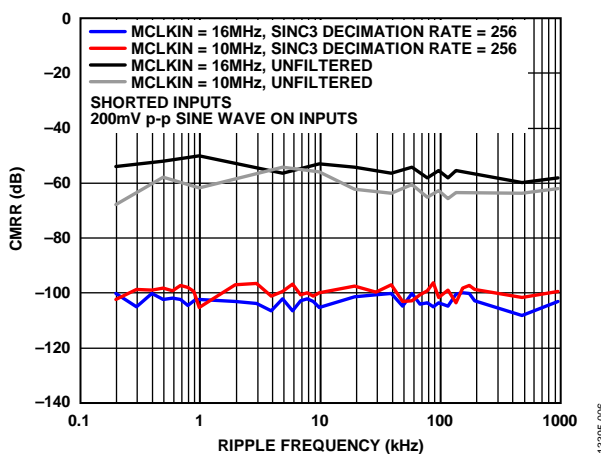


Figure 6. CMRR vs. Common-Mode Ripple Frequency

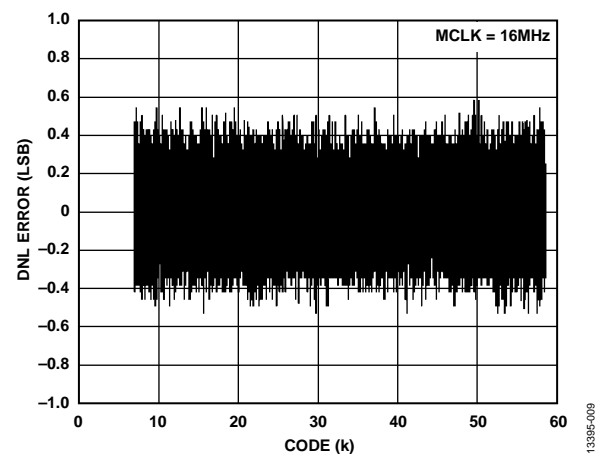


Figure 9. Typical DNL Error

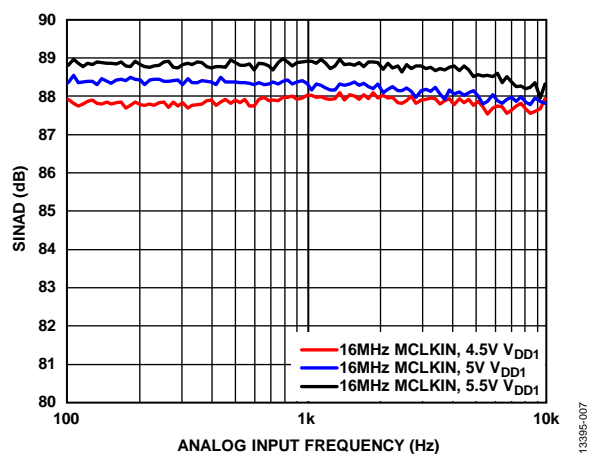


Figure 7. SINAD vs. Analog Input Frequency

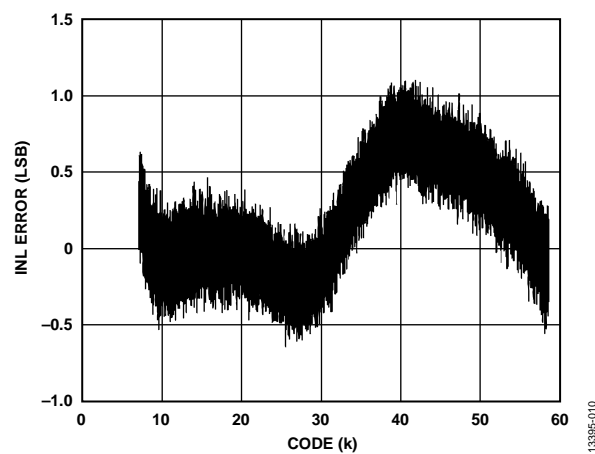


Figure 10. Typical INL Error

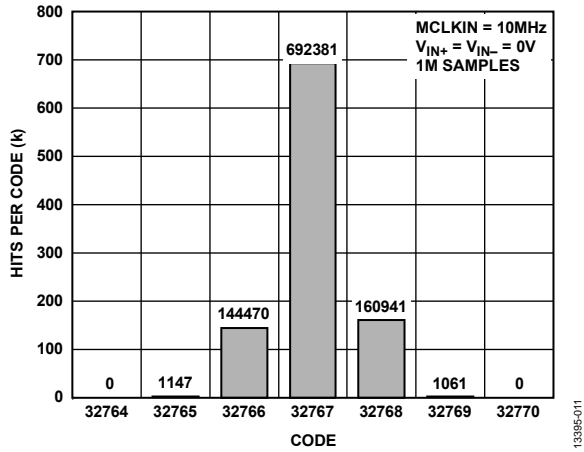


Figure 11. Histogram of Codes at Code Center

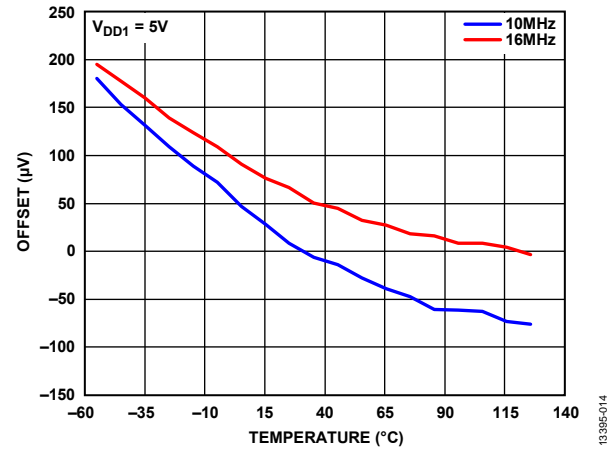


Figure 14. Offset vs. Temperature

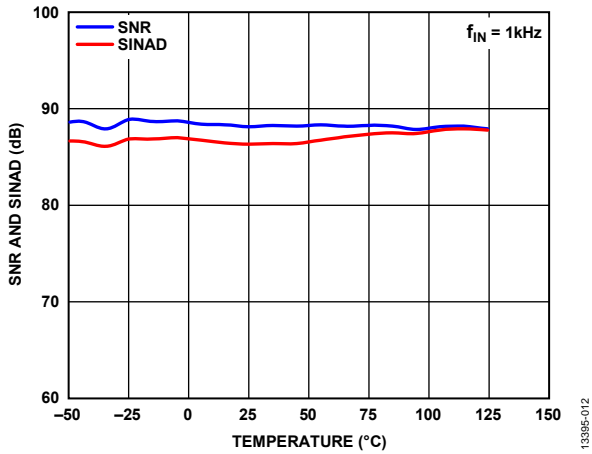


Figure 12. SNR and SINAD vs. Temperature

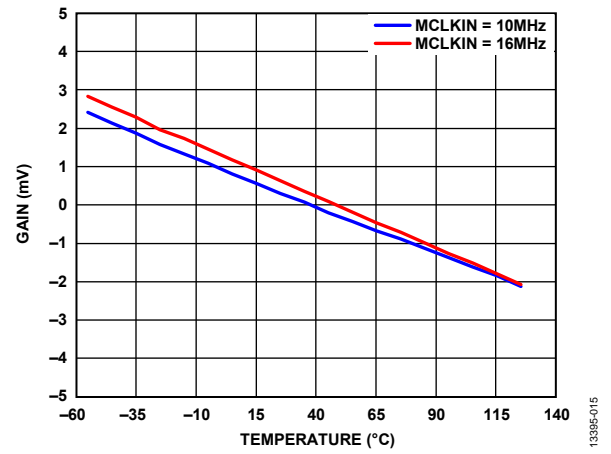


Figure 15. Gain Error vs. Temperature

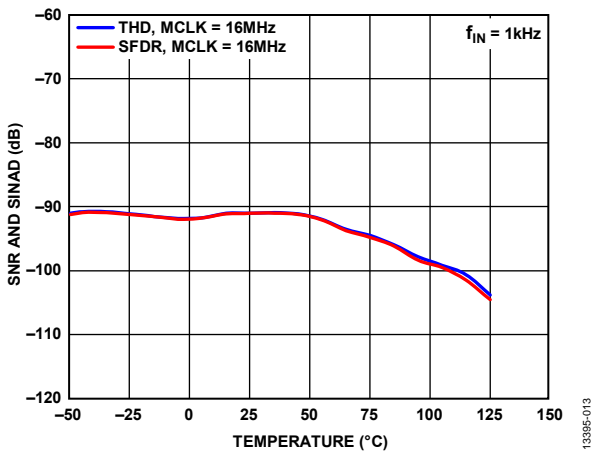
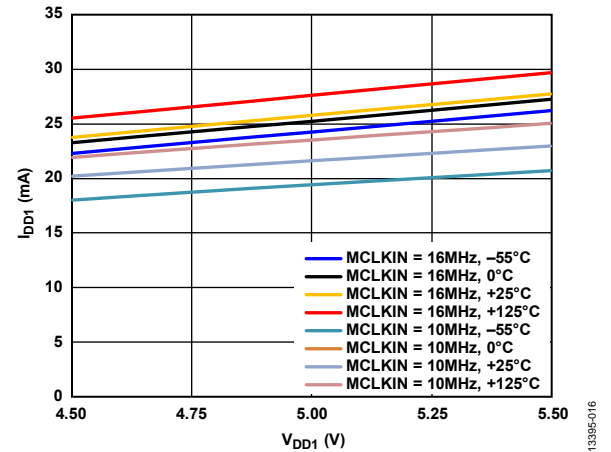
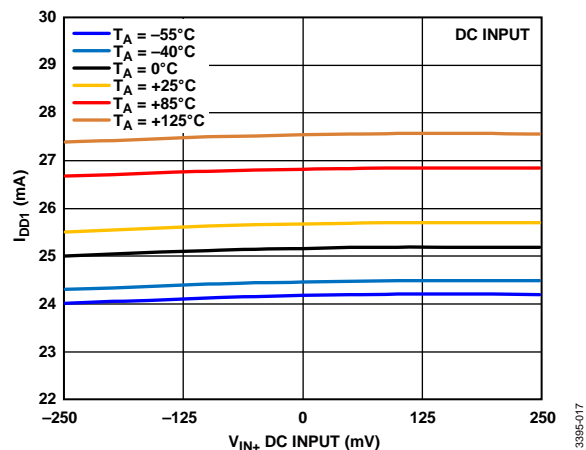
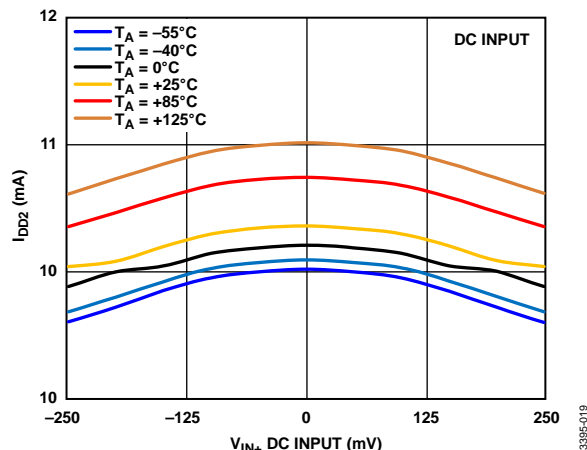
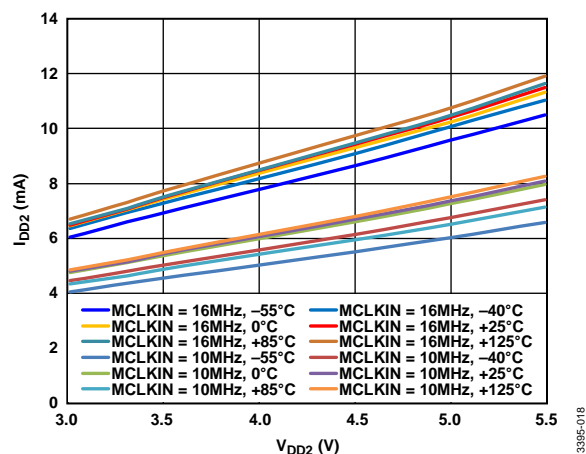
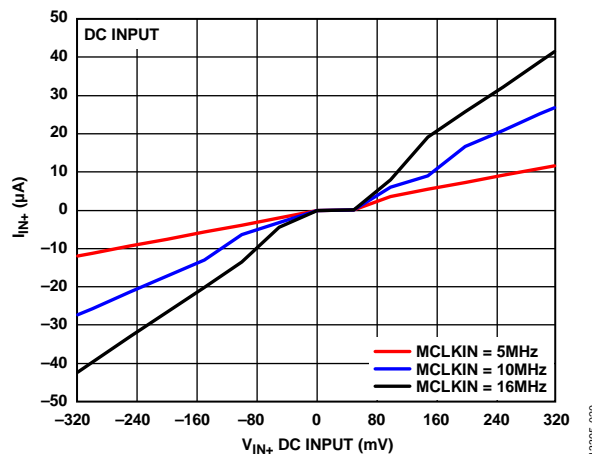


Figure 13. THD and SFDR vs. Temperature

Figure 16.  $I_{DD1}$  vs.  $V_{DD1}$  at Various Temperatures and Clock Rates

Figure 17.  $I_{DD1}$  vs.  $V_{IN+}$  DC Input at Various TemperaturesFigure 19.  $I_{DD2}$  vs.  $V_{IN+}$  DC Input at Various TemperaturesFigure 18.  $I_{DD2}$  vs.  $V_{DD2}$  at Various Temperatures and Clock RatesFigure 20.  $I_{IN+}$  vs.  $V_{IN+}$  DC Input at Various Clock Rates

## OUTLINE DIMENSIONS

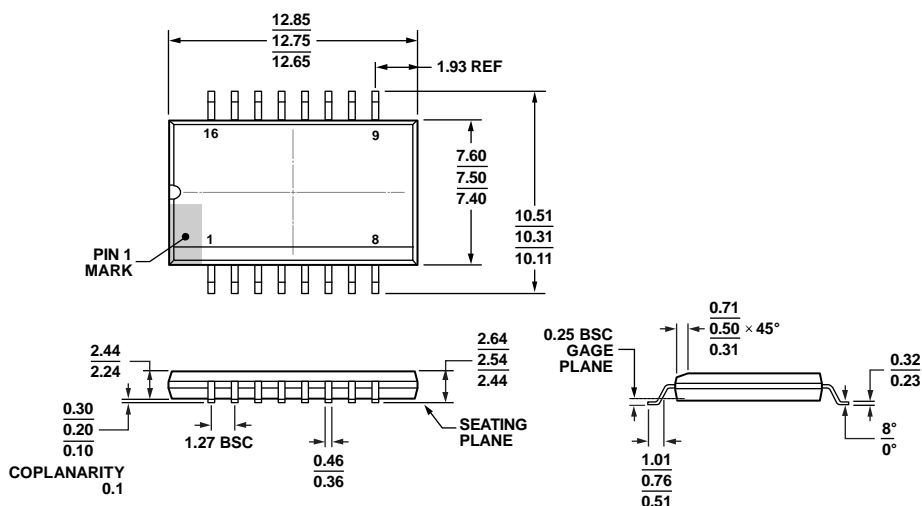


Figure 21. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC\_IC]  
Wide Body  
(RI-16-2)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD7403TRIZ-EP	–55°C to +125°C	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
AD7403TRIZ-EP-RL7	–55°C to +125°C	16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-16-2
EVAL-AD7403FMCZ		AD7403 Evaluation Board	
EVAL-SDP-CH1Z		System Demonstration Platform	

<sup>1</sup> Z = RoHS Compliant Part.