



PL60708X

PCIe Octal, Ultra-Low Jitter, HCSL Frequency Synthesizer

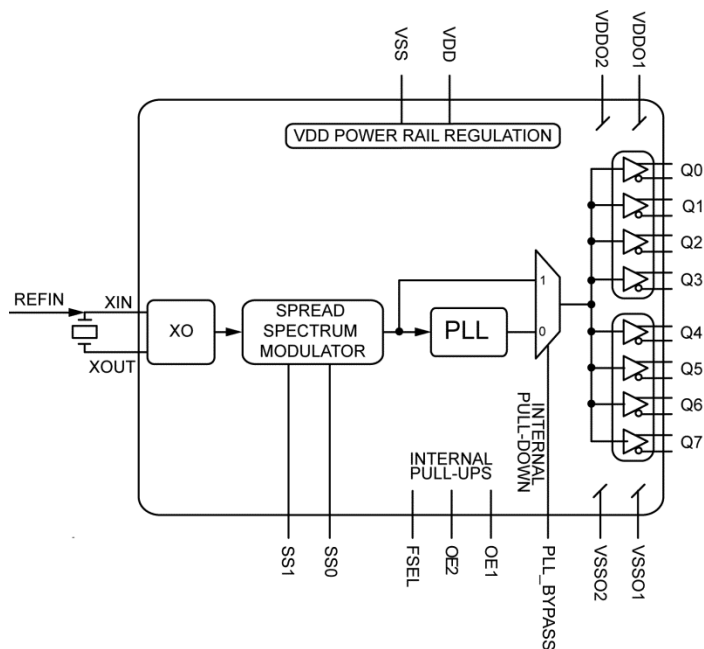
General Description

The PL607081 and PL607082 are members of the PCI Express family of devices from Micrel and provide extremely low-noise spread-spectrum clocks for PCI Express requirements.

The devices operate from a 3.3V or 2.5V power supply and synthesize eight HCSL output clocks. The PL607081 synthesizes 25MHz, 100MHz, or 200MHz frequencies and the PL607082 synthesizes 25MHz, 125MHz, or 250MHz frequencies. The PL60708x devices accept a 25MHz crystal or LVCMOS reference clock.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Generates eight HCSL clock outputs
- PL607081 output frequencies: 25MHz, 100MHz, or 200MHz
- PL607082 output frequencies: 25MHz, 125MHz, or 250MHz
- Spread spectrum for EMI reduction
- 2.5V or 3.3V operating range
- Typical phase jitter @ 100MHz: 320fs for 1.5MHz to 10MHz
- Compliant with PCI Express Gen1, Gen2, and Gen3
- Industrial temperature range (–40°C to +85°C)
- RoHS and PFOS compliant
- Available in a 44-pin 7mm × 7mm QFN package

Applications

- Servers
- Storage systems
- Switches and routers
- Gigabit Ethernet
- Set-top boxes/DVRs

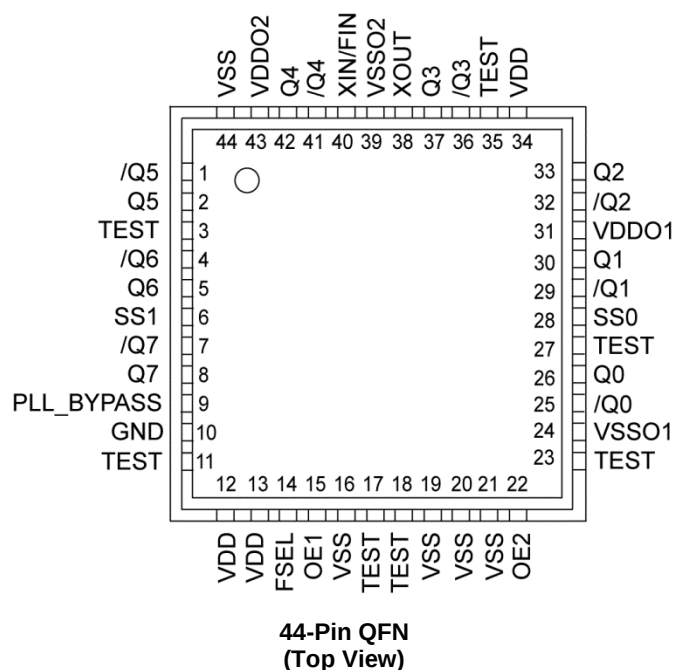
Ordering Information⁽¹⁾

Part Number	Marking	Shipping	Junction Temperature Range	Package
PL607081UMG	PL607 081	Tray	–40°C to +85°C	44-Pin QFN
PL607081UMG TR	PL607 081	Tape and Reel	–40°C to +85°C	44-Pin QFN
PL607082UMG	PL607 082	Tray	–40°C to +85°C	44-Pin QFN
PL607082UMG TR	PL607 082	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:

1. Devices are RoHS and PFOS compliant.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Name
1, 2 4, 5 7, 8 25, 26 29, 30 32, 33 36, 37 41, 42	/Q5, Q5 /Q6, Q6 /Q7, Q7 /Q0, Q0 /Q1, Q1 /Q2, Q2 /Q3, Q3 /Q4, Q4	O, (DIF)	HCSL	Differential clock output
14	FSEL	I, (SE)	LVC MOS	Frequency select, 45k Ω pull-up PL607081: 1 = 100MHz, 0 = 200MHz PL607082: 1 = 125MHz, 0 = 250MHz
12, 13, 34	VDD	PWR		Power supply
31	VDDO1	PWR		Power supply for outputs Q0–Q3
43	VDDO2	PWR		Power supply for outputs Q4–Q7
16, 19, 20, 21, 44	VSS (exposed pad)	PWR		Core power supply ground. The exposed pad must be connected to the VSS ground plane.
24	VSSO1	PWR		Power supply ground for outputs Q0–Q3
39	VSSO2	PWR		Power supply ground for outputs Q4–Q7
10	GND	I	LVC MOS	This pin is not a power supply ground but must be tied to VSS for proper operation.

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Name
9	PLL_BYPASS	I, (SE)	LVC MOS	PLL bypass, selects output source. 0 = normal PLL operation 1 = output from input reference clock or crystal 45k Ω pull-down
3, 11, 17, 18, 23, 27, 35	TEST			Factory test pins. Do not connect anything to these pins.
40	XIN/FIN	I, (SE)	15pF crystal	Crystal or reference clock input, no load caps needed (see Figure 7)
38	XOUT	O, (SE)	15pF crystal	Crystal output, no load caps needed (see Figure 7)
15	OE1	I, (SE)	LVC MOS	Output enable, outputs Q0–Q3 disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ω pull-up
22	OE2	I, (SE)	LVC MOS	Output enable, outputs Q4–Q7 disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ω pull-up
28	SS0	I, (SE)	LVC MOS	Spread-spectrum select, 60k Ω pull-up 0 = Spread OFF, 1 = Spread ON
6	SS1	I, (SE)	LVC MOS	Spread-spectrum select, 60k Ω pull-up 0 = –0.25%, 1 = Spread –0.50%

EMI Reduction

Spread-spectrum modulation reduces the emission of spectral components in the clock signal. The spectrum plot on the right (Figure 1) shows measurement results with the two spread settings versus no spread. This plot refers to the 11th harmonic in a 100MHz clock, at 1.1GHz. The scale is normalized to the strength of this spur without spread. The plot shows about 21dB reduction for -0.25% spread magnitude and 24dB for -0.50% spread magnitude.

The plot also shows how the frequency spreads downwards.

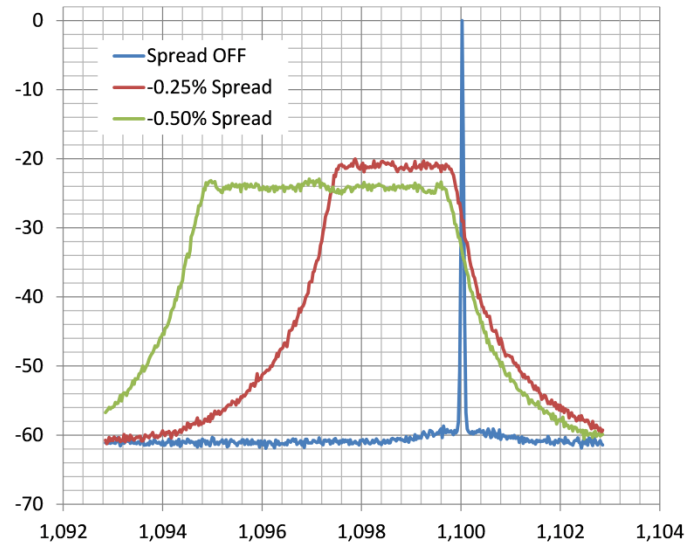


Figure 1. Spectrum Plot

Absolute Maximum Ratings⁽²⁾

Supply Voltage (V_{DD} , $V_{DDO1/2}$)	+4.6V
Input Voltage (V_{IN})	-0.50V to V_{DD} +0.5V
Lead Temperature (soldering, 20s)	260°C
Case Temperature	115°C
Storage Temperature (T_S)	-65°C to +150°C

Operating Ratings⁽³⁾

Supply Voltage (V_{DD} , $V_{DDO1/2}$)	+2.375V to +3.465V
Ambient Temperature (T_A)	-40°C to +85°C
Junction Thermal Resistance ⁽⁴⁾	
QFN (θ_{JA}) Still-Air	24°C/W
QFN (ψ_{JB}) Junction-to-Board	8°C/W

DC Electrical Characteristics⁽⁵⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD} , $V_{DDO1/2}$	2.5V Operating Range		2.375	2.5	2.625	V
V_{DD} , $V_{DDO1/2}$	3.3V Operating Range		3.135	3.3	3.465	V
I_{DD}	Supply Current $V_{DD} + V_{DDO}$	Eight outputs enabled, 100MHz Outputs 50Ω to V_{SS}		230	285	mA
		Eight outputs enabled, 200MHz Outputs 50Ω to V_{SS}		240	300	
		Four outputs enabled, 100MHz Outputs 50Ω to V_{SS} , OE1 or OE2 = 0		160	200	
		Four outputs enabled, 200MHz Outputs 50Ω to V_{SS} , OE1 or OE2 = 0		170	210	

HCSL DC Electrical Characteristics⁽⁵⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. $R_L = 50\Omega$ to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		660	700	850	mV
V_{OL}	Output Low Voltage		-150	0	27	mV
V_{CROSS}	Crossing Point Voltage		250	350	550	mV

Notes:

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
- Specification for packaged product only.

LVCMOS (PLL_BYPASS, FSEL, OE1, OE2, SS0, SS1) DC Electrical Characteristics⁽⁵⁾

$V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			μA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	15pF load	Fundamental, parallel resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			2	5	pF
Correlation Drive Level			10	100	μW

AC Electrical Characteristics^(4, 6)

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ C$ to $+85^\circ C$. $R_L = 50\Omega$ to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency	PL607081		25 100 200		MHz
		PL607082		25 125 250		MHz
F_{REF}	Crystal Input Frequency			25		MHz
F_{IN}	Reference Input Frequency			25		MHz
F_{IN}	F_{IN} Signal Amplitude	Internally AC Coupled	0.9		V_{DD}	V _{pp}
T_R/T_F	HCSL Output Rise/Fall Time	20%–80%	150	300	450	ps
ODC	Output Duty Cycle		48	50	52	%
T_{SKEW}	Output-to-Output Skew	Note 7			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\emptyset)$	RMS Phase Jitter ⁽⁸⁾	100MHz Integration Range (1.5MHz to 10MHz)		320		fs
	Cycle to Cycle Jitter				30	ps, peak

Spread Spectrum Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Modulation Rate ⁽⁹⁾			31.6		kHz
Modulation Magnitude ⁽¹⁰⁾	Setting is –0.25%	-0.073 to -0.265	0 to –0.250	+0.031 to -0.375	%
	Setting is –0.50%	-0.136 to -0.383	0 to –0.500	+0.078 to -0.589	%

Notes:

6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions; measured at the output differential crossing points.
8. Measured using a 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise follows the input source phase noise up to about 1MHz.
9. The modulation rate is the crystal frequency divided by 792.
10. The typical modulation makes the output frequency sweep between the target frequency (0%) and the down-spread value (–0.25% or –0.5%). There is process variation on the modulation magnitude; the smallest and largest possible modulation magnitude sweep ranges are listed in the Spread Spectrum Characteristics table.

Truth Tables

OE2	OE1	OUTPUT
0	1	Q4-Q7 Tri-state
1	0	Q0-Q3 Tri-state

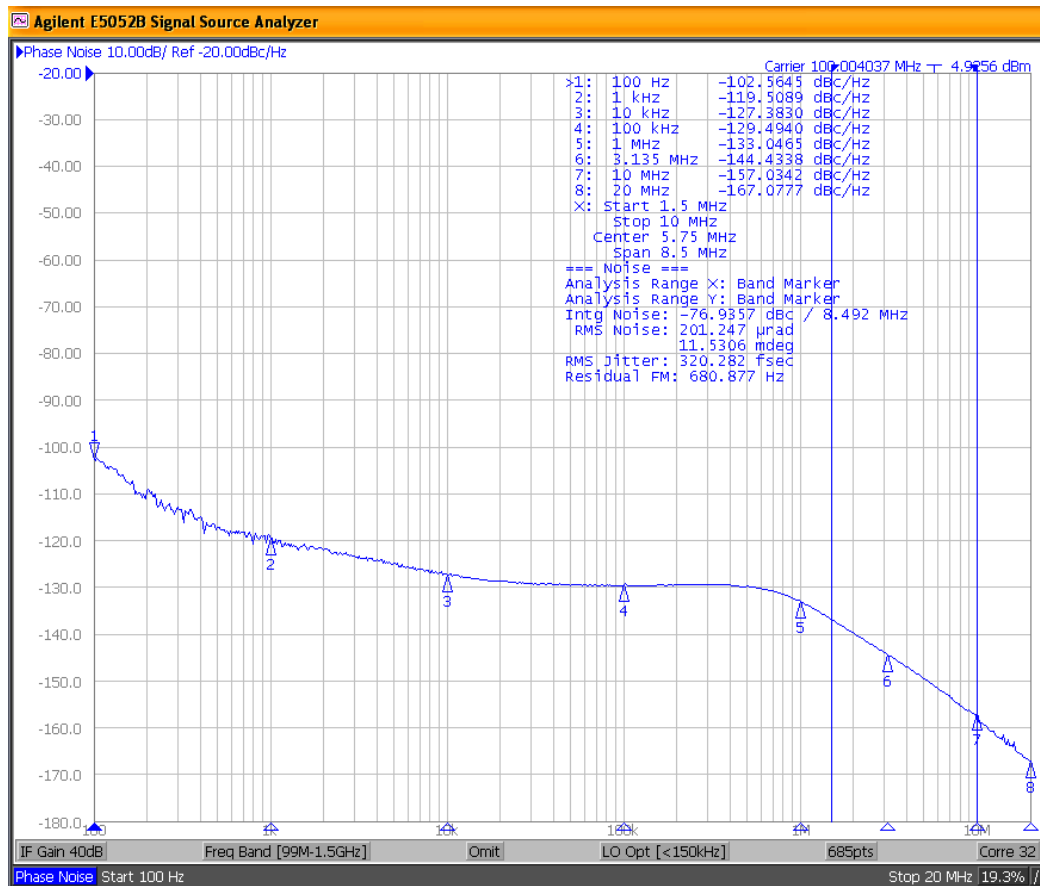
FSEL	PLL_BYPASS	Output Frequency (MHz)	
		PL607081	PL607082
0	0	200	250
1	0	100	125
X	1	25	25

SS1 ⁽¹¹⁾	SS0 ⁽¹¹⁾	Spread Type	Spread
0	0	Spread is OFF	No Spread
0	1	Down Spread	–0.25%
1	0	Spread is OFF	No Spread
1	1	Down Spread	–0.50%

Note:

11. SS0 turns ON/OFF spread-spectrum modulation and SS1 selects the spread magnitude.

Phase Noise Plot



Phase Noise Plot: 100MHz, 1.5MHz to 10MHz 320fs

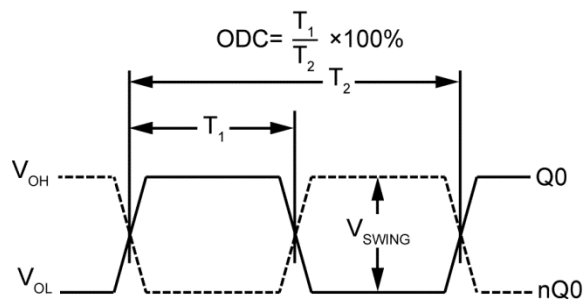


Figure 2. Duty Cycle Timing

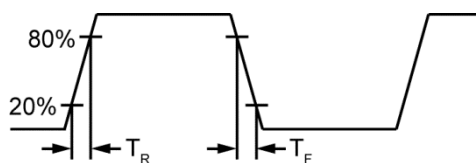
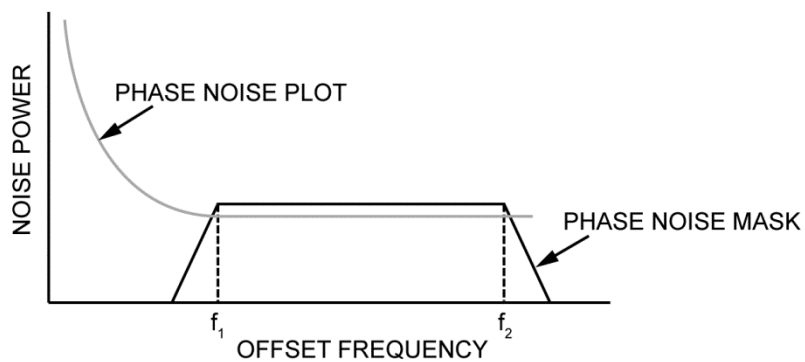


Figure 3. All Outputs Rise/Fall Time

RMS PHASE NOISE/JITTER



$$RMS \text{ JITTER} = \sqrt{\text{AREA UNDER THE MASKED PHASE NOISE PLOT}}$$

Figure 4. RMS Phase/Noise Jitter

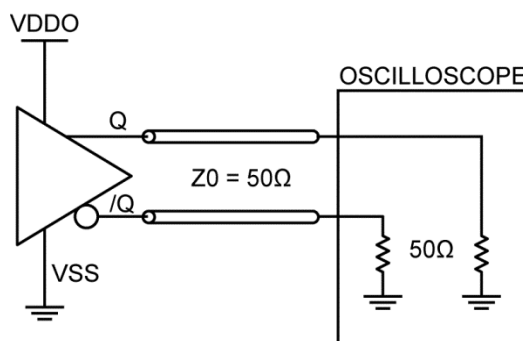


Figure 5. HCSL Output Load and Test Circuit

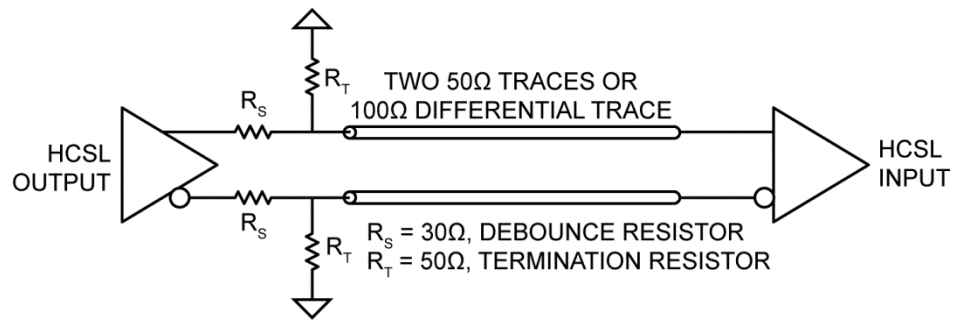


Figure 6. HCSL Recommended Application Termination (source terminated)

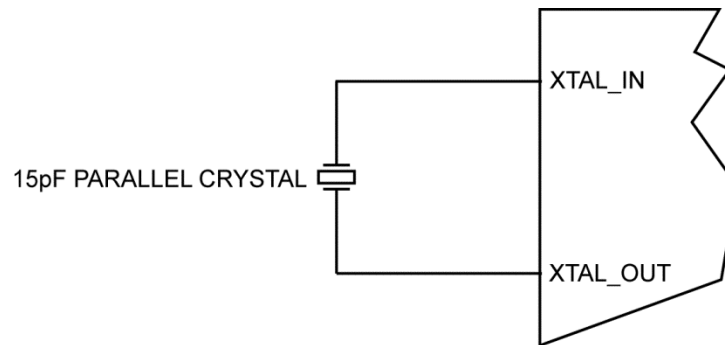


Figure 7. Crystal Input Interface

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex Family of Precision Synthesizers* application note for more details.

Contact Micrel's HBW applications group at: tcghelp@micrel.com if you need help selecting a suitable crystal for your application

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL60708X.

The impedance value of the ferrite bead (FB) must be between 240Ω and 600Ω with a saturation current $\geq 150\text{mA}$.

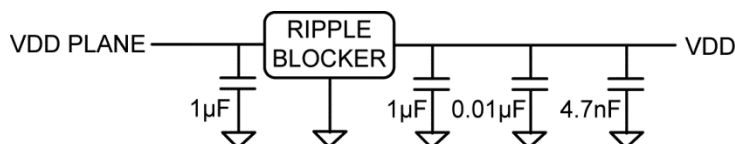
The VDDO1 and VDDO2 pins connect directly to the VDD plane. All VDD pins on the PL60708X connect to VDD after the power supply filter.

HCSL Outputs

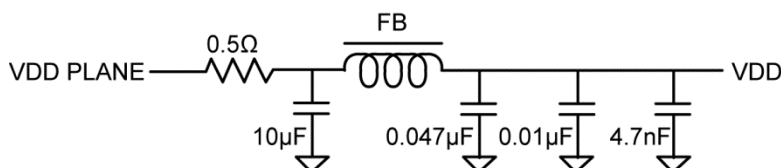
Terminate HCSL outputs with 50Ω to V_{SS} . For best performance, load all outputs. If you want to AC-couple or change the termination, contact Micrel's applications group at: tcghelp@micrel.com (see Figure 6).

Power Supply Filtering Recommendations

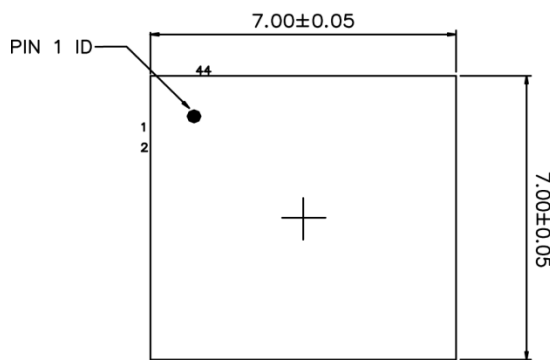
Preferred filter, using Micrel MIC94300 or MIC94310 Ripple Blocker™:



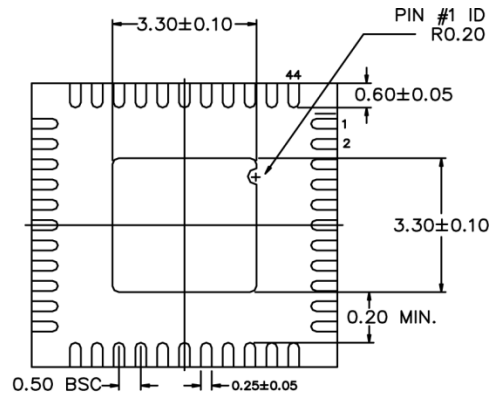
Alternative, traditional filter, using a ferrite bead:



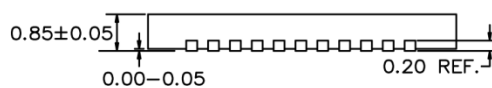
Package Information⁽¹²⁾



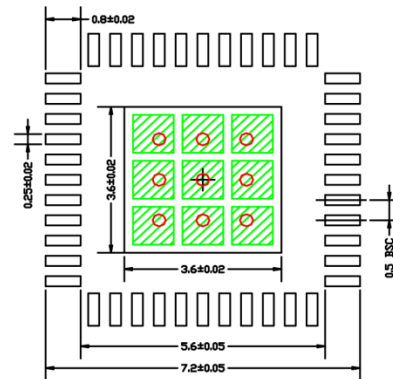
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX. PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

44-Pin QFN

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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