256K x 16 Static RAM

Features

- High Speed
  - 55 ns and 70 ns availability
- Low voltage range:
  - CY62147CV18: 1.65V–1.95V
- Pin Compatible w/ CY62147V18/BV18
- Ultra-low active power
  - Typical Active Current: 0.5 mA @ f = 1 MHz
  - Typical Active Current: 2 mA @ $f = f_{max}$ (70 ns speed)
- Low standby power
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

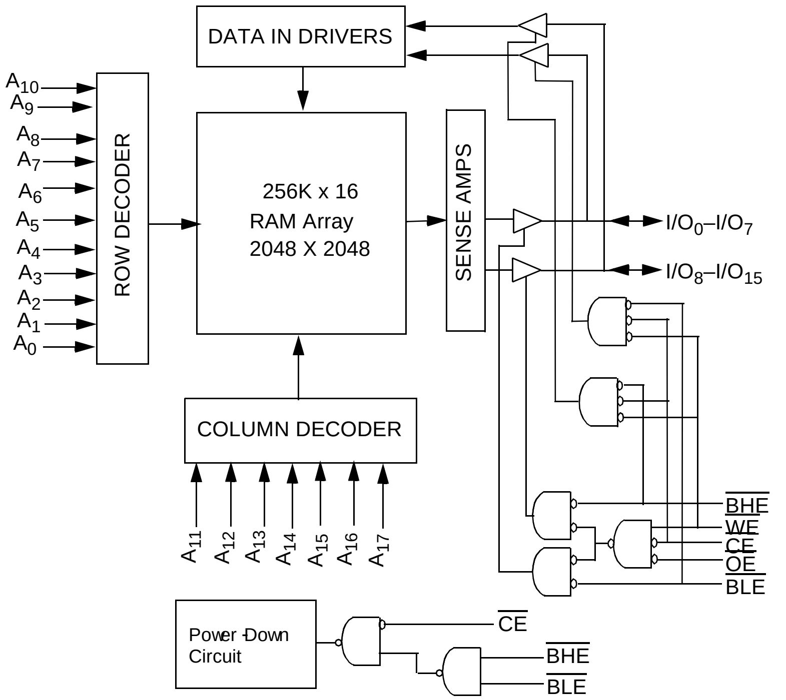
The CY62147CV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{\text{CE}}$ HIGH or both $\overline{\text{BLE}}$ and $\overline{\text{BHE}}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62147CV18 is available in a 48-ball FBGA package.

Logic Block Diagram



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Pin Configuration[1, 2]

FBGA
Top View

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{ccq}
E	V_{CC}	I/O_{12}	DNU	A_{16}	I/O_4	V_{ssq}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.2V to +2.4V

DC Voltage Applied to Outputs
in High Z State[3] .... –0.2V to V_{CC} + 0.2V

DC Input Voltage[3].................................. –0.2V to V_{CC} + 0.2V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62147CV18	Industrial	–40°C to +85°C	1.65V to 1.95V

Product Portfolio

					Power Dissipation (Industrial)					
					Operating (I_{CC})				Standby (I_{SB2})	
	V_{CC} Range				f = 1 MHz		f = f_{max}			
Product	$V_{CC(min.)}$	$V_{CC(typ.)}$[4]	$V_{CC(max.)}$	Speed	Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.
CY62147CV18	1.65V	1.80V	1.95V	55 ns	0.5 mA	3 mA	2.5 mA	7 mA	1 µA	10 µA
				70 ns	0.5 mA	3 mA	2 mA	6 mA		

Notes:

1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
3. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$ Typ, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62147CV18-55			CY62147CV18-70			Unit
				Min.	Typ.[4]	Max.	Min.	Typ.[4]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	V_{CC} = 1.65V	1.4			1.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V			0.2			0.2	V
V_{IH}	Input HIGH Voltage			1.4		V_{CC} + 0.2V	1.4		V_{CC} + 0.2V	V
V_{IL}	Input LOW Voltage			–0.2		0.4	–0.2		0.4	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = 1.95V I_{OUT} = 0 mA CMOS levels		2.5	7		2	6	mA
		f = 1 MHz			0.5	3		0.5	3	mA
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$)			1	10		1	10	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, V_{CC} = 1.95V								

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

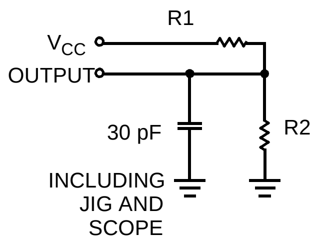
Thermal Resistance

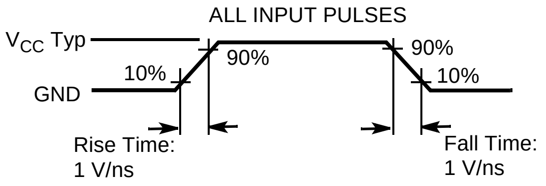
Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient)[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance (Junction to Case)[5]		Θ_{JC}	16	°C/W

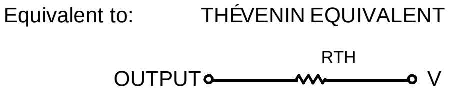
Note:

[5] Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





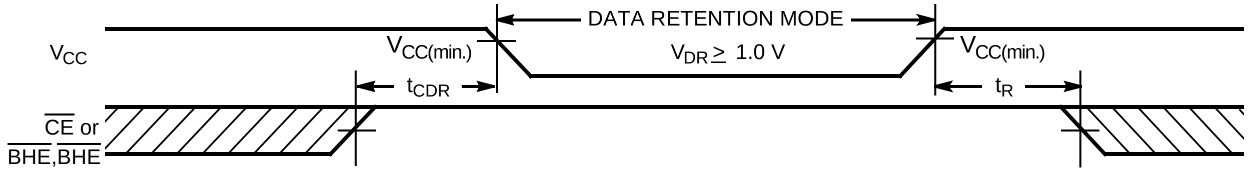


Parameters	1.8V	UNIT
R1	13500	Ohms
R2	10800	Ohms
R_{TH}	6000	Ohms
V_{TH}	0.80	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		1.95	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$ $\overline{CE} \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$		1	8	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0			ns
t_R[6]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform[7]



Notes:

6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100$ µs or stable at $V_{CC(min)} \ge 100$ µs.
7. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$.

Switching Characteristics Over the Operating Range[8]

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	5		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[9]	5		5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[9, 10]		20		25	ns
WRITE CYCLE[11]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		60		ns
t_{AW}	Address Set-Up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to Write End	40		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		15		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	5		10		ns

Notes:

[8] Test conditions assume signal transition time of 3ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

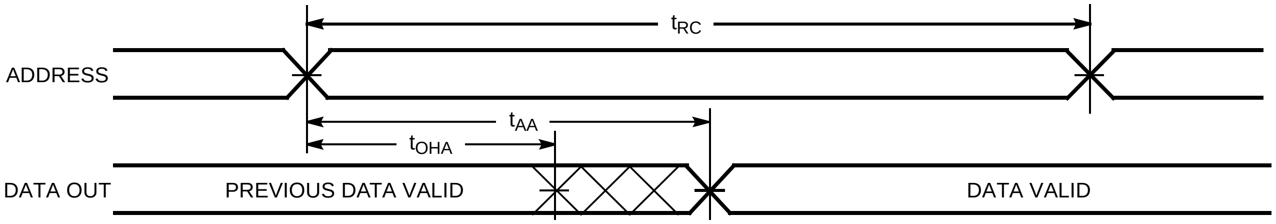
[9] At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

[10] t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

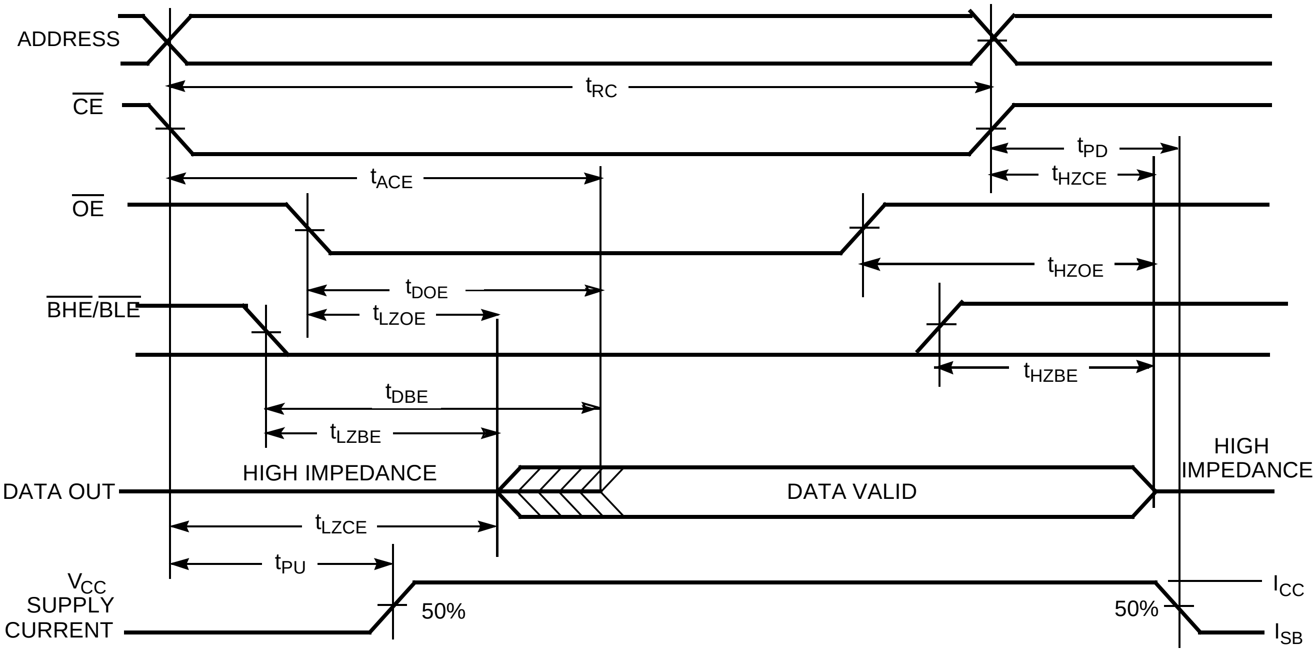
[11] The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[12, 13]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]

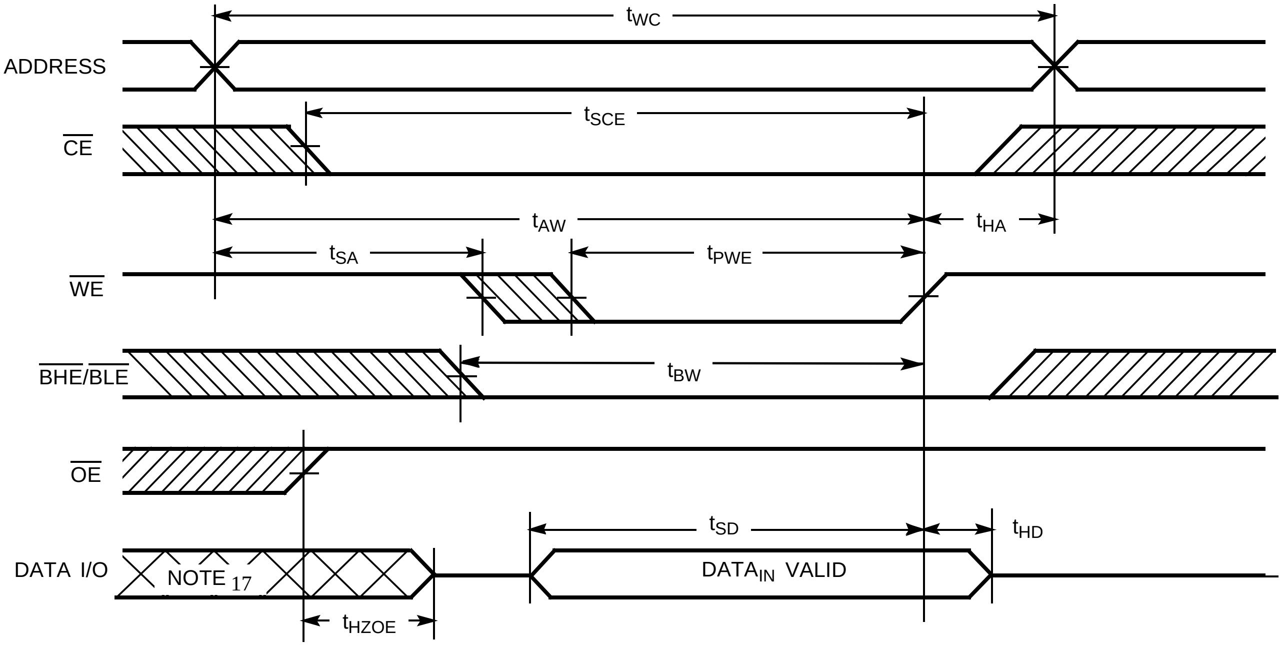


Notes:

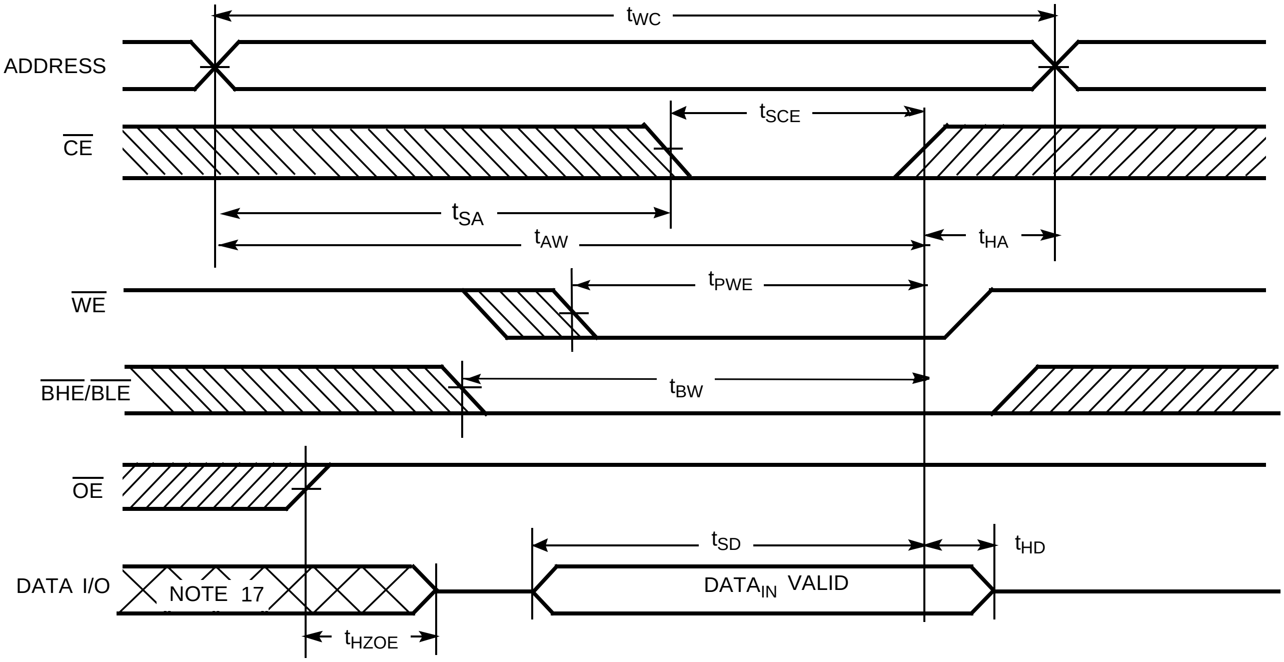
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$, transition LOW.

Switching Waveforms

Write Cycle No. 1(WE Controlled)[11, 15, 16]



Write Cycle No. 2 (CE Controlled)[11, 15, 16]

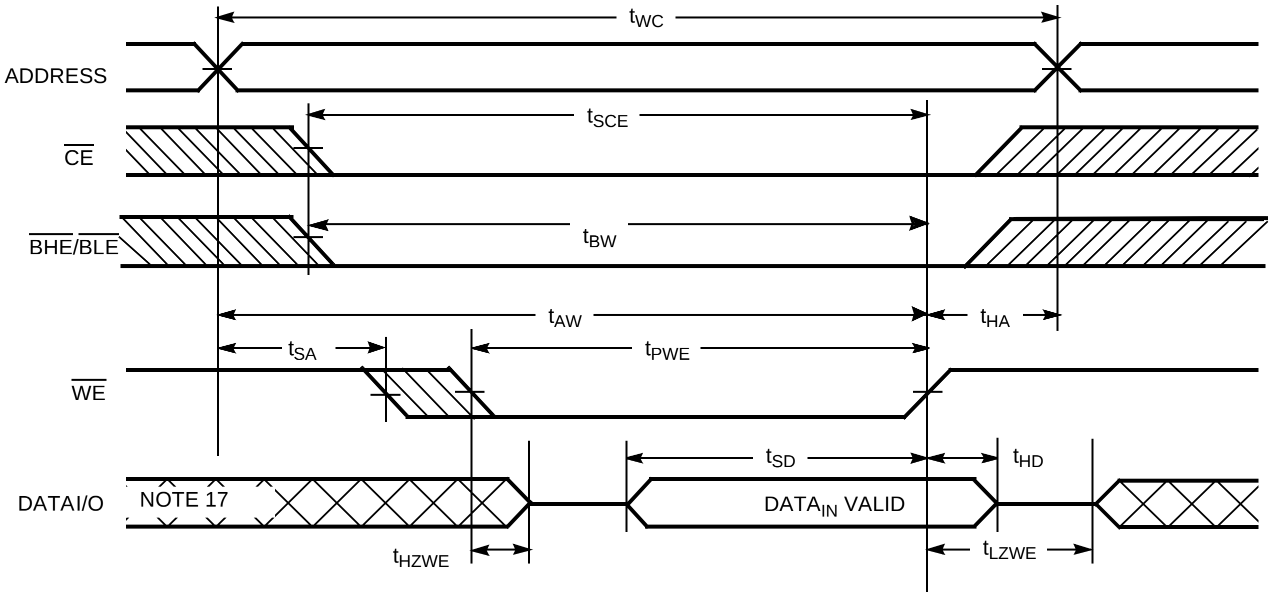


Notes:

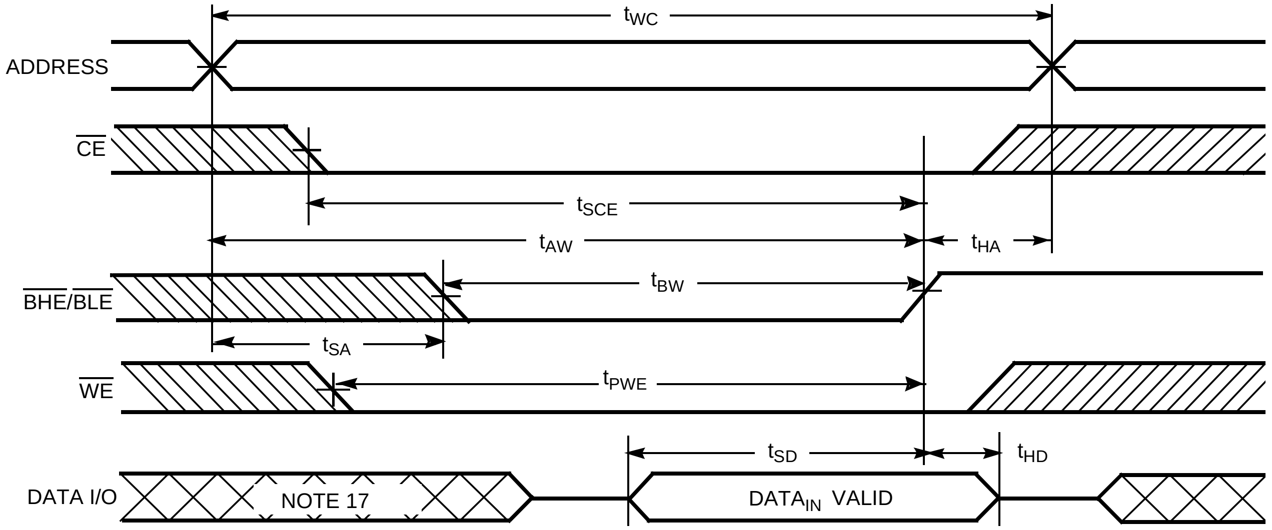
15. Data I/O is high impedance if OE = V_{IH}.
16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]

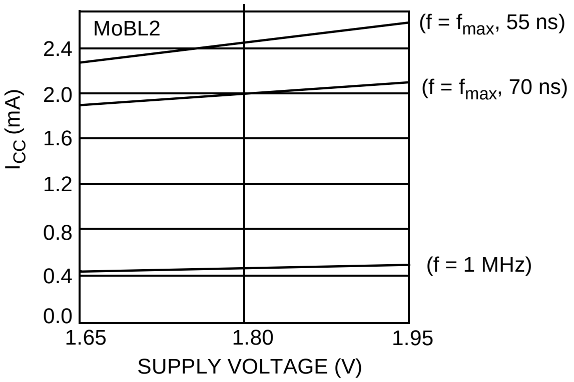


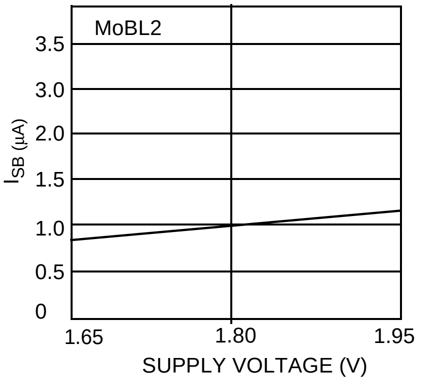
Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[16]

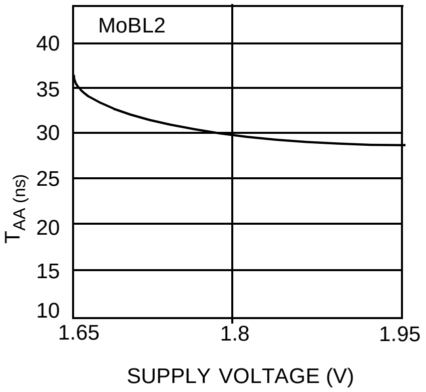


Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ Typ, $T_A = 25°C$.)


Operating Current vs. Supply Voltage


Standby Current vs. Supply Voltage


Access Time vs. Supply Voltage

Truth Table

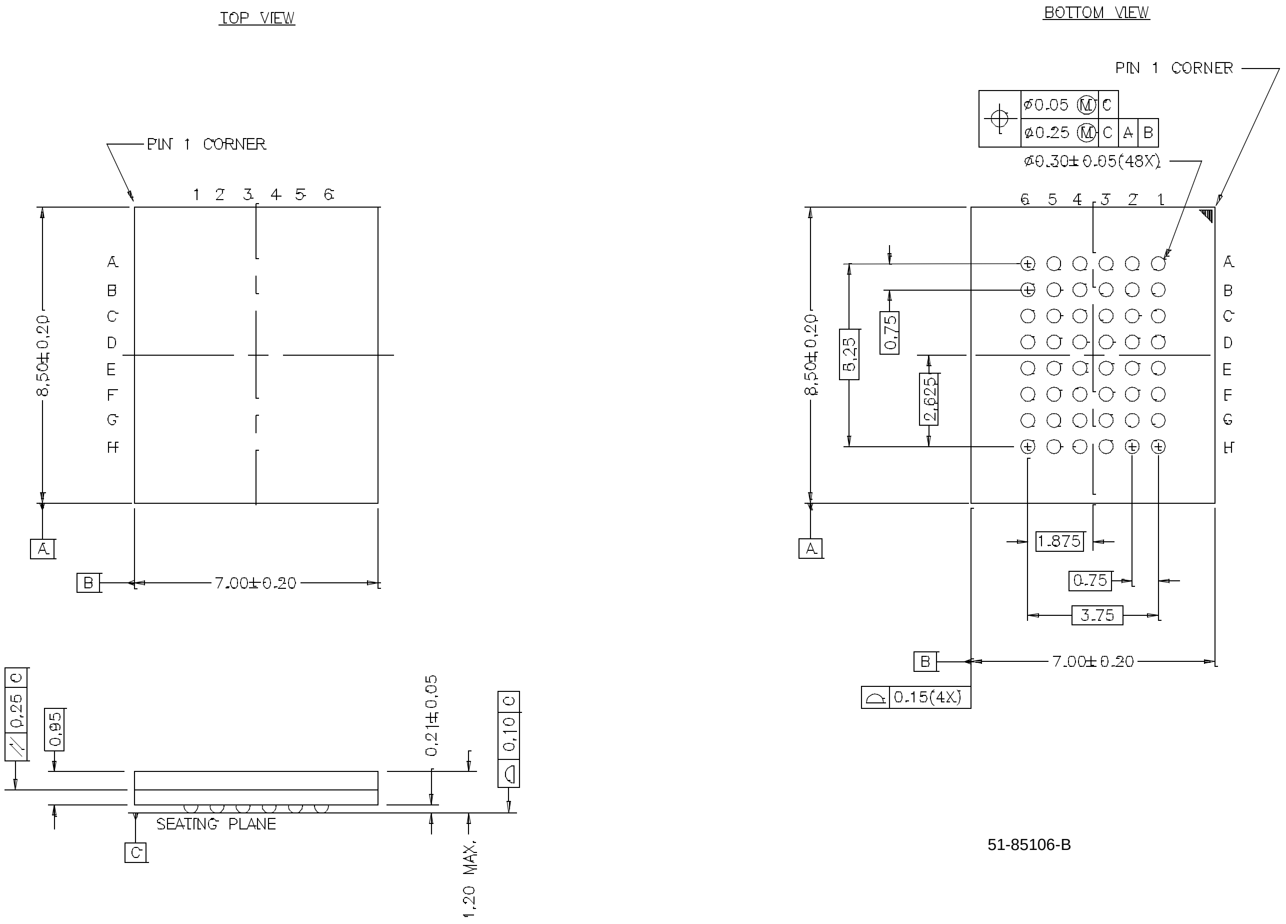
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information[18]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV18LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV18LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62147CV18LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV18LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams

48-Ball (7 mm x 8.5 mm x 1.2 mm) Fine Pitch BGA BA48B

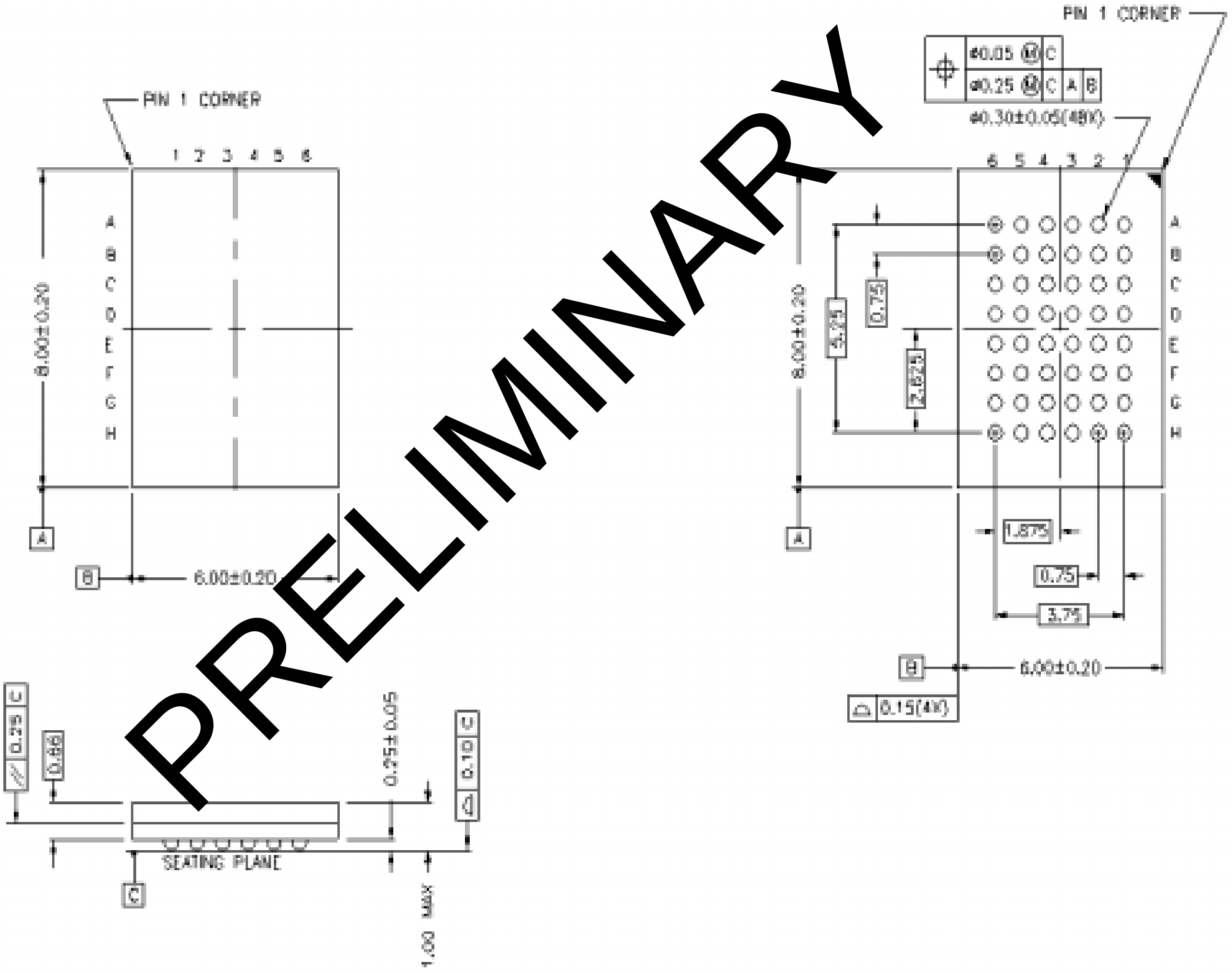


Note:

18. Gray Shading represents preliminary information.

Package Diagrams (continued)

48-Ball (6 mm x 8 mm x 1 mm) Fine Pitch BGA BV48A



Top View

Bottom View

Document Title: CY62147CV18 MoBL2™, 256K x 16 Static RAM **Document Number: 38-05011**				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106265	5/7/01	HRT/MGN	New Data Sheet
*A	108941	08/24/01	MGN	From Preliminary to Final
*B	110573	11/02/01	MGN	Improved I_{SB} Typ. from 1.5 µA to 1 µA. Improved Typical DC & AC Characteristics graphs. Improved Switching Characteristics: t_{OHA}, t_{LZCE}. Add preliminary package diagram of BV48A. Format standardization