0.75-Ω DUAL SPST ANALOG SWITCH WITH 1.8-V COMPATIBLE INPUT LOGIC

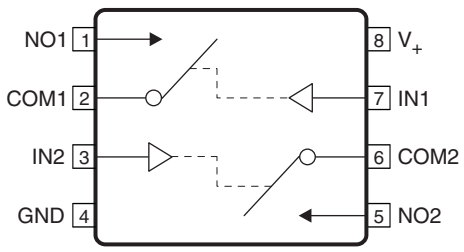
FEATURES

- Dual Single-Pole Single-Throw (SPST) Switch
- 1.65-V to 5.5-V Power Supply (V_+)
- Isolation in Powerdown Mode, V_+ = 0
- Low ON-State Resistance (0.75 Ω Typ)
- Excellent ON-State Resistance Matching
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- High Bandwidth (260 MHz)
- 1.8-V Compatible Control Input Threshold Independent of V_+
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

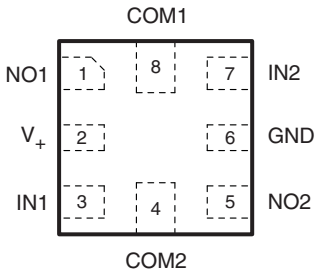
APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Portable Media Players
- Communication Circuits
- Computer Peripherals

DCU PACKAGE
(TOP VIEW)



RSE PACKAGE
(TOP VIEW)



DESCRIPTION

The TS5A21366 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power.

The control pin can be connected to a low voltage GPIO allowing it to be controlled by 1.8-V signals.

These features make this device ideal for portable audio applications.

The TS5A21366 is available in a small, space-saving 8-pin DCU or RSE package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	VSSOP – DCU	Tape and reel	TS5A21366DCUR	JBS_
	QFN – RSE	Tape and reel	TS5A21366RSER	4F

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SUMMARY OF CHARACTERISTICS(1)

Configuration	Single-pole, single-throw (SPST)
Number of channels	2
ON-state resistance (r_{ON})	0.75 Ω
ON-state resistance match (Δr_{ON})	0.04 Ω
ON-state resistance flatness ($r_{ON(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	49 ns/243 ns
Charge injection (Q_C)	1.3 pC
Bandwidth (BW)	260 MHz
OFF isolation (O_{ISO})	–62 dB at 1 MHz
Crosstalk (X_{TALK})	–98 dB at 1 MHz
Total harmonic distortion (THD)	0.002%
Power-supply current (I_+) with V_{IN} = 1.8 V	7.6 µA
Package option	8-pin QFN (RSE) or VSSOP (DCU)

(1) V_+ = 5 V, T_A = 25°C

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
DCU PIN NO.	RSE PIN NO.	NAME	
1	1	NO1	Switch 1, normally open
2	8	COM1	Switch 1, common
3	7	IN2	Switch 2, digital control pin to connect COM to NO
4	6	GND	Digital ground
5	5	NO2	Switch 2, normally open
6	4	COM2	Switch 2, common
7	3	IN1	Switch 1, digital control pin to connect COM to NO
8	2	V_+	Power supply

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	ON-state switch current	$V_{NO,}$ V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)		–400	400	
V_I	Digital input voltage range(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle

THERMAL IMPEDANCE

				UNIT
θ_{JA}	Package thermal impedance(1)	DCU package	227	°C/W
		RSE package	253	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Power supply voltage range(1)	1.65	5.5	V
V_{NO} V_{COM}	Analog signal voltage range	0	V_+	V
V_{IN}	Control input voltage range	0	5.5	V
T_A	Ambient temperature	–40	85	°C

(1) V_+ needs to be supplied prior to the control input, refer to the Application Information section.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.75	1	Ω
				Full				1.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.15	0.25	Ω
				Full				0.25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 16	25°C	5.5 V	–10	1.4	10	nA
						–235		235	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		Full	0 V	–5	0.06	5	µA
						–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, See Figure 16	25°C	5.5 V	–10	1.4	10	nA
				Full		–235		235	
	$I_{COM(PWROFF)}$	V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–5	0.06	5	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	5.5 V	–5	1.33	5	nA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	5.5 V	–5	1.33	5	nA
				Full		–50		50	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full	5.5 V	1.05		5.5	V
Input logic low	V_{IL}			Full	5.5 V	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or GND		Full	5.5 V	–0.6		0.6	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	5.5 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	5 V	39	49	72	ns
				Full	4.5 V to 5.5 V	28		97	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V	168	243	318	ns
				Full	4.5 V 5.5 V	178		323	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	5 V		1.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	5 V		17		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 18	25°C	5 V		33		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	5 V		33		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 18	25°C	5 V		2.5		pF
Power supply rejection ratio	PSRR	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	5 V		–84		dB
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	5 V		260		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	5 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	5 V		–98		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.002		%
Supply									
Positive supply current	I_+	V_I = 1.95 V or GND	Switch ON or OFF	25°C	5.5 V		7.6	9	µA
				Full				10	

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		1.1	1.5	Ω
				Full				1.8	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2 V, 0.8 V I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		0.045	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		0.15	0.25	Ω
				Full				0.25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, 1 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 16	25°C	3.6 V	–5	0.9	5	nA
						–160		160	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		Full	0 V	–5	0.03	5	µA
						–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 3 V, V_{COM} = 1 V, or V_{NO} = 1 V, V_{COM} = 3 V,	Switch OFF, See Figure 16	25°C	3.6 V	–5	0.9	5	nA
				Full		–160		160	
	$I_{COM(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–5	0.03	5	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	3.6 V	–2	1	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	See Figure 17	25°C	3.6 V	–2	1	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full	3.6 V	1.05		5.5	V
Input logic low	V_{IL}			Full	3.6 V	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or GND		Full	3.6 V	–0.6		0.6	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	3.6 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	3.3 V	66	83	133	ns
				Full	3 V to 3.6 V	43		178	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V	138	247	306	ns
				Full	3 V to 3.6 V	204		329	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		1.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		17		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 18	25°C	3.3 V		30		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	3.3 V		30		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 18	25°C	3.3 V		2.5		pF
Power supply rejection ratio	PSRR	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	3.3 V		–84		dB
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	3.3 V		260		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	3.3 V		–62		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	3.3 V		–99		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.004		%
Supply									
Positive supply current	I_+	V_I = 1.95 V or GND	Switch ON or OFF	25°C	3.6 V		6.8	9	µA
				Full				10	

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		1.2	2.1	Ω
				Full				2.7	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		0.045	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		0.4	0.6	Ω
				Full				0.6	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 16	25°C	2.7 V	–8	0.7	8	nA
						–136		136	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		Full	0 V	–5	0.02	5	µA
						–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 2.3 V, V_{COM} = 0.5 V, or V_{NO} = 0.5 V, V_{COM} = 2.3 V,	Switch OFF, See Figure 16	25°C	2.7 V	–8	0.7	8	nA
				Full		–136		136	
	$I_{COM(PWROFF)}$	V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		25°C	0 V	–5	0.02	5	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	2.7 V	–2	0.3	2	nA
				Full		–15		15	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.3 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	2.7 V	–2	0.3	2	nA
				Full		–15		15	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full	2.7 V	1.05		5.5	V
Input logic low	V_{IL}			Full	2.7 V	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or GND		Full	2.7 V	–0.6		0.6	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	2.7 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	2.5 V	101	137	222	ns
				Full	2.3 V to 2.7 V	68		288	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	148	264	333	ns
				Full	2.3 V to 2.7 V	197		367	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		1.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		17		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 18	25°C	2.5 V		27.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	2.5 V		27.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 18	25°C	2.5 V		2.5		pF
Power supply rejection ratio	PSRR	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	2.5 V		–84		dB
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	2.5 V		260		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	2.5 V		–61		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	2.5 V		–99		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.011		%
Supply									
Positive supply current	I_+	V_I = 1.95 V or GND	Switch ON or OFF	25°C	2.7 V		6.6	9	µA
				Full				10	

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}								V
ON-state resistance	r_{on}	V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		1.6	4	Ω
				Full				5	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		0.045	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		1.7	2.8	Ω
				Full				3	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 16	25°C	1.95 V	–10	0.5	10	nA
						–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		Full	0 V	–5	0.02	5	µA
						–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 1.65 V, V_{COM} = 0.3 V, or V_{NO} = 0.3 V, V_{COM} = 1.65 V,	Switch OFF, See Figure 16	25°C	1.95 V	–10	0.5	10	nA
				Full		–30		30	
	$I_{COM(PWROFF)}$	V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		25°C	0 V	–5	0.02	5	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.2	2	nA
				Full		–15		15	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.3 V, V_{NO} = Open, or V_{COM} = 1.65 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.2	2	nA
				Full		–15		15	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full	1.95 V	1.05		5.5	V
Input logic low	V_{IL}			Full	1.95 V	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or GND		Full	1.95 V	–0.6		0.6	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	1.95 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	1.8 V	198	297	448	ns
				Full	1.65 V to 1.95 V	136		620	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V	225	308	430	ns
				Full	1.65 V to 1.95 V	204		514	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	1.8 V		1.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	1.8 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	1.8 V		17		pF
NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 18	25°C	1.8 V		27.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	1.8 V		27.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 18	25°C	1.8 V		2.5		pF
Power supply rejection ratio	PSRR	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	1.8 V		–78		dB
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	1.8 V		260		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	1.8 V		–59		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	1.8 V		–101		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.001		%
Supply									
Positive supply current	I_+	V_I = 1.95 V or GND	Switch ON or OFF	25°C	1.95 V		3.6	9	µA
				Full				10	

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NO1 to NO2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

TYPICAL PERFORMANCE

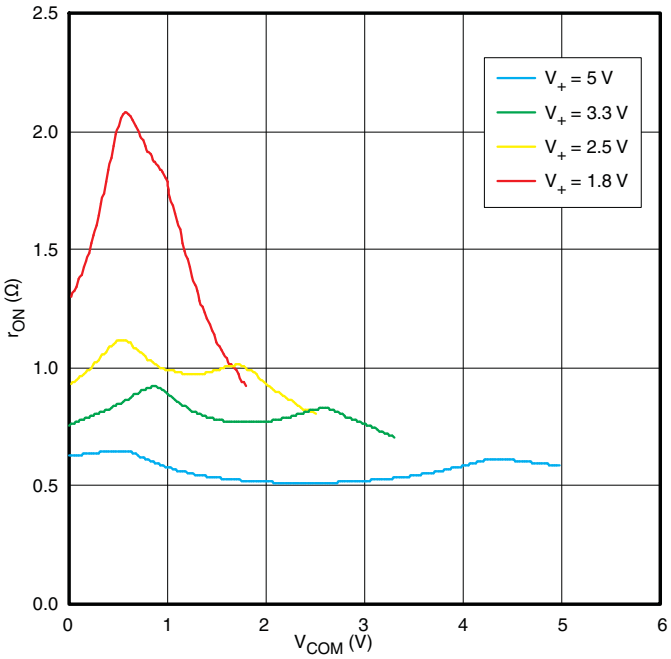


Figure 1. r_{on} vs V_{COM}

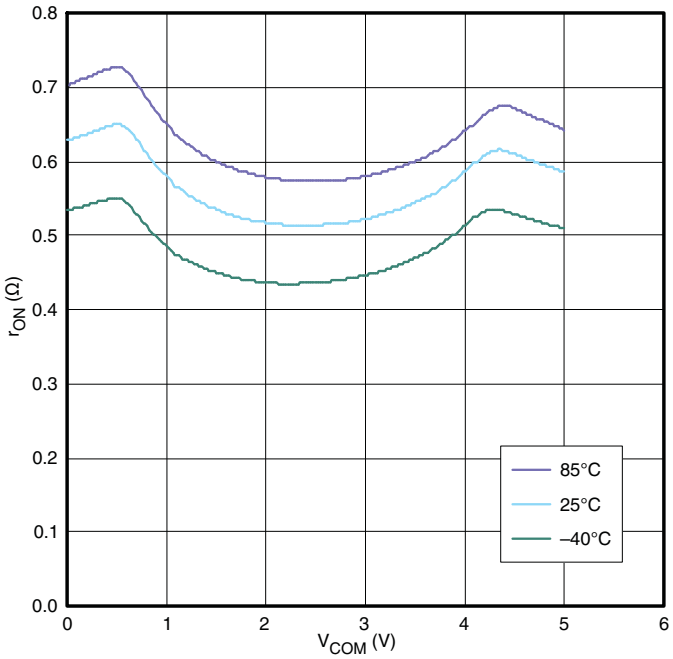


Figure 2. r_{on} vs V_{COM} (V_+ = 5 V)

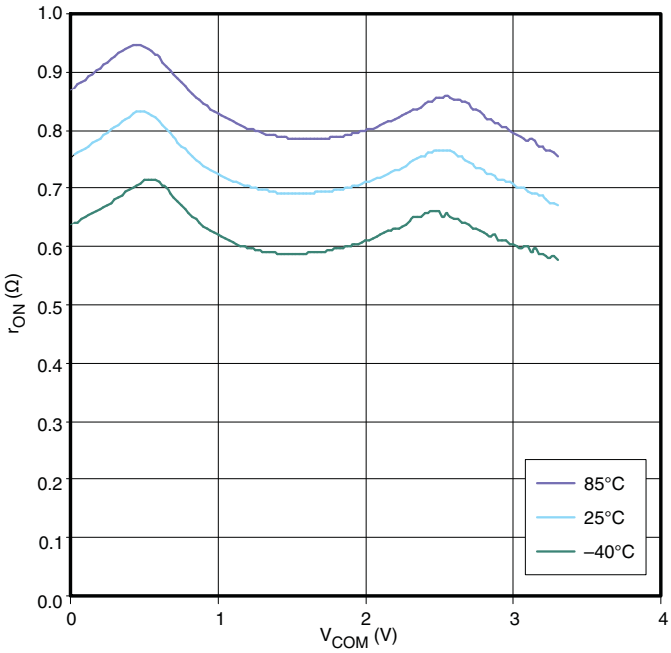


Figure 3. r_{on} vs V_{COM} (V_+ = 3.3 V)

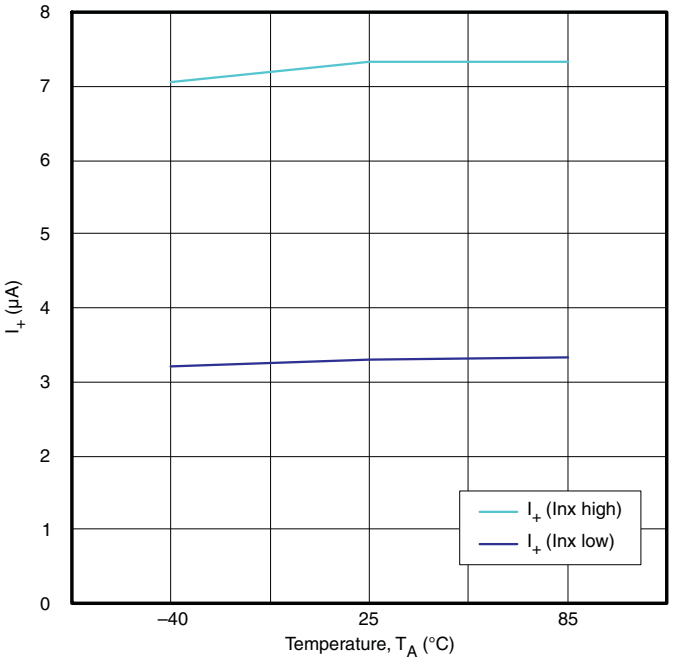


Figure 4. Power-Supply Current vs Temperature (V_+ = 5 V)

TYPICAL PERFORMANCE (continued)

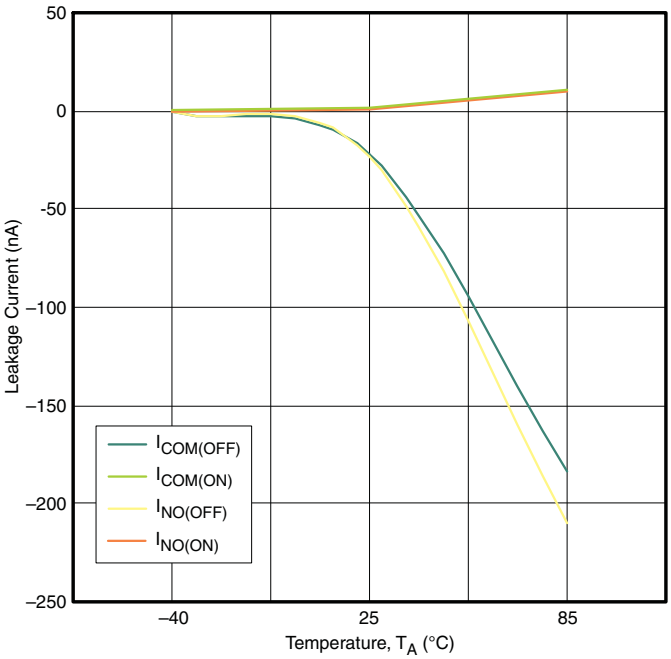


Figure 5. Leakage Current vs Temperature (V_+ = 5.5 V)

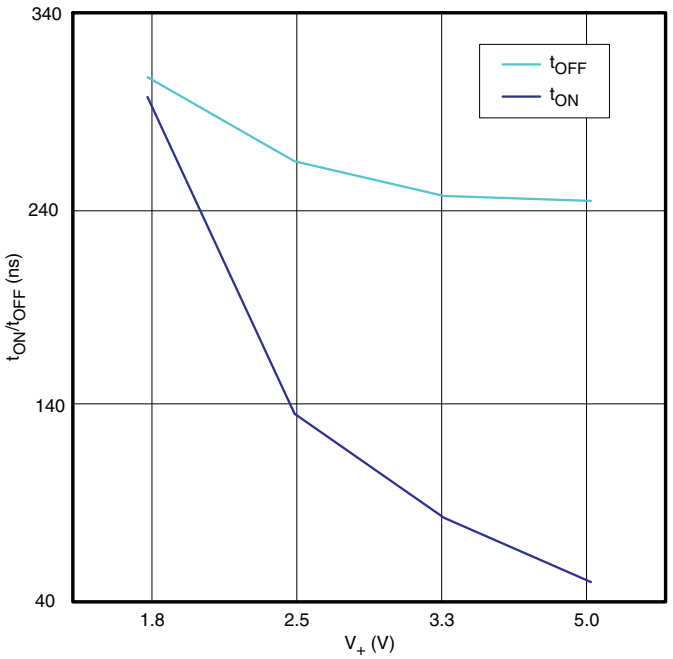


Figure 6. t_{ON}/t_{OFF} vs Supply Voltage

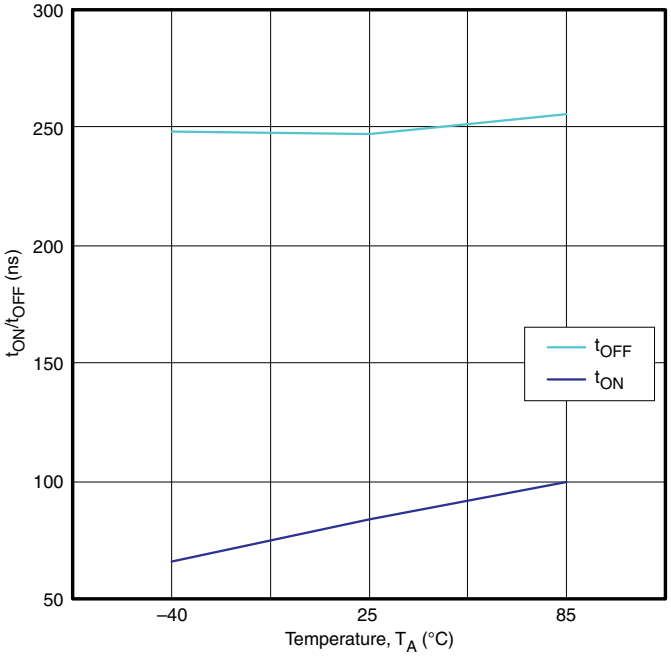


Figure 7. t_{ON}/t_{OFF} vs Temperature (V_+ = 3.3 V)

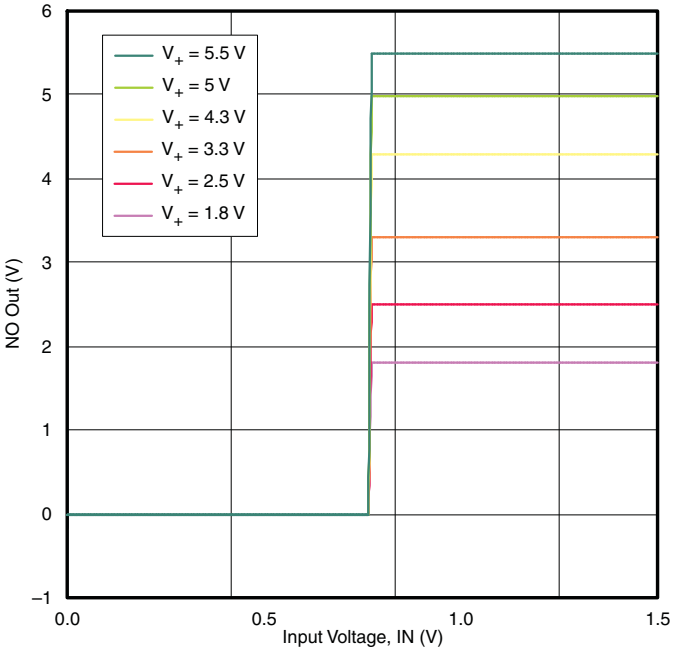


Figure 8. Input Voltage Thresholds

TYPICAL PERFORMANCE (continued)

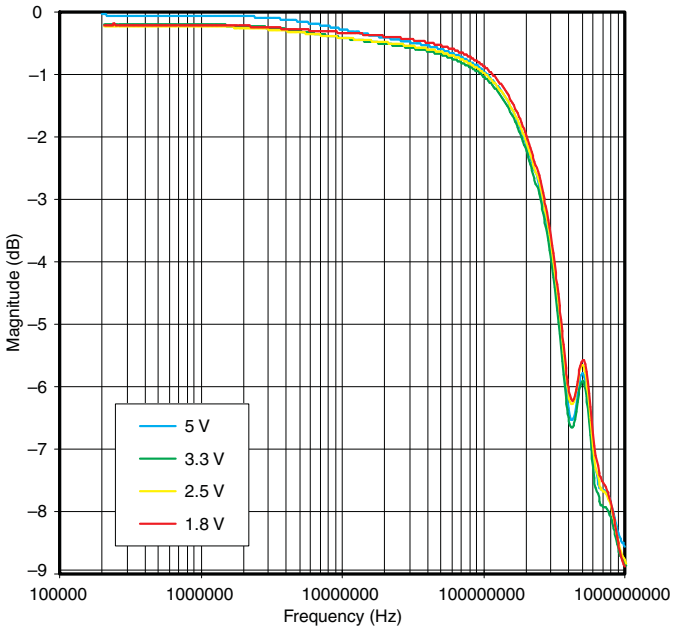


Figure 9. Insertion Loss

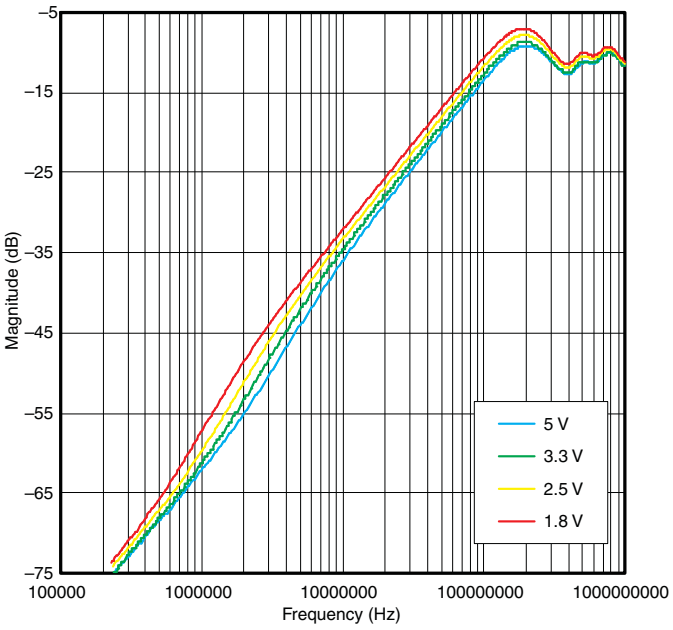


Figure 10. OFF Isolation

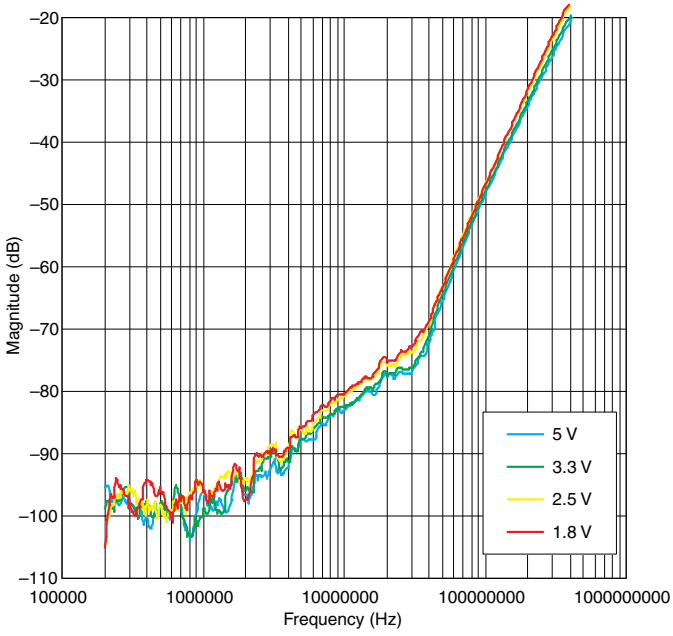


Figure 11. Crosstalk

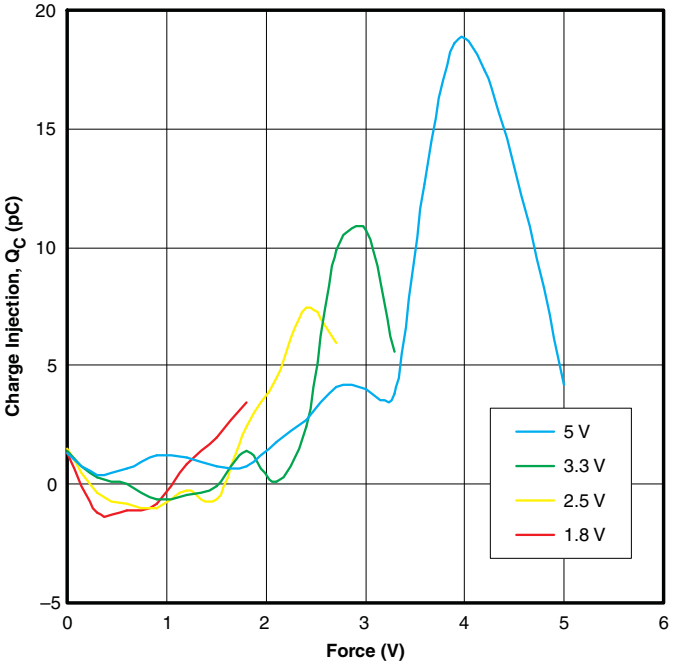


Figure 12. Charge Injection (Q_C) vs Bias Voltage

TYPICAL PERFORMANCE (continued)

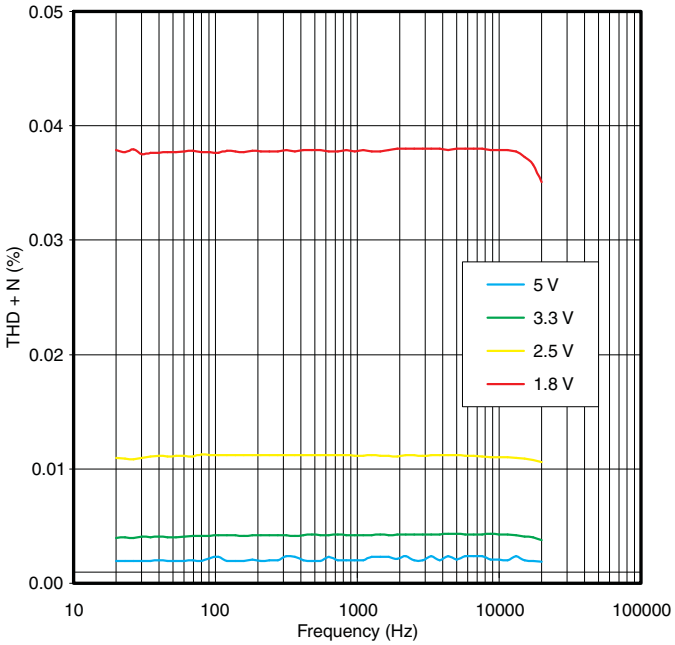


Figure 13. THD + N (%) vs Frequency

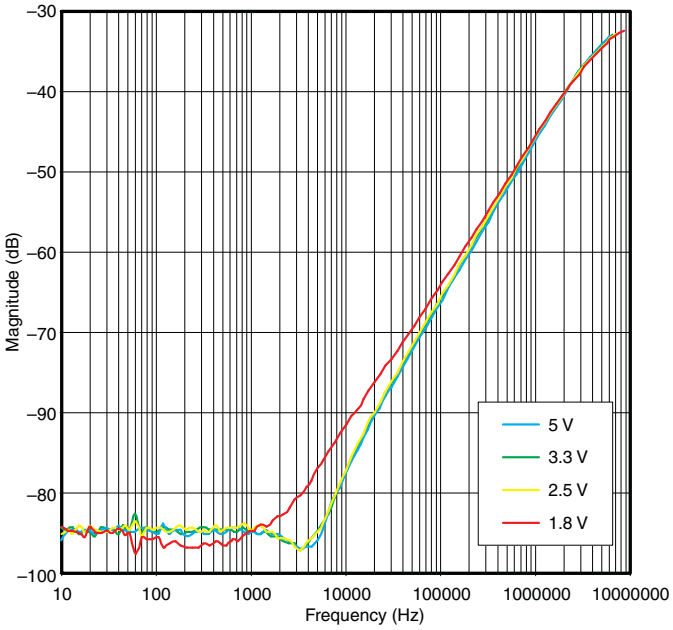


Figure 14. Power Supply Rejection Ratio (PSRR)

PARAMETER MEASUREMENT INFORMATION

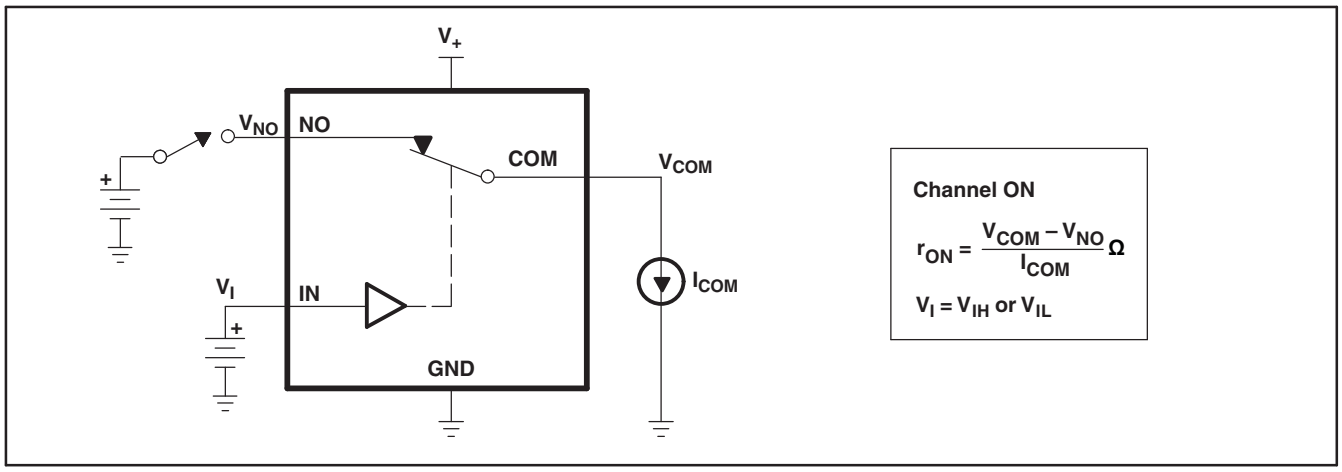


Figure 15. ON-State Resistance (r_{on})

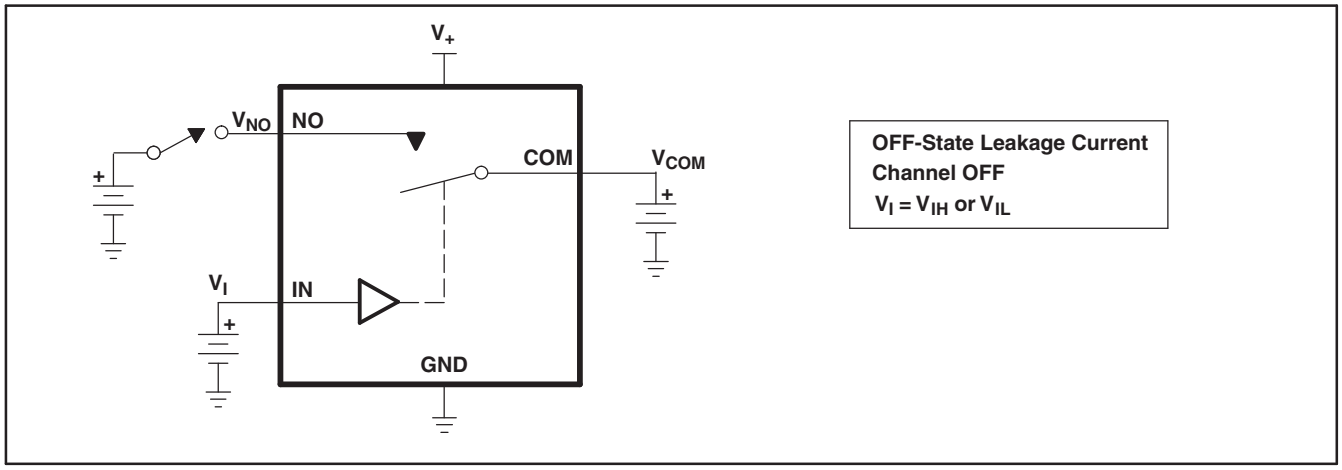


Figure 16. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NOC(PWR(FF)}$)

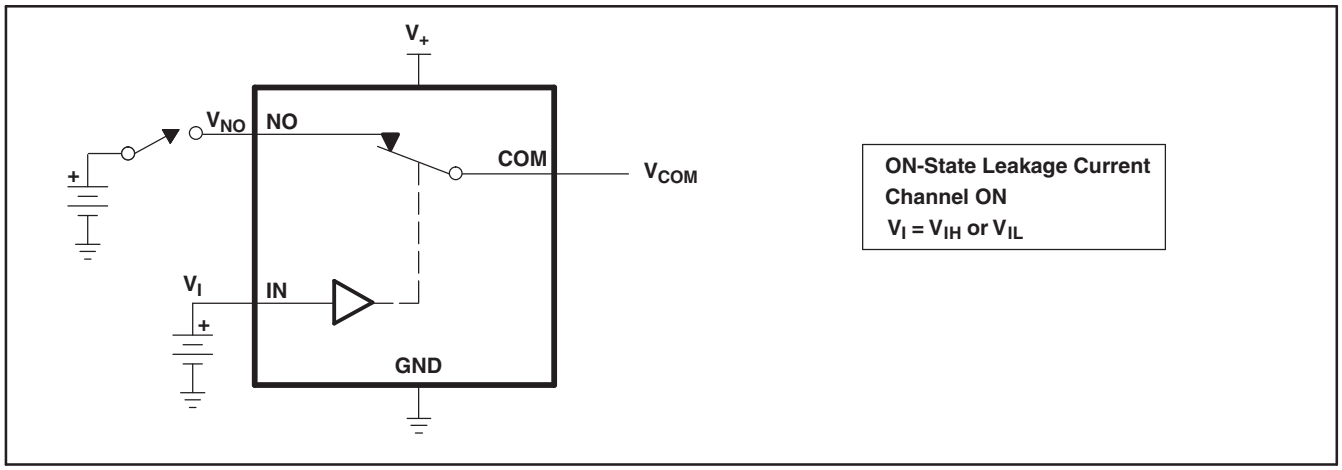


Figure 17. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

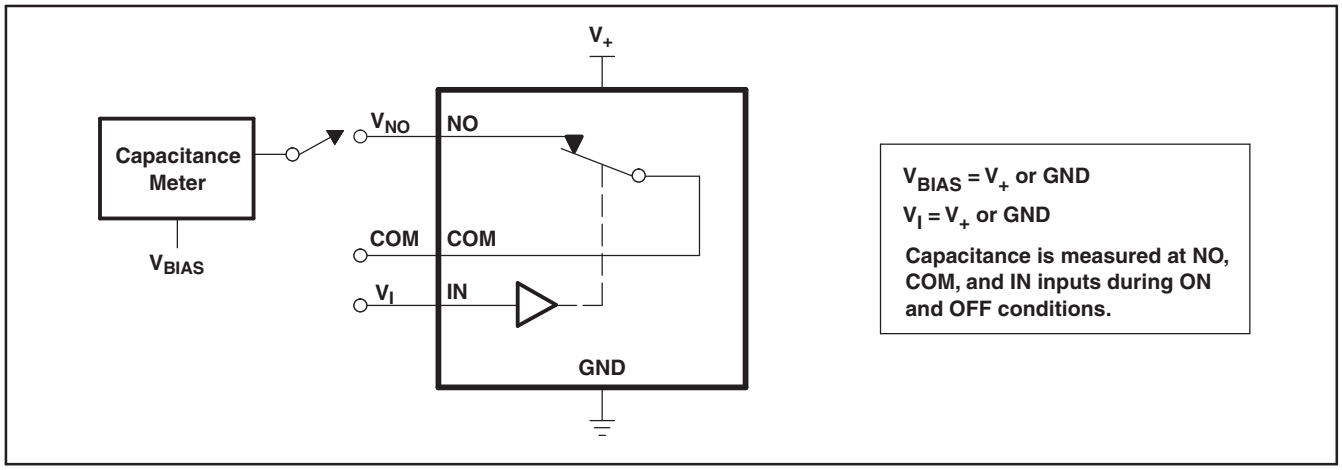
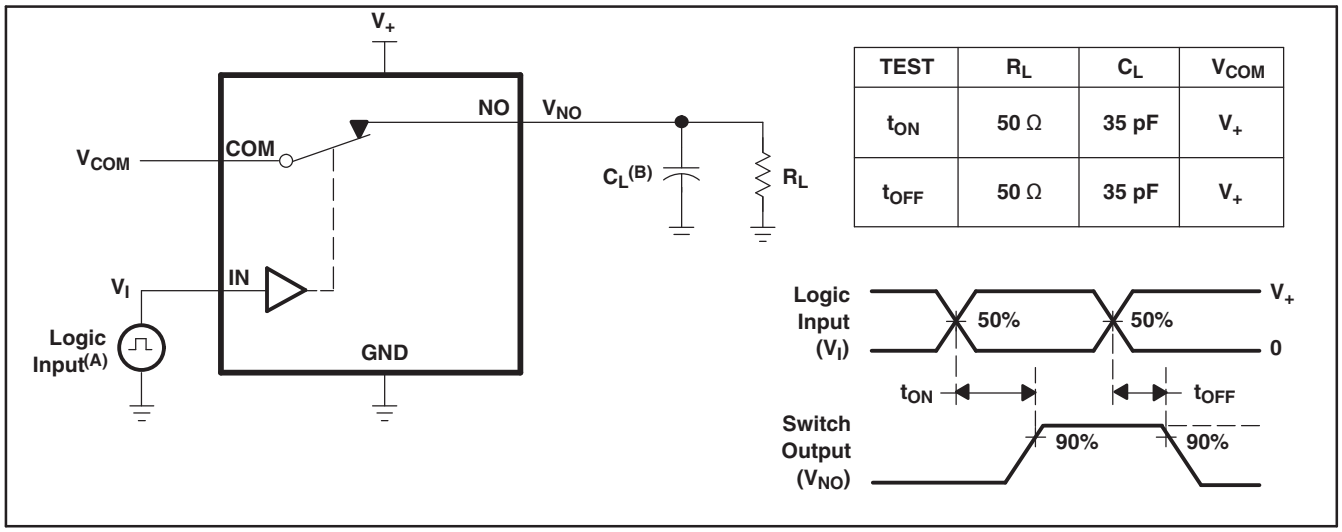


Figure 18. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 5 ns, t_f ≤ 5 ns.

B. C_L includes probe and jig capacitance.

Figure 19. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)

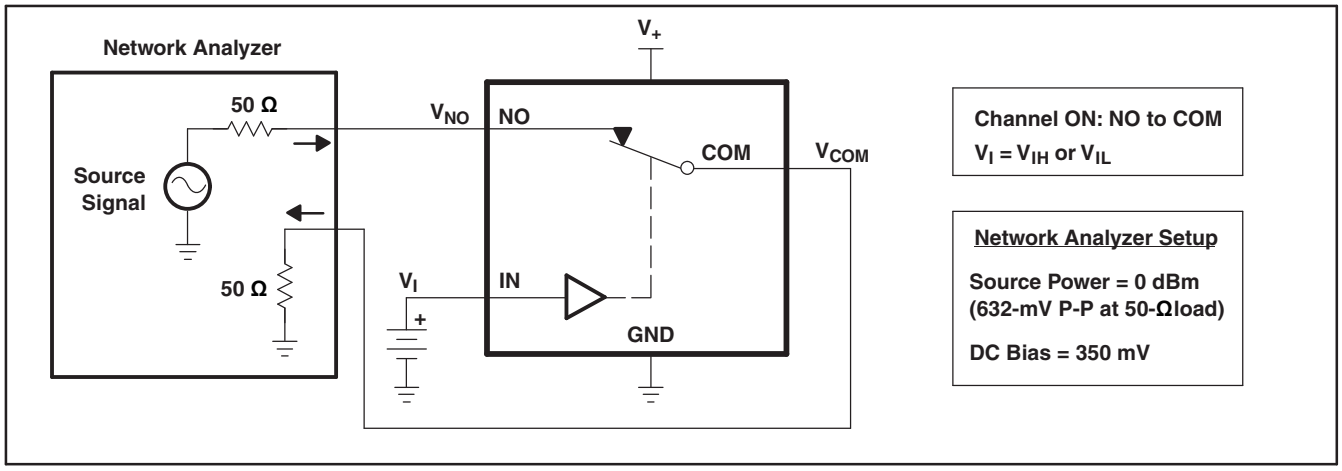


Figure 20. Bandwidth (BW)

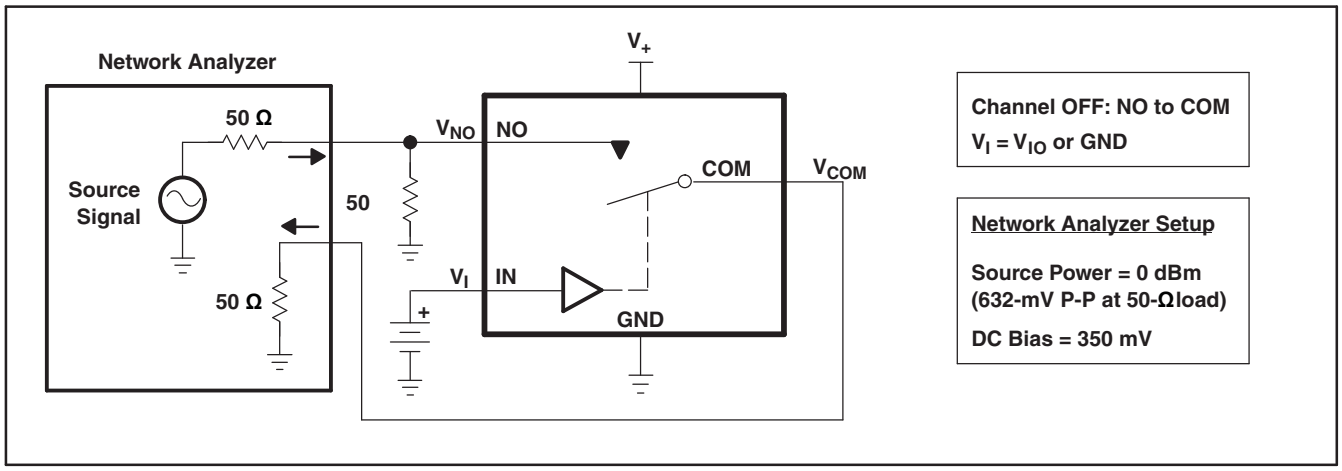


Figure 21. OFF Isolation (O_{ISO})

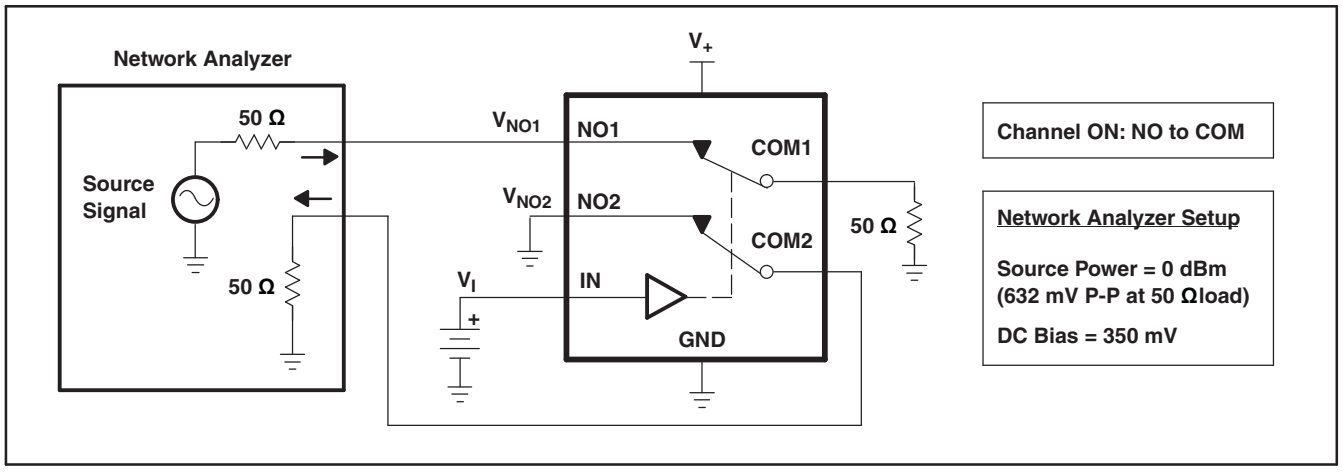
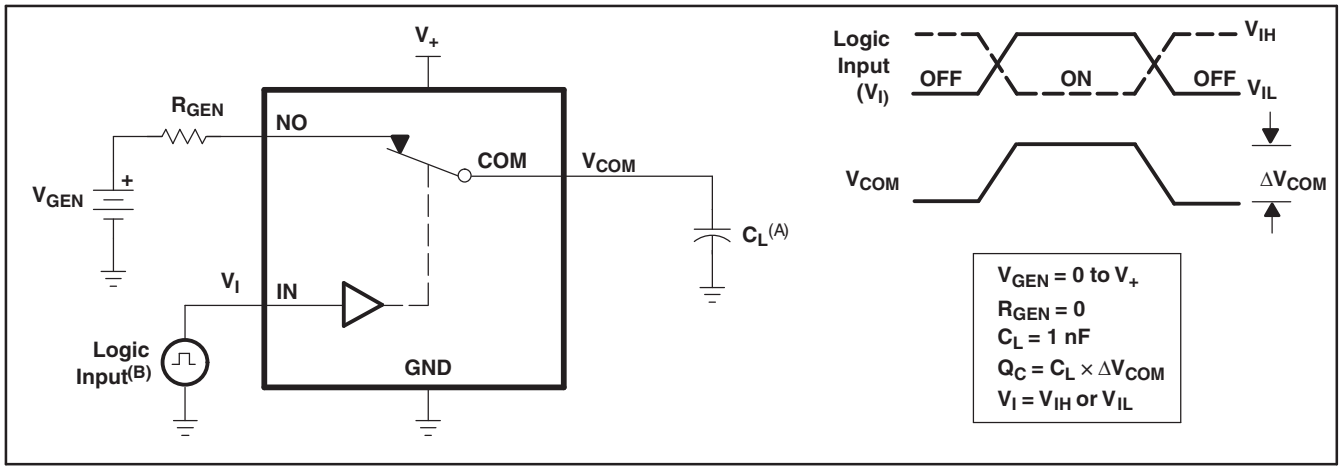


Figure 22. Crosstalk (X_{TALK})

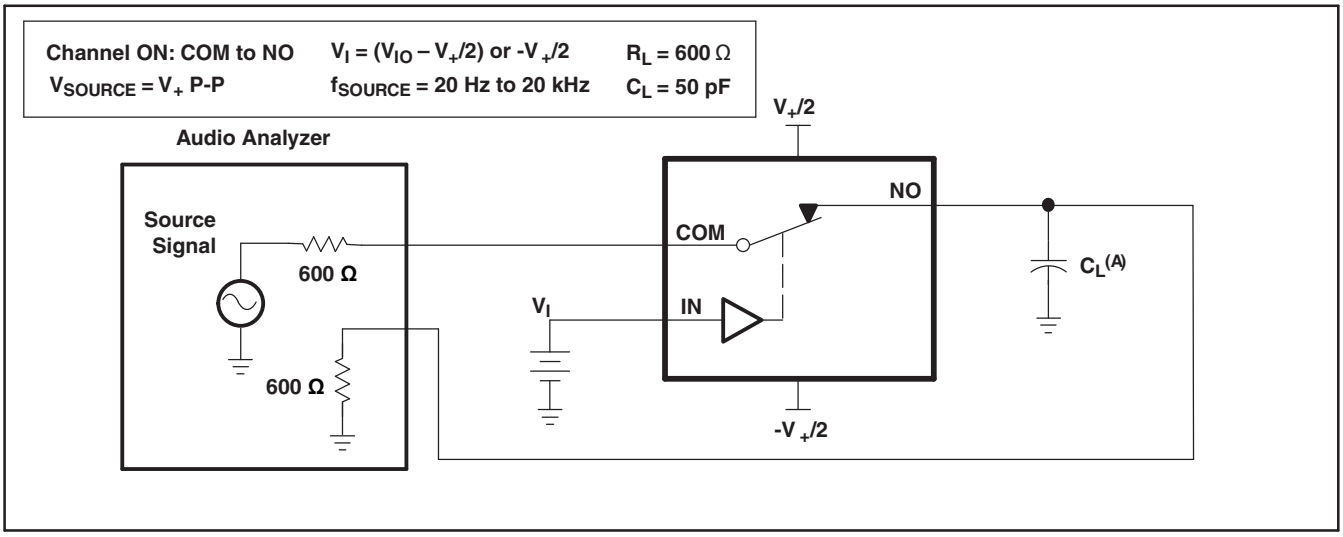
PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 5 ns, t_f ≤ 5 ns.

Figure 23. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

PARAMETER MEASUREMENT INFORMATION (continued)

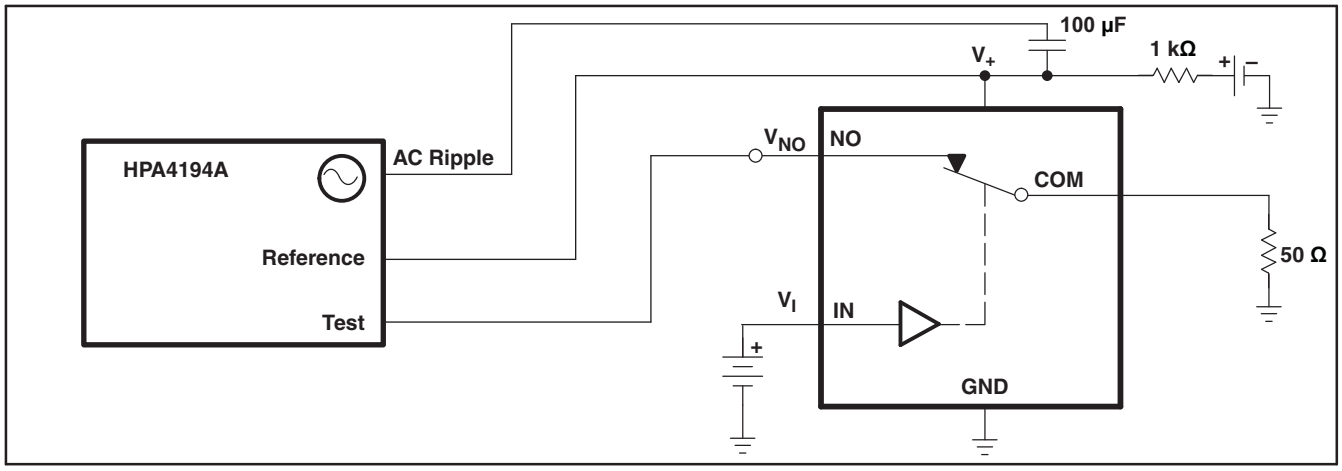


Figure 25. Power Supply Rejection Ratio (PSRR)

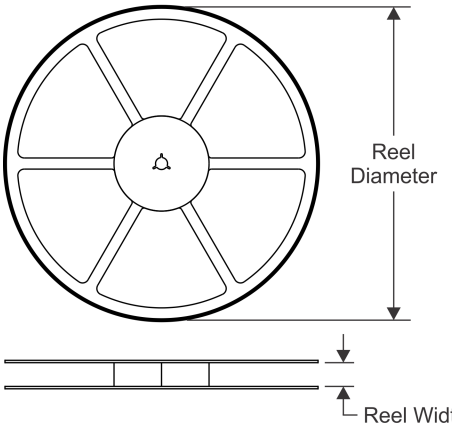
APPLICATION INFORMATION

Independent of V_+, low-voltage GPIO-compatible control inputs

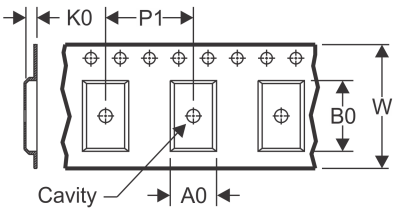
TS5A21366 integrates special control inputs with low threshold allowing the device to be controlled by 1.8-V signals. The thresholds are fixed and independent of the supply value (V_+). The low threshold (V_{IH}, V_{IL}) of the control inputs (IN1, IN2) is achieved by use of an internal bias circuit. To avoid an increased quiescent current (I_+) condition, proper power sequencing must be followed to ensure that the bias circuitry is powered up prior to applying voltage on the I/Os. The proper sequence is for the V_+ pin to be brought up to V_+ before the control inputs (IN1, IN2) are allowed to go to a high level.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

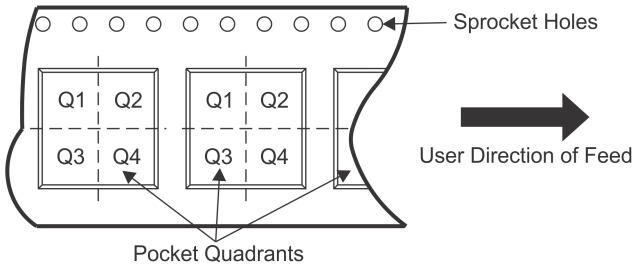


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

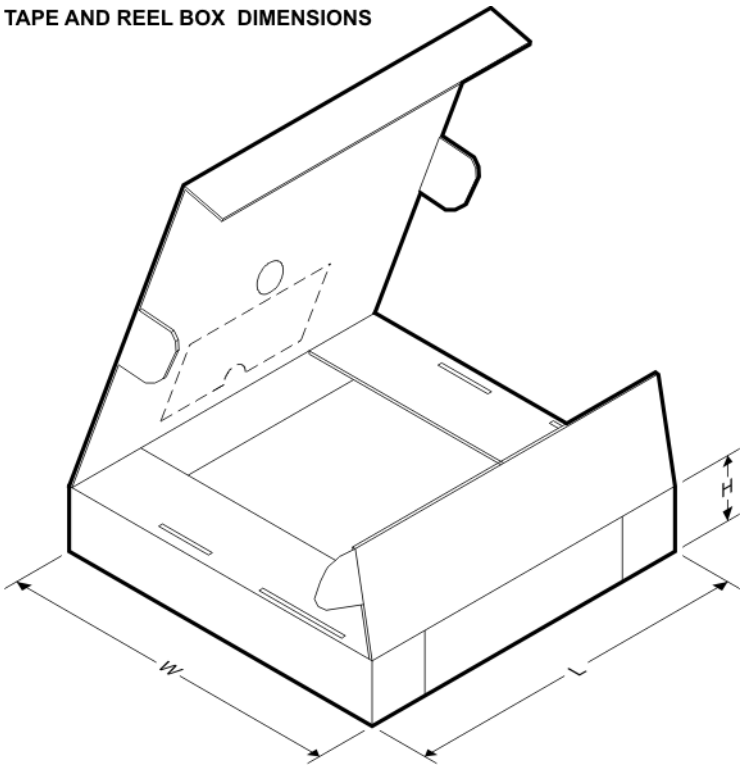
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A21366DCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
TS5A21366DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A21366DCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A21366RSER	UQFN	RSE	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

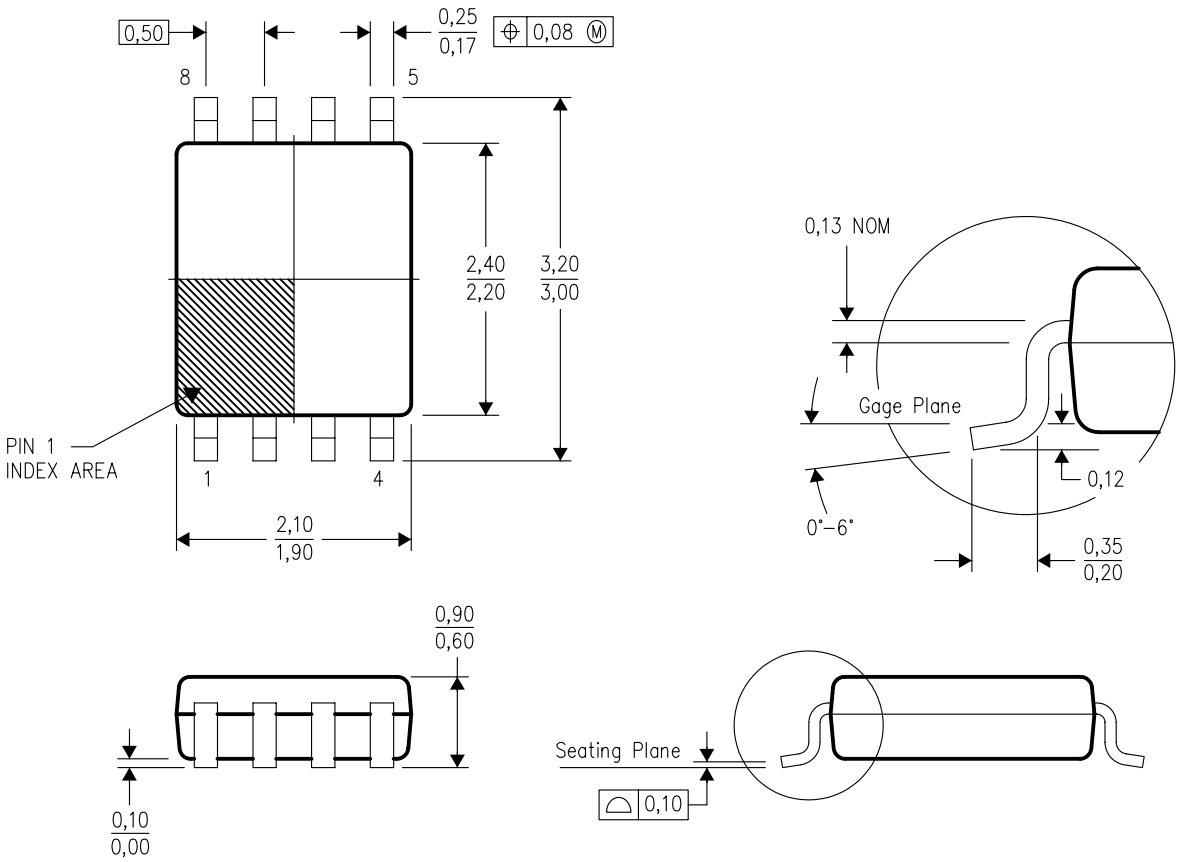
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A21366DCUR	US8	DCU	8	3000	182.0	182.0	20.0
TS5A21366DCUR	US8	DCU	8	3000	202.0	201.0	28.0
TS5A21366DCURG4	US8	DCU	8	3000	202.0	201.0	28.0
TS5A21366RSER	UQFN	RSE	8	3000	202.0	201.0	28.0

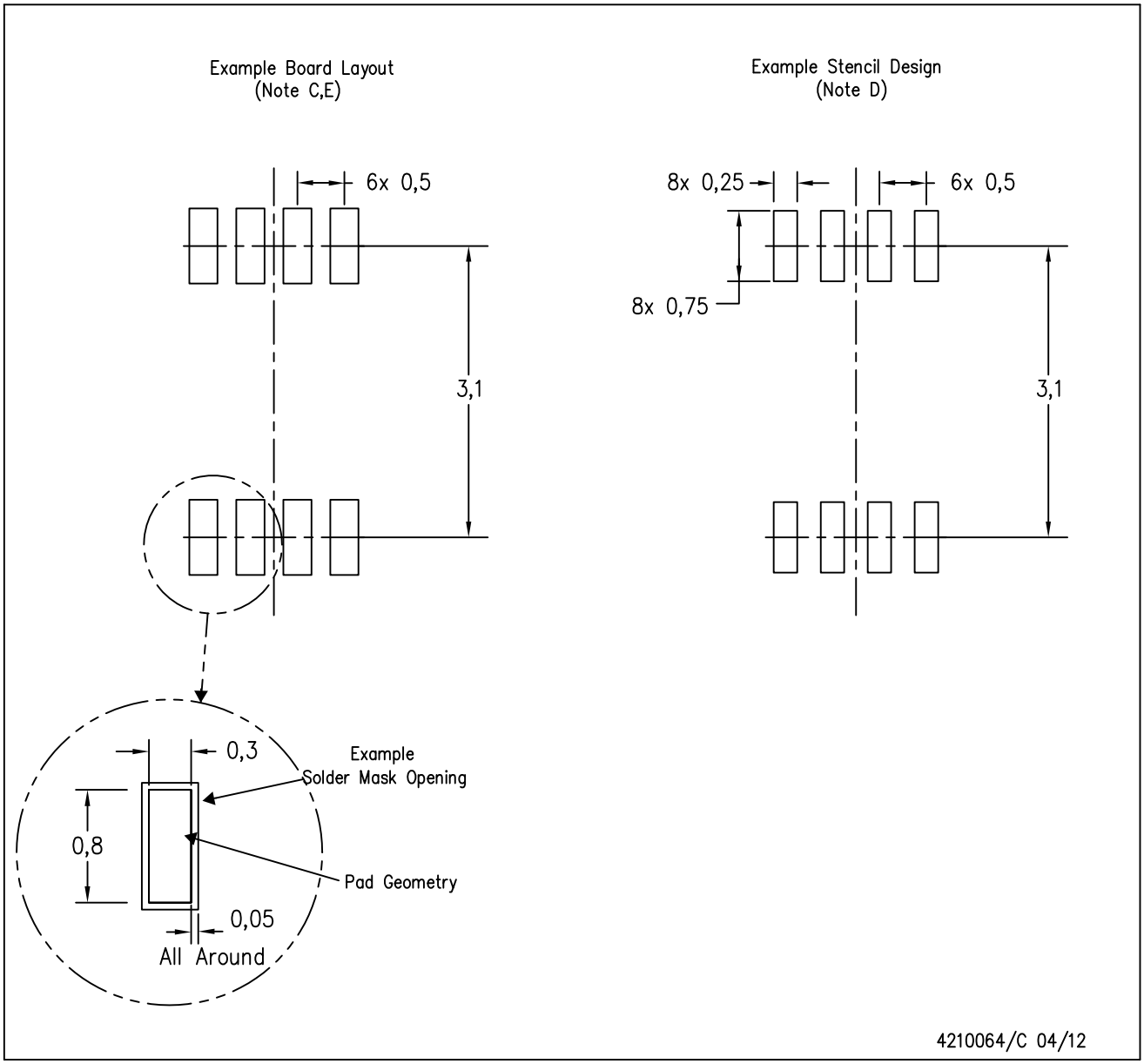
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

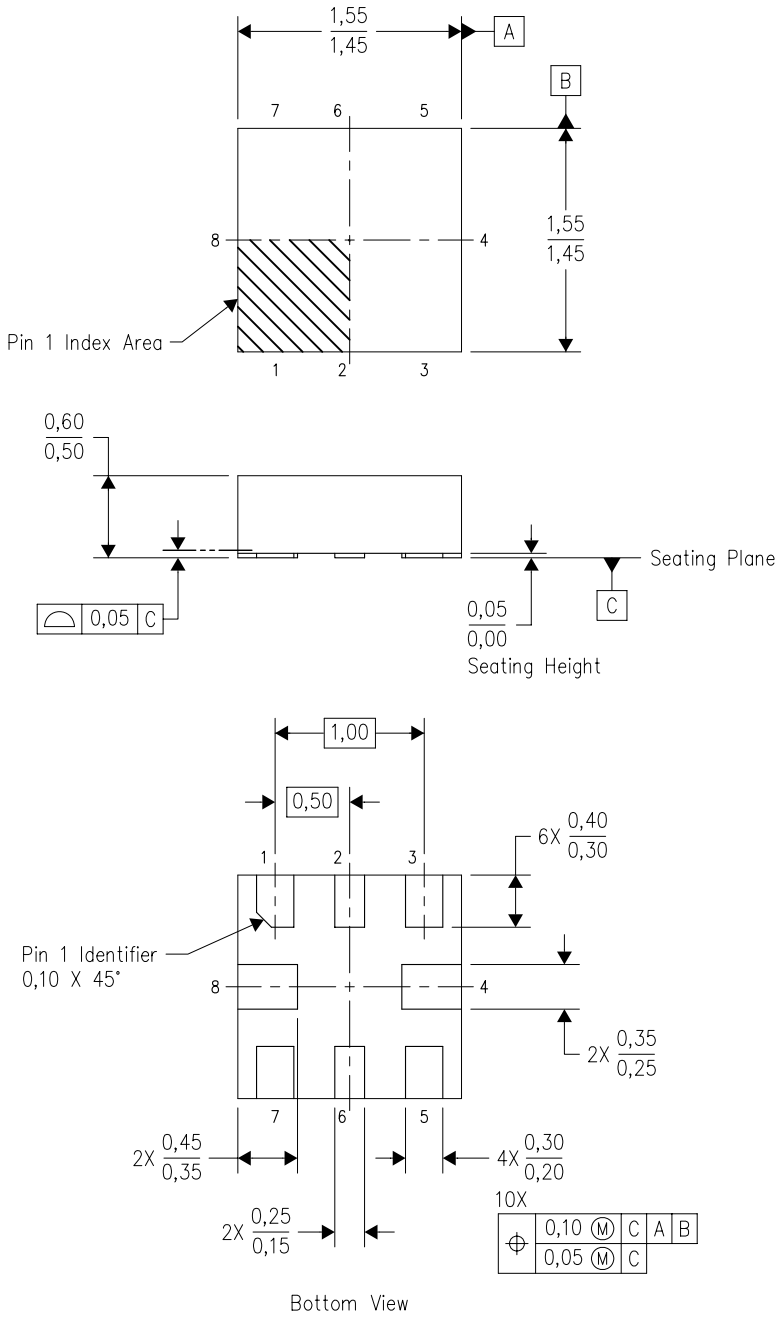
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

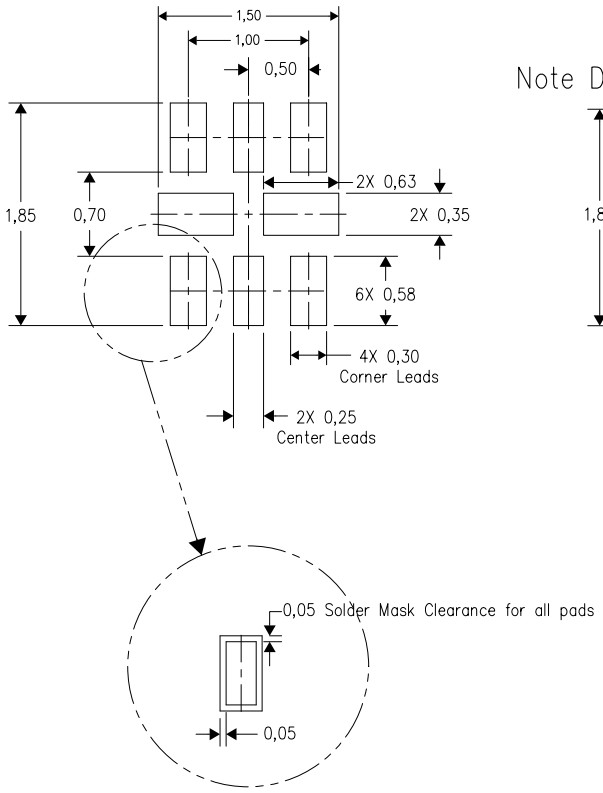


4207268–2/D 01/11

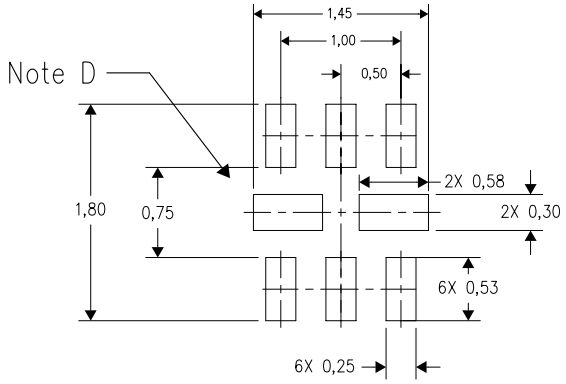
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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